

CLAIMS

What is claimed is:

1. A semiconductor package ~~substrate~~, comprising:
 - a first patch and a second patch on an interposer of the semiconductor package;
 - a first substrate in the first patch, and a second substrate in the second patch;
 - an encapsulation layer over and around the first patch and the second patch;
 - a plurality of build-up layers on the first patch, the second patch, and the encapsulation layer; and
 - a plurality of dies and a bridge on the plurality of build-up layers, wherein the bridge is communicatively coupled with the first substrate of the first patch and the second substrate of the second patch.
2. The semiconductor package ~~substrate~~ of claim 1, wherein the bridge is an embedded multi-die interconnect bridge (EMIB).
3. The semiconductor package ~~substrate~~ of claim 1, wherein the first and second substrates are EMIBs.
4. The semiconductor package ~~substrate~~ of claim 1, wherein the first and second substrates are high-density packaging (HDP) substrates.
5. The semiconductor package ~~substrate~~ of claim 1, wherein the bridge is positioned

between two of the dies, and wherein the bridge is positioned over an edge of the first patch and an edge of the second patch.

6. The semiconductor package ~~substrate~~ of claim 1, wherein the first and second substrates communicatively couple the plurality of dies to the bridge, the first and second patches, and the interposer.

7. The semiconductor package ~~substrate~~ of claim 1, further comprising an underfill material on the interposer and the plurality of build-up layers, wherein the underfill material is between a top surface of the interposer and the encapsulation layer, and wherein the underfill material is on a top surface of the plurality of build-up layers and surrounds surfaces of the bridge and the plurality of dies.

8. The semiconductor package ~~substrate~~ of claim 5, wherein a top surface of the encapsulation layer is substantially coplanar to top surfaces of the first and second patches, and wherein the encapsulation layer is between the edge of the first patch and the edge of the second patch.

9. The semiconductor package ~~substrate~~ of claim 1, wherein the first and second substrates are respectively embedded in the first and second patches, and wherein the first and second patches are embedded in the encapsulation layer.

10. The semiconductor package ~~substrate~~ of claim 1, wherein the plurality of dies, the bridge,

the first and second substrates, and the first and second patches are communicatively coupled to each other by conductive traces and vias in the plurality of build-up layers.

11. A semiconductor package ~~substrate~~, comprising:
a first patch and a second patch on an interposer;
a substrate on the first patch and the second patch;
an encapsulation layer over and around the first patch and the second patch; and
a plurality of dies over the substrate, the first patch, and the second patch, wherein the substrate communicatively couples the plurality of dies to the first and second patches.

12. The semiconductor package ~~substrate~~ of claim 11, wherein the substrate is an EMIB.

13. The semiconductor package ~~substrate~~ of claim 11, wherein the substrate is a HDP substrate.

14. The semiconductor package ~~substrate~~ of claim 12, further comprising:
a plurality of build-up layers on the first and second patches, the encapsulation layer, and the EMIB, wherein the plurality of dies, the EMIB, and the first and second patches are communicatively coupled to each other by conductive traces and vias in the plurality of build-up layers; and
an adhesive layer coupled to a bottom surface of the EMIB and top surfaces of the first and second patches, wherein the plurality of build-up layers embed the EMIB and the adhesive layer, wherein the EMIB is positioned on an edge of the first patch and an edge of the second

patch, and wherein the adhesive layer of the EMIB is on the encapsulation layer between the first and second patches.

15. The semiconductor package substrate of claim 14, further comprising a cavity between the edge of the first patch and the edge of the second patch, wherein the EMIB is in the cavity, and wherein the plurality of build-up layers embed the EMIB and the adhesive layer in the cavity.

16. The semiconductor package substrate of claim 13, wherein the HDP substrate is over the first patch, the second patch, and the encapsulation layer, and wherein the plurality of dies are on the HDP substrate.

17. The semiconductor package substrate of claim 11, wherein the substrate communicatively couples the plurality of dies to the first patch, the second patch, and the interposer.

18. The semiconductor package substrate of claim 14, further comprising an underfill material on the interposer and the plurality of build-up layers, wherein the underfill material is between a top surface of the interposer and the encapsulation layer, and wherein the underfill material is on a top surface of the plurality of build-up layers and surrounds surfaces of the plurality of dies.

19. The semiconductor package substrate of claim 16, further comprising a first underfill

material on the interposer, wherein the first underfill material is between a top surface of the interposer and the encapsulation layer, wherein the first underfill material is on a top surface of the HDP substrate and a bottom surface of the HDP substrate, and wherein the first underfill material is over the first patch, the second patch, and the encapsulation layer.

20. The semiconductor package substrate of claim 11, wherein a top surface of the encapsulation layer is substantially coplanar to top surfaces of the first and second patches, wherein the encapsulation layer is between the first patch and the second patch, and wherein the first and second patches are embedded in the encapsulation layer.

21. A semiconductor package substrate, comprising:
a first patch on an interposer;
a second patch on the interposer;
a plurality of dies over the first patch, the second patch, and the interposer, wherein the plurality of dies are communicatively coupled to the first and second patches.

22. The semiconductor package substrate of claim 21, further comprising:
a cavity between an edge of the first patch and an edge of the second patch;
an EMIB on the edge of the first patch and the edge of the second patch, wherein the EMIB is in the cavity;
a plurality of build-up layers in the cavity, wherein the plurality of build-up layers is between the edge of the first patch and the edge of the second patch, wherein the plurality of dies, the EMIB, and the first and second patches are communicatively coupled to each other by

conductive traces and vias in the plurality of build-up layers;

an adhesive layer coupled to a bottom surface of the EMIB and top surfaces of the first and second patches, wherein the plurality of build-up layers embed the EMIB and the adhesive layer in the cavity, wherein the EMIB is positioned on the edge of the first patch and the edge of the second patch, and wherein the adhesive layer of the EMIB is on the plurality of build-up layers between the first and second patches; and

an underfill material on the interposer, wherein the underfill material is over the first and second patches, the EMIB, and the plurality of build-up layers, wherein the underfill material is between the interposer and bottom surfaces of the first patch, the second patch, and the plurality of build-up layers, and wherein the underfill material surrounds surfaces of the plurality of dies.

23. The semiconductor package substrate of claim 21, further comprising:

a first HDP substrate on the first and second patches, wherein the first HDP substrate communicatively couples the plurality of dies to the first and second patches; or

a second HDP substrate on the interposer, wherein the second HDP substrate communicatively couples the first and second patches to the interposer.

24. The semiconductor package substrate of claim 23, further comprising a first underfill material on the interposer, wherein the first underfill material is between the first and second patches, wherein the first underfill material is on a top surface of the first HDP substrate and a bottom surface of the first HDP substrate, and wherein the first underfill material is over the first and second patches.

25. The semiconductor package substrate of claim 23, further comprising a second underfill material on the interposer, wherein the second underfill material is between the first and second patches, wherein the second underfill material is on a top surface of the second HDP substrate and a bottom surface of the second HDP substrate, and wherein the second underfill material is over the first and second patches.