WHAT IS CLAIMED IS:

1. A bevel etcher wherein a bevel edge of a semiconductor substrate is subjected to plasma cleaning, comprising:

a lower support having a cylindrical top portion;

a lower plasma-exclusion-zone (PEZ) ring supported on the top portion of the lower support, the lower PEZ ring having an upper surface on which the substrate is supported such that the bevel edge of the substrate extends outwardly of an outer edge of the upper surface;

an upper dielectric component disposed above the lower support and having a cylindrical bottom portion opposing the top portion of the lower support;

an upper PEZ ring surrounding the bottom portion of the dielectric component and opposing the lower PEZ ring, an annular space between the lower and upper PEZ rings limiting the extent of the bevel edge to be cleaned by the plasma; and

at least one radio frequency (RF) power source adapted to energize process gas into the plasma during a cleaning operation;

wherein the lower and upper PEZ rings are adapted to respectively shield the lower support and the upper dielectric component from the plasma during the cleaning operation.

2. The bevel etcher as recited in claim 1, wherein the at least one RF power source includes:

a lower electrode ring surrounding the lower PEZ ring; and

an upper electrode ring surrounding the upper PEZ ring and opposing the lower electrode ring.

3. The bevel etcher as recited in claim 2, wherein (a) the lower and upper electrode rings are grounded and the lower support is coupled to a radio frequency (RF) power generator supplying RF power to generate the plasma; (b) the lower electrode ring is grounded and the upper electrode ring is coupled to a radio frequency (RF) power generator supplying RF power to generate the plasma; or (c)

the upper electrode ring is grounded and the lower electrode ring is coupled to a radio frequency (RF) power generator supplying RF power to generate the plasma.

4. The bevel etcher as recited in claim 3, wherein the top portion of the lower support is formed of a dielectric material.

5. The bevel etcher as recited in claim 2, wherein the upper and lower electrode rings are formed of a material selected from the group consisting of metal, Si, SiC, and carbon based materials.

6. The bevel etcher as recited in claim 2, further comprising:

an upper metal component overlying the upper dielectric component, the upper electrode ring and upper PEZ ring;

an upper dielectric ring surrounding the upper electrode ring and secured to the upper metal component, the upper dielectric ring including a flange clamping the upper electrode ring to the upper metal component;

a lower metal liner underlying the lower electrode ring;

a lower dielectric ring surrounding the lower electrode ring and secured to the lower metal liner, the lower dielectric ring including a flange clamping the lower electrode ring to the lower metal liner; and

a focus ring interposed between the lower support and the lower metal liner and adapted to electrically separate the lower support from the lower metal liner and from the lower electrode ring.

7. The bevel etcher as recited in claim 6, wherein the upper metal component includes at least one gas passage adapted to be coupled to a gas source containing process gas, the upper electrode ring is separated from the upper PEZ ring by a gap, and the gap is in fluid communication with the at least one gas passage via a tortuous path through which the process gas flows from the gas supply to the annular space.

8. The bevel etcher as recited in claim 6, wherein: (a) the lower dielectric ring includes threaded holes receiving bolts passing through holes in the lower metal liner, wherein the bolts secure the lower dielectric ring against the lower metal liner; (b) the upper dielectric ring includes threaded holes receiving bolts passing through holes in the upper metal component, wherein the bolts secure the upper dielectric ring against the upper metal component; (c) the focus ring and the upper dielectric component are formed of a ceramic optionally coated with Y_2O_3; and/or (d) the lower and upper dielectric rings are formed of a ceramic.

9. The bevel etcher as recited in claim 7, further comprising: (a) a hollow cathode ring surrounding the outer edges of the lower and upper dielectric rings, wherein either the hollow cathode ring is coupled to an RF power generator and the upper and lower electrode rings are grounded or the upper and lower electrode rings are coupled to an RF power generator and the hollow cathode ring is grounded during a bevel cleaning operation; or (b) an inductive coil coupled to an RF generator and surrounding the outer edges of the lower and upper dielectric rings, the upper and lower electrode rings being grounded and the coil operative to generate the plasma upon receipt of RF power from the RF generator.

10. The bevel etcher as recited in claim 2, wherein (a) the upper dielectric component has a ring-shaped flange formed along the outer edge of the bottom portion and wherein the upper PEZ ring has a mating inner flange formed along the inner edge thereof, the ring-shaped flange engaging the inner flange such that the upper PEZ ring is detachably secured to the upper dielectric component and/or (b) the lower support has a ring-shaped flange formed along the outer edge of the top portion and wherein the lower PEZ ring has a mating inner flange formed along the inner edge thereof, the ring-shaped flange engaging the inner flange such that the lower PEZ ring is detachably secured to the lower support.

11. The bevel etcher as recited in claim 1, wherein: (a) the outer diameter of the top portion of the lower PEZ ring defines the bottom edge exclusion of the substrate; (b) the lower and upper PEZ rings are formed of a material selected from

the group consisting of an electrically conductive, semiconductive, dielectric material, a ceramic, and a high electrical resistance material; (c) the outer diameter of the bottom portion of the upper PEZ ring defines the top edge exclusion of the substrate; and/or (d) the cylindrical top portion of the lower support includes an electrostatic chuck.

12. A method of cleaning the bevel edge of a semiconductor substrate, comprising:

supporting a semiconductor substrate in the bevel etcher according to claim 1;

energizing process gas into a plasma; and

cleaning the bevel edge with the plasma.

13. A method of replacing the upper or lower PEZ ring in the bevel etcher according to claim 6, comprising: (a) detaching the upper dielectric component from the upper metal component, disengaging a flange on the dielectric component from a flange on the upper PEZ ring, replacing the upper PEZ ring with a new PEZ ring by fitting the new PEZ ring on the dielectric plate and attaching the dielectric plate to the upper metal component or (b) lifting the lower PEZ ring above the lower support and replacing the lower PEZ ring with a new PEZ ring.

WHAT IS CLAIMED IS:

1. A bevel etcher wherein a bevel edge of a semiconductor substrate is subjected to plasma cleaning, comprising:

a lower support having a cylindrical top portion;

a lower plasma-exclusion-zone (PEZ) ring supported on the top portion of the lower support, the lower PEZ ring having an upper surface on which the substrate is supported such that the bevel edge of the substrate extends outwardly of an outer edge of the upper surface;

an upper dielectric component disposed above the lower support and having a cylindrical bottom portion opposing the top portion of the lower support;

an upper PEZ ring surrounding the bottom portion of the dielectric component and opposing the lower PEZ ring, an annular space between the lower and upper PEZ rings limiting the extent of the bevel edge to be cleaned by the plasma; and

at least one radio frequency (RF) power source adapted to energize process gas into the plasma during a cleaning operation;

wherein the lower and upper PEZ rings are adapted to respectively shield the lower support and the upper dielectric component from the plasma during the cleaning operation;

wherein: (a) the outer diameter of the top portion of the lower PEZ ring defines the bottom edge exclusion of the substrate; (b) the lower and upper PEZ rings are formed of a material selected from the group consisting of an electrically conductive, semiconductive, dielectric material, a ceramic, and a high electrical resistance material; (c) the outer diameter of the bottom portion of the upper PEZ ring defines the top edge exclusion of the substrate; and/or (d) the cylindrical top portion of the lower support includes an electrostatic chuck;

wherein the at least one RF power source includes a lower electrode ring surrounding the lower PEZ ring; and an upper electrode ring surrounding the upper PEZ ring and opposing the lower electrode ring; and

wherein the upper and lower electrode rings are formed of a SiC.

2. A bevel etcher wherein a bevel edge of a semiconductor substrate is subjected to plasma cleaning, comprising:

a lower support having a cylindrical top portion;

a lower plasma-exclusion-zone (PEZ) ring supported on the top portion of the lower support, the lower PEZ ring having an upper surface on which the substrate is supported such that the bevel edge of the substrate extends outwardly of an outer edge of the upper surface;

an upper dielectric component disposed above the lower support and having a cylindrical bottom portion opposing the top portion of the lower support;

an upper PEZ ring surrounding the bottom portion of the dielectric component and opposing the lower PEZ ring, an annular space between the lower and upper PEZ rings limiting the extent of the bevel edge to be cleaned by the plasma; and

at least one radio frequency (RF) power source adapted to energize process gas into the plasma during a cleaning operation;

wherein the lower and upper PEZ rings are adapted to respectively shield the lower support and the upper dielectric component from the plasma during the cleaning operation;

wherein: (a) the outer diameter of the top portion of the lower PEZ ring defines the bottom edge exclusion of the substrate; (b) the lower and upper PEZ rings are formed of a material selected from the group consisting of an electrically conductive, semiconductive, dielectric material, a ceramic, and a high electrical resistance material; (c) the outer diameter of the bottom portion of the upper PEZ ring defines the top edge exclusion of the substrate; and/or (d) the cylindrical top portion of the lower support includes an electrostatic chuck;

wherein the at least one RF power source includes a lower electrode ring surrounding the lower PEZ ring; and an upper electrode ring surrounding the upper PEZ ring and opposing the lower electrode ring; and

further comprising:

an upper metal component overlying the upper dielectric component, the upper electrode ring and upper PEZ ring;

an upper dielectric ring surrounding the upper electrode ring and secured to the upper metal component, the upper dielectric ring including a flange clamping the upper electrode ring to the upper metal component;

a lower metal liner underlying the lower electrode ring;

a lower dielectric ring surrounding the lower electrode ring and secured to the lower metal liner, the lower dielectric ring including a flange clamping the lower electrode ring to the lower metal liner; and

a focus ring interposed between the lower support and the lower metal liner and adapted to electrically separate the lower support from the lower metal liner and from the lower electrode ring.

3. The bevel etcher as recited in claim 2, wherein the upper metal component includes at least one gas passage adapted to be coupled to a gas source containing process gas, the upper electrode ring is separated from the upper PEZ ring by a gap, and the gap is in fluid communication with the at least one gas passage via a tortuous path through which the process gas flows from the gas supply to the annular space.

4. The bevel etcher as recited in claim 2, wherein: (a) the lower dielectric ring includes threaded holes receiving bolts passing through holes in the lower metal liner, wherein the bolts secure the lower dielectric ring against the lower metal liner; (b) the upper dielectric ring includes threaded holes receiving bolts passing through holes in the upper metal component, wherein the bolts secure the upper dielectric ring against the upper metal component; (c) the focus ring and the upper dielectric component are formed of a ceramic optionally coated with Y_2O_3; and/or (d) the lower and upper dielectric rings are formed of a ceramic.

5. A configurable part of a bevel etcher wherein a bevel edge of a semiconductor substrate is subjected to plasma cleaning, the bevel etcher including a lower electrode assembly on which the wafer is supported during the bevel cleaning operation, an upper electrode assembly including a dielectric plate facing the lower support and attached to an upper support which is movable vertically to position the dielectric plate at a small distance from the upper surface of the substrate, the upper electrode assembly including at least one gas passage through which gas can be flowed in the vicinity of the bevel edge during the bevel cleaning operation, the dielectric plate having at least one gas passage through which gas can be flowed over the surface of the substrate during the bevel cleaning operation, the configurable part comprising at least one of: (1) a lower plasma-exclusion-zone (PEZ) ring of electrically conductive, semiconductive or dielectric material adapted to shield the lower support from the plasma during the cleaning operation, (2) an upper PEZ ring of electrically conductive, semiconductive or dielectric material adapted to shield the upper dielectric plate from the plasma during the cleaning operation, (3) an upper ring electrode surrounding the upper PEZ ring, (4) a lower ring electrode surrounding the lower PEZ ring, (5) an upper dielectric ring surrounding the upper electrode ring, and/or (6) a lower dielectric ring surrounding the lower electrode.

6. The configurable part of claim 5, wherein: (a) the configurable part is the lower PEZ ring, the lower PEZ ring having a lower surface adapted to be supported on the lower support, the lower PEZ ring having an upper surface configured to support the substrate such that the bevel edge of the substrate extends outwardly of an outer edge of the upper surface, the lower surface being wider than the upper surface and/or (b) the configurable part is the upper PEZ ring, the upper PEZ ring including an inner flange having a lower surface thereof engaging an upper surface of an outer flange on the dielectric plate such that when mounted in the bevel etcher an annular space is formed between the lower and upper PEZ rings limiting the extent of the bevel edge to be cleaned by the plasma.

7. The configurable part of claim 5, wherein: (a) the configurable part is the upper ring electrode, the upper ring electrode having an inner diameter adapted to fit closely around the upper PEZ ring, the upper ring electrode having an outer flange adapted to engage the inner flange on an upper dielectric ring which clamps the upper ring electrode to the upper support and/or (b) the configurable part is the lower ring electrode, the lower ring electrode having an inner diameter adapted to fit closely around the lower PEZ ring, the lower ring electrode having an outer flange adapted to engage an inner flange on the lower dielectric ring which clamps the lower ring electrode to the lower support.

8. The configurable part of claim 5, wherein the configurable part is the upper dielectric ring, the upper dielectric ring including an inner flange adapted to engage an outer flange on the upper ring electrode and clamp the upper ring electrode to the upper support, the upper dielectric ring including holes in an upper surface thereof adapted to align with holes in the upper support through which fasteners can be secured to the upper dielectric ring.

9. The configurable part of claim 5, wherein the configurable part is the lower dielectric ring, the lower dielectric ring including an inner flange adapted to engage an outer flange on the lower ring electrode and clamp the lower ring electrode to the lower support, the lower dielectric ring including holes in a lower surface thereof adapted to align with holes in the lower support through which fasteners can be secured to the lower dielectric ring.

10. The configurable part of claim 6, wherein the lower PEZ ring includes a stepped inner surface extending vertically between the lower surface and the upper surface, the upper and lower surfaces being parallel to each other, and an outer surface which is stepped such that an open space underlies the substrate when the substrate is supported on the lower PEZ ring.

11. The configurable part of claim 7, wherein the upper PEZ ring includes a stepped inner surface extending vertically between upper and lower surfaces thereof, the upper and lower surfaces being parallel to each other, and an outer surface which is stepped such that an open space overlies the substrate when the substrate is supported on the lower PEZ ring.