CLAIMS

What is claimed is:

1. An apparatus comprising:

an interface device disposed above or below a processor module, the interface device including a plurality of routing elements;

at least one memory device disposed above or below the interface device and including a first plurality of memory arrays, the first plurality of memory arrays coupled to the interface device using a plurality of interconnects provided in vias in at least one of the interface device and the memory device; and

wherein the interface device is configured to communicatively couple the first plurality of memory arrays to the processor module using the plurality of routing elements and the interconnects.

2. The apparatus of claim 1, wherein the interface device is configured to provide memory commands to the memory device.

3. The apparatus of claim 1, further comprising a second memory device including a second plurality of memory arrays.

4. The apparatus of claim 3, wherein the first memory device further comprises another plurality of interconnects provided in vias to couple the second plurality of memory arrays to the plurality of routing elements in the interface device.

5. The apparatus of claim 4, wherein the interface device includes circuitry configured to perform sequencing of at least one DRAM array.

6. The apparatus of claim 1, wherein the interface device is configured to perform power management of the apparatus, and wherein the interface device is configured to operate at a voltage sufficient to preclude error bit generation.

7. The apparatus of claim 1, wherein the interface device further comprises an input/output driver circuit.

8. The apparatus of claim 1, wherein the interface device is configured to implement a refresh scheme to control error rates based on the type of array used in the memory device.

9. The apparatus of claim 1, wherein the interface device is configured to implement a refresh scheme to control error rates based on the signal characteristics of the memory device.

10. The apparatus of claim 3, wherein the interface device is configured to perform Error Check and Correction (ECC) during data communication between the at least one memory device and the processor module.

11. The apparatus of claim 3, wherein the second plurality of memory arrays comprises a NAND flash memory array.

12. The apparatus of claim 3, wherein the second plurality of memory arrays comprises a NOR flash memory array.

13. The apparatus of claim 5, wherein the first and second plurality of through wafer interconnects extend in a vertical direction with respect to a plane including the first memory device.

14. The apparatus of claim 3, wherein the interconnects comprises through wafer interconnects that form a data bus coupling the plurality of first and second memory arrays and the interface device.

15. A system comprising:

a processor module including a plurality of processors;

an interface device disposed on the processing module, the interface device including a plurality of routing elements and a first plurality of vias adapted to pass a plurality of interconnects;

a first memory device disposed above or below the interface device, the first memory device including a plurality of DRAM memory arrays and a second plurality of vias adapted to pass at least one of the plurality of interconnects to couple the plurality of DRAM memory arrays to the interface device;

a second memory device disposed above or below the interface device, the second memory device including a plurality of FLASH memory arrays and a third plurality of vias adapted to pass at least one of the plurality of interconnects to couple the plurality of FLASH memory arrays to the interface device; and

wherein the plurality of routing elements in interface device is configured to communicatively couple the plurality of DRAM memory arrays and the plurality of FLASH memory arrays to the plurality of processors using the plurality of routing elements.

16. The system of claim 15, wherein the interface device is disposed above a circuit board within a package.

17. The system of claim 15, wherein the first and second memory device is coupled to the processor module using a portion of the plurality of interconnects.

18. The system of claim 15, wherein the pluralities of routing elements are coupled to the plurality of processors using the plurality of interconnects.

19. The system of claim 15, wherein the pluralities of routing elements are coupled to the plurality of processors using connection pins.

20. The system of claim 15, wherein the processor module comprises a substrate with embedded processors.

21. The system of claim 15, wherein the processor module comprises an ASIC.

22. The system of claim 15, wherein the processor module includes a single-core processor.

23. The system of claim 15, wherein the processor module includes a multi-core processor.

24. A method comprising:

receiving data from a processor module at an interface device disposed above or below the processor module;

routing the received data to a plurality of memory arrays within at least one memory device disposed above or below the interface device using a plurality of routing elements in the interface device and a plurality of interconnects provided in vias of the interface device and/or at least one memory device;

retrieving data from a plurality of memory arrays of at least one memory device using interconnects provided in vias of the interface device and/or the at least one memory device, the interface device being disposed above or below and being coupled to the at least one memory device; and

routing retrieved data to the processor module using the plurality of routing elements and the interconnects.

25. An apparatus comprising:

an interface device coupled to a processor module including a plurality of processors, the interface device including a plurality of routing elements and the interface device configured to send and receive packet data to and from at least one of the plurality of processors;

at least one memory device including a plurality of memory arrays coupled to the interface device using a plurality of interconnects provided in vias in at least one of the interface device and the memory device, the memory device configured to send and receive data to and from the interface device; and

wherein the interface device is configured to communicatively couple the plurality of memory arrays to the plurality of processors using the plurality of routing elements based on commands stored in the packet data.

26. A method comprising:

receiving packet data from a processor module at an interface device in an electronic package;

routing the received packet data using a plurality of routing elements in the interface device based on the address provided within the packet data;

retrieving stored data from a plurality of memory arrays of at least one memory device based on memory commands provided within the packet data; and

routing retrieved stored data to the processor module using the plurality of routing elements.

Claims:

1. An apparatus comprising:

an interface chip disposed on a processor integrated circuit (IC), the interface chip including a plurality of routing elements;

at least one memory die disposed on the interface chip and including a first plurality of memory arrays, the first plurality of memory arrays coupled to the interface device using a first plurality of interconnects provided in vias in at least one of the interface chip or the at least one memory die,

wherein each via includes an opening, the opening configured to allow an interconnect of the first plurality of interconnects to partially or completely pass through at least one of the interface chip or the at least one memory die; and

wherein the interface chip is configured to communicatively couple the first plurality of memory arrays to the processor IC using the plurality of routing elements and the interconnects.

2. The apparatus of claim 1, wherein the interface chip is configured to provide memory commands to the at least one memory die.

3. The apparatus of claim 1, further comprising a second memory die including a second plurality of memory arrays.

4. The apparatus of claim 3, wherein the interface chip is configured to perform Error Check and Correction (ECC) during data communication between the at least one memory die and the processor IC.

5. The apparatus of claim 3, wherein the second plurality of memory arrays comprises a NAND flash memory array.

6. The apparatus of claim 3, wherein the second plurality of memory arrays comprises a NOR flash memory array.

7. The apparatus of claim 3, wherein the interconnects comprise through wafer interconnects that form a data bus coupling the plurality of first and second plurality of memory arrays and the interface device.

8. The apparatus of claim 3, wherein the at least one memory die further comprises a second plurality of interconnects provided in vias to couple the second plurality of memory arrays to the plurality of routing elements in the interface device.

9. The apparatus of claim 8, wherein the interface device includes circuitry configured to perform sequencing of at least one DRAM array.

10. The apparatus of claim 9, wherein the first and second plurality of interconnects extend in a vertical direction that is substantially perpendicular to a plane including the at least one memory die.

11. The apparatus of claim 1, wherein the interface chip is configured to perform power management of the apparatus, and wherein the interface chip is configured to operate at a voltage sufficient to preclude error bit generation.

12. The apparatus of claim 1, wherein the interface chip further comprises an input/output driver circuit.

13. The apparatus of claim 1, wherein the interface chip is configured to implement a refresh scheme to control error rates based on a type of array used in the at least one memory die.

14. The apparatus of claim 1, wherein the interface chip is configured to implement a refresh scheme to control error rates based on signal characteristics of the at least one memory die.

15. A system comprising:

a processor module including a plurality of processors;

an interface chip disposed on the processing module, the interface chip including a plurality of routing elements and a first plurality of vias adapted to pass a plurality of interconnects, wherein a via of the first plurality of vias includes an opening configured to allow a first interconnect of the plurality of interconnects to partially or completely pass through the interface chip;

a first memory device disposed above or below the interface chip, the first memory device including a plurality of DRAM memory arrays and a second plurality of vias adapted to pass at least one of the plurality of interconnects to couple the plurality of DRAM memory arrays to the interface chip, wherein a via of the second plurality of vias includes an opening configured to allow a second interconnect of the plurality of interconnects to partially or completely pass through the first memory device;

a second memory device disposed above or below the interface device, the second memory device including a plurality of FLASH memory arrays and a third plurality of vias adapted to pass at least one of the plurality of interconnects to couple the plurality of FLASH memory arrays to the interface chip, wherein a via of the third plurality of vias includes an opening configured to allow a third interconnect of the plurality of interconnects to partially or completely pass through the second memory device; and

wherein the plurality of routing elements in the interface chip is configured to communicatively couple the plurality of DRAM memory arrays and the plurality of FLASH memory arrays to the plurality of processors.

16. The system of claim 15, wherein the interface chip is disposed above a circuit board within a package.

17. The system of claim 15, wherein the first and second memory device are coupled to the processor module using a portion of the plurality of interconnects.

18. The system of claim 15, wherein the plurality of routing elements are coupled to the plurality of processors using the plurality of interconnects.

19. The system of claim 15, wherein the plurality of routing elements are coupled to the plurality of processors using connection pins.

20. The system of claim 15, wherein the processor module comprises a substrate with embedded processors.

21. The system of claim 15, wherein the processor module comprises an ASIC.

22. The system of claim 15, wherein the processor module includes a single-core processor.

23. The system of claim 15, wherein the processor module includes a multi-core processor.

24. A method comprising:

receiving data to provide received data from a processor integrated circuit (IC) at an interface chip disposed above or below the processor IC module;

routing the received data to a plurality of memory arrays within at least one memory die disposed above or below the interface chip using a plurality of routing elements in the interface chip and a plurality of interconnects extending through openings in the interface chip and/or the at least one memory die;

retrieving data to provide retrieved data from the plurality of memory arrays using the interconnects, the interface chip being disposed above or below and being coupled to the at least one memory die; and

routing the retrieved data to the processor module using the plurality of routing elements and the plurality of interconnects.

25. An apparatus comprising:

an interface device coupled to a processor module including a plurality of processors, the interface device including a plurality of routing elements and the interface device configured to send and receive packet data to and from at least one of the plurality of processors;

at least one memory device including a plurality of memory arrays coupled to the interface device using a plurality of interconnects extending through openings in at least one of the interface device or the memory device, the memory device configured to send and receive data to and from the interface device; and

wherein the interface device is configured to communicatively couple the plurality of memory arrays to the plurality of processors using the plurality of routing elements based on commands stored in the packet data.

26. A method comprising:

receiving packet data to provide received packet data from a processor module at an interface device in an electronic package;

routing the received packet data based on an address provided within the packet data using a plurality of routing elements in the interface device and a plurality of interconnects extending through openings in the interface device;

retrieving stored data to provide retrieved stored data from a plurality of memory arrays of at least one memory device based on memory commands provided within the packet data; and

routing the retrieved stored data to the processor module using the plurality of routing elements.