

ABSTRACT

A memory device includes a first memory area including a first memory cell array having a plurality of first memory cells each for storing N-bit data, where N is a natural number, and a second memory area including a second memory cell array having a plurality of second
5 memory cells each for storing M-bit data, where M is a natural number greater than N, the first memory area and the second memory area are included in a single semiconductor chip and share an input and output interface, and a controller configured to generate calculation data by applying a weight stored in the first memory area to sensing data in response to receiving the sensing data obtained by an external sensor, and store the calculation data in
10 one of the first memory area or the second memory area according to the weight.

FIG. 5