

Description

The present invention relates generally to gating pulse generators for use in television receivers, and particularly to line-rate gating pulse generators subject to periodic field-rate disabling.

In co-filed EP-A-145490 corresponding to US Patent Application Serial No. 561,280 of R. Shanley et al, entitled "Keyed DC Stabilization System With Protection From Error Introduction During Vertical Sync Interval", stabilizing the DC levels of the respective color signals in a color television receiver is disclosed. This system employs a plurality of DC control loops using keyed voltage comparators. In the Shanley, et al. system, the comparator keying is effected in response to recurring line-rate gating pulses. These gating pulses are timed to coincide with backporch segments of successive horizontal blanking intervals of the received signals during active scan time. To avoid error introduction during the vertical sync intervals of the received signals (when such timing of the recurring pulses will result in coincidence with exhibitions of sync peak level, rather than blanking level, by the received signal), the Shanley, et al. arrangement seeks to bar comparator keying during all, or a significant portion of, each vertical sync interval.

The present invention is directed to a line-rate gating pulse generator which is subject to periodic field-rate disabling in such a manner as to interrupt gating pulse appearances throughout a selected portion of each field interval of the received signals, and which may be used, for example, to achieve the keying preclusion sought by Shanley, et al. above.

According to the invention, there is provided a television receiver comprising a line-rate gating pulse generator subject to periodic field-rate disabling including: a source of periodic line-rate timing pulses; a source of periodic field-rate pulses; and a source of DC potential; said generator being characterized by: means, responsive to said line-rate timing pulses, for developing gating pulses with leading edges normally determined by the leading edges of said timing pulses; and a gating pulse width control circuit for controlling the widths of the said gating pulses the control circuit being subject to keying by said field-rate pulses and including a first resistor, a capacitor, and a second resistor serially connected across said DC potential source; said gating pulse width control circuit operating in a first mode during periods intervening between successive field-rate pulse appearances, in which first mode said second resistor is effectively bypassed and the RC time constant of said first resistor and said capacitor is determinative of a substantially fixed, finite width for said gating pulses; and said gating pulse width control circuit

operating in a second mode during appearances of said field-rate pulses, in which second mode said second resistor is not bypassed and the width of said gating pulses is reduced to zero so as to effect a desired field-rate suppression of gating pulse appearances.

In accordance with an illustrative embodiment of the present invention, a gating pulse generator includes an output load across which the generator develops said gating pulse, and first and second transistors having normally conducting emitter-collector paths, with the emitter-collector path of the first transistor serially coupled with the output load. Timing pulses recurring at a line rate suppress conduction in the emitter-collector paths of the first and second transistors during each timing pulse appearance. A first resistor, a capacitor, and a second resistor are connected in series across a DC potential supply, with the emitter-collector path of the second transistor shunted across the series combination of the capacitor and the second resistor. A third transistor, responsive to field-rate pulses indicative of the timing of recurring vertical sync intervals, has an emitter-collector path rendered non-conductive during each field-rate pulse appearance. The series combination of a diode and the emitter-collector path of the third transistor is connected in shunt with the second resistor, with the diode poled to exhibit a conductive state when cutoff of the second transistor coincides with the third transistor's conduction. A fourth transistor, with its emitter-collector path shunting the first transistor's emitter-collector path, is rendered conducting when the voltage across the series combination of the capacitor and the second resistor exceeds a reference level.

In operation of the above-described embodiment, during each field-rate pulse appearance, each initiation of cut off of said second transistor is accompanied by a step rise of the voltage across the series combination of the capacitor and the second resistor. The resistance value of the second resistor is desirably selected such that the magnitude of said step rise exceeds the magnitude of said reference level. The charging time constant of a charging circuit formed by the first resistor, the capacitor, the diode in its conductive state, and the emitter-collector path of the third transistor in its conductive state, is determinative of the gating pulse width in the periods intervening between successive field-rate pulses.

In the accompanying drawing, the sole figure illustrates, partially schematically and partially by block representation, a portion of a television receiver including a line-rate gating pulse generator subject to field-rate disabling in accordance with an illustrative embodiment of the present invention.

In the illustrated receiver portion, a sync sepa-

rator 10, functioning to separate deflection synchronizing pulses from the image-representative components of received video signals, develops a composite sync waveform at its output terminal CS. The composite sync signals appearing at terminal CS are commonly supplied to an integrating circuit 20 and to a differentiating circuit 30. The integrating circuit 20 comprises a resistor 21 serially disposed between separator output terminal CS and the integrating circuit output terminal IS, and a shunt capacitor 22 connected between terminal IS and a reference potential point (ground). The differentiating circuit 30 comprises a capacitor 31 serially disposed between separator output terminal CS and the differentiating circuit output terminal DS, and a shunt resistor 32 connected between terminal DS and ground.

The integrated version of the composite sync signal which is developed at terminal IS is supplied to a vertical drive pulse generator 24 to synchronize the development of a train of vertical drive pulses at the generator output terminal DP. The pulse train at terminal DP is applied to the base electrode of an NPN amplifier transistor 25, disposed with its emitter electrode grounded and with its collector electrode connected via a resistor 26 to the positive terminal ($+V_{cc}$) of an operating potential supply. Illustratively, the vertical drive pulses at terminal DP comprise negative-going pulses of an eight-line duration, with a leading edge coincident with, or slightly delayed with respect to, the beginning of the received signal's vertical sync interval. Amplified vertical drive pulses appear at terminal VD (directly connected to the collector electrode of transistor 25) and are supplied to the receiver's vertical deflection circuits 27 to control the development of field-rate deflection waves.

The differentiated version of the composite sync signal which appears at terminal DS is coupled via a resistor 33 to the base electrode of an NPN transistor 35, and to the receiver's horizontal deflection circuits 34 to synchronize the development of line rate deflection waves. The deflection circuits 34 include a synchronized horizontal oscillator from which a sawtooth voltage wave is derived for delivery to an output terminal ST. Also available from the horizontal deflection circuits 34 are periodically recurring horizontal flyback pulses, appearing at output terminal FB.

The emitter electrode of transistor 35 is grounded, while the collector electrode thereof is connected via a resistor 36 to the $+V_{cc}$ supply terminal. The collector electrode of transistor 35 is also directly connected to the base electrode of a PNP emitter-follower transistor 37. Transistor 37 is disposed with its collector electrode grounded, and with its emitter electrode directly connected to a first input terminal (N) of a non-additive mixer 40.

The non-additive mixer 40 comprises a pair of PNP transistors 41 and 42, disposed with joined collector electrodes directly connected to ground, and with joined emitter electrodes connected to the $+V_{cc}$ supply terminal via an emitter resistor 43. The base electrode of transistor 41 is directly connected to the aforementioned first mixer input terminal N, while the base electrode of transistor 42 is directly connected to a second mixer input terminal N'.

Mixer input terminal N is additionally connected via a resistor 46 to the emitter electrode of an NPN transistor 44 disposed as an emitter-follower, with its collector electrode directly connected to the $+V_{cc}$ supply terminal, and with its emitter electrode returned to ground via resistor 45. The base electrode of the emitter-follower transistor 44 is directly connected to terminal VR, to which a positive DC potential of a selected level is supplied.

Mixer input terminal N' is directly connected to the emitter electrode of an NPN transistor 47 disposed as an emitter-follower, with its collector electrode directly connected to the $+V_{cc}$ supply terminal, and with its emitter electrode returned to ground via resistor 48. The base electrode of the emitter-follower transistor 47 is connected to terminal FB, at which appear horizontal flyback pulses developed by the horizontal deflection circuits 34.

The output of the non-additive mixer 40, which is developed at the joined emitter electrodes of transistors 41 and 42, is supplied to a voltage comparator 50 for comparison with sawtooth voltage waves supplied from terminal ST of the horizontal deflection circuits 34.

The output of voltage comparator 50, comprising negative-going, line-rate timing pulses developed when the comparator input from mixer 40 is more positive than the comparator input from terminal ST, appears at a timing pulse output terminal TP, which is directly connected to the base electrodes of a pair of NPN transistors 51 and 61. The emitter electrodes of transistors 51 and 61 are both directly connected to ground. The collector electrode of transistor 51 is directly connected to terminal BG, linked by a resistor 52 to the $+V_{cc}$ supply terminal. Terminal BG constitutes the output terminal of the illustrated gating pulse generating apparatus.

Resistor 62, capacitor 63, and resistor 64 are connected in series, in the order named, between the $+V_{cc}$ supply terminal and ground. Terminal PW, at the junction of resistor 62 and capacitor 63, is directly connected to the collector electrode of the aforementioned transistor 61, the connection placing the emitter-collector path of transistor 61 in shunt with the series combination of capacitor 63 and resistor 64. A diode 65 is disposed with its anode connected to the junction of capacitor 63

and resistor 64, and with its cathode connected to terminal VD, with the consequence that the series combination of diode 65 and the emitter-collector path of transistor 25 is connected in shunt with resistor 64.

A voltage comparator 70, comprising a pair of PNP transistors 71, 72 with joined emitter electrodes, receives a first input via the direct connection of terminal PW to the base electrode of comparator transistor 72. The second input to comparator 70 is derived from a voltage divider formed by resistors 74 and 75, serially disposed between the $+V_{cc}$ supply terminal and ground. The divider output, appearing at the junction of resistors 74 and 75, is directly applied to the base electrode of comparator transistor 71. A current source for the comparator transistors 71, 72 is formed by PNP transistor 73, disposed with its collector electrode directly connected to the joined emitter electrodes of transistors 71 and 72, with its emitter electrode returned to the $+V_{cc}$ supply terminal via an emitter resistor 73R, and with its base electrode connected to a bias supply terminal V_B .

The collector electrode of comparator transistor 72 is directly connected to the joined base and collector electrodes of a diode-connected NPN transistor 76, disposed with its emitter electrode grounded. The base electrode of transistor 76 is directly connected to the base electrode of NPN transistor 77. Transistor 77 is disposed with its collector electrode directly connected to the collector electrode of comparator transistor 71, and with its base-emitter path shunting the base-emitter path of the diode-connected transistor 76. The collector electrode of comparator transistor 71 is also directly connected to the base electrode of an NPN transistor 78. Transistor 78 is disposed with its emitter electrode grounded and with its collector electrode directly connected to the gating pulse output terminal BG, with the consequence that the emitter-collector path of transistor 78 is connected in shunt with the emitter-collector path of the previously mentioned transistor 51.

In operation of the above-described gating pulse generating apparatus, during the periods intervening between the successive line-rate timing pulse appearances at terminal TP, transistors 51 and 61 are strongly conducting, holding terminal PW and output terminal BG at a low potential. The leading edge of each negative-going timing pulse initiates cutoff of transistors 51 and 61. The resultant effect on the voltage at output terminal BG depends upon the conduction condition of the vertical drive pulse amplifying transistor 25. That is, as explained below, the output potential behavior at terminal BG during vertical drive pulse appearances at terminal DP (when transistor 25 is cut off) will differ from that occurring during periods inter-

vening between successive vertical drive pulse appearances (when transistor 25 is strongly conducting).

Considering first the conditions prevailing during the periods intervening between successive vertical drive pulse appearances, the cutoff of transistor 61 releases terminal PW for voltage excursions thereat, and permits formation of a capacitor charging circuit comprising, in series, resistor 62, capacitor 63, diode 65 in its conductive state, and the collector-emitter path of the conducting transistor 25. Resistor 64 is effectively bypassed by a low impedance path formed by conducting diode 65 and the collector-emitter path of conducting transistor 25. While an initial step rise of the voltage at terminal PW (of a magnitude equal to the voltage drop across conducting diode 65) accompanies the release of terminal PW, this rise is not of sufficient magnitude to elevate the potential at the base of comparator transistor 72 to the level of the reference voltage supplied to the base of comparator transistor 71 from voltage divider 74/75, wherefore comparator 70 remains in an operating state (inclusive of cutoff of comparator transistor 71) which holds transistor 78 in a cutoff condition. In the absence of conduction by transistor 78, the cutoff of transistor 51 allows output terminal BG to rise in potential to form the leading edge of an output gating pulse of positive-going form.

Terminal BG remains at a high positive potential until an exponential rise of the potential at terminal PW (due to the charging of capacitor 63) reaches a reference level permitting a turn-on of comparator transistor 71 and a consequent initiation of conduction by transistor 78. Conduction by transistor 78 returns terminal BG to a low potential to define the trailing edge of the output gating pulse. Subsequently, when the negative-going timing pulse at terminal TP terminates, transistors 51 and 61 return to a conducting state, and terminal PW swings low, returning comparator 70 to its normal operating state and cutting off transistor 78. The cutoff of transistor 78 does not affect the potential at output terminal BG, since the resumed conduction by transistor 51 continues to hold terminal BG at a low potential. It will be appreciated that the time constant of the capacitor charging circuit is determinative of the output gating pulse width under the above-described operating conditions, with variations of the timing pulse width not disturbing a desired constancy of the output gating pulse width.

Considering now the conditions prevailing during vertical drive pulse appearances, whenever cutoff of transistor 61 releases terminal PW from a clamped condition, conduction by diode 65 does not result since the diode cathode is at an elevated potential due to the cutoff of the vertical drive pulse

amplifying transistor 25. Resistor 64 is thus not bypassed, and an initial step rise of the voltage at terminal PW of a magnitude determined by the resistance value of resistor 64 now accompanies the release of terminal PW. By suitable choice of this resistance value, the magnitude of this step rise will exceed the aforementioned reference level, wherefore a change in operating state of comparator 70 and a turn-on of transistor 78 are initiated by the leading edge of the timing pulse at terminal TP. A rise in potential at terminal BG in response to a timing pulse appearance at terminal TP is thus prevented throughout each vertical drive pulse appearance, since each cutoff of transistor 51 is accompanied by a simultaneous turn-on of transistor 78. The desired field-rate blanking of line-rate gating pulses is thus readily achieved.

As described above, elements 62,63,64,65 and 25 cooperate to form a keyed pulse width control circuit, which in one mode of operation, determines a finite gating pulse width in accordance with an RC time constant, and which, in a second mode of operation, establishes a zero pulse width to effect a selective suppression of output gating pulses.

It may be noted that addition of the field-rate blanking feature to a line-rate gating pulse generator of the type disclosed in copending US-A-4581630 requires the addition of only two circuit elements: resistor 64, and diode 65.

In the Fernsler et al. application, a capacitor charging circuit enabled at the initiation of gating pulse generation, controls the timing of the termination of gating pulse generation, ensuring constancy of gating pulse width. The modification of the capacitor charging circuit of the Fernsler, et al. arrangement to a field-rate keyed form enables the gating pulse width to be effectively reduced to zero during the period when gating pulse interruption is desired.

The particular mode of timing pulse generation employed in the illustrated embodiment is the same as that disclosed in the aforementioned Fernsler et al. US Patent application. Reference may be made to that patent application for a detailed explanation of the operation of the timing pulse generating apparatus (35, 37, 40, 44, 47, 50, etc.), a description of said operation being briefly summarized below.)

Non-additive mixer 40 provides an output which follows the least positive of its respective inputs. One input comprises positive-going horizontal flyback pulses from terminal FB of deflection circuits 34, while the other input normally corresponds to a reference DC voltage (equal to the voltage at terminal VR less the base-emitter offset potential, V_{be} , of transistor 44), but is periodically depressed therefrom during each horizontal sync interval as it follows an inverted version of the

output of differentiating circuit 30. The waveform of the mixer 40 output comprises a clipped, positive-going flyback pulse with a central (negative-going) notch. The output of voltage comparator 50 (at terminal TP) is normally high, but swings low when the input from mixer 40 swings above a declining return stroke of the sawtooth voltage wave input from terminal ST. This change in the operating state of comparator 50 is normally initiated at a point in the rise of the trailing edge of the central notch of the mixer's output waveform.

With the timing of the notch's trailing edge coinciding with trailing edges of the received signal's horizontal sync pulses, the resultant timing pulses at terminal TP have the desired "backporch" location. The output of comparator 50 remains low until a decline of the clipped flyback pulse component returns comparator 50 to its original operating state, terminating the timing pulse.

It should be appreciated that, while the above-described technique provides an advantageous approach to the generation of the timing pulses at terminal TP, the principles of the present invention are readily applicable to use with other forms of timing pulse generation.

While in some possible applications of the present invention, the output of gating pulse generator of the illustrated form may be used directly for keying purposes, a particular contemplated application of the present invention is its use in the formation of a multilevel keying waveform of the so-called "sandcastle" type (for application to an input terminal of an integrated circuit, bearing, inter alia, a sandcastle decoder from which a plurality of different keying waves may be derived). Reference may be made to the coiled European Patent Application EP-A-145490 corresponding to the aforementioned US Patent Application Serial No. 561,280 of R. Shanley et al., for an example of a trilevel sandcastle pulse encoding/decoding system in which a gating pulse generator of the herein described type may be used to advantage.

Claims

1. A television receiver comprising a line-rate gating pulse generator subject to periodic field-rate disabling including:
 - a source (50) of periodic line-rate timing pulses (TP);
 - a source (24) of periodic field-rate pulses (DP); and
 - a source (+VCC) of DC potential; said generator being characterized by:
 - means (51,52,78), responsive to said line-rate timing pulses, for developing gating

amplifying transistor 25. Resistor 64 is thus not bypassed, and an initial step rise of the voltage at terminal PW of a magnitude determined by the resistance value of resistor 64 now accompanies the release of terminal PW. By suitable choice of this resistance value, the magnitude of this step rise will exceed the aforementioned reference level, wherefore a change in operating state of comparator 70 and a turn-on of transistor 78 are initiated by the leading edge of the timing pulse at terminal TP. A rise in potential at terminal BG in response to a timing pulse appearance at terminal TP is thus prevented throughout each vertical drive pulse appearance, since each cutoff of transistor 51 is accompanied by a simultaneous turn-on of transistor 78. The desired field-rate blanking of line-rate gating pulses is thus readily achieved.

As described above, elements 62,63,64,65 and 25 cooperate to form a keyed pulse width control circuit, which in one mode of operation, determines a finite gating pulse width in accordance with an RC time constant, and which, in a second mode of operation, establishes a zero pulse width to effect a selective suppression of output gating pulses.

It may be noted that addition of the field-rate blanking feature to a line-rate gating pulse generator of the type disclosed in copending US-A-4581630 requires the addition of only two circuit elements: resistor 64, and diode 65.

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With the timing of the notch's trailing edge coinciding with trailing edges of the received signal's horizontal sync pulses, the resultant timing pulses at terminal TP have the desired "backporch" location. The output of comparator 50 remains low until a decline of the clipped flyback pulse component returns comparator 50 to its original operating state, terminating the timing pulse.

It should be appreciated that, while the above-described technique provides an advantageous approach to the generation of the timing pulses at terminal TP, the principles of the present invention are readily applicable to use with other forms of timing pulse generation.

While in some possible applications of the present invention, the output of gating pulse generator of the illustrated form may be used directly for keying purposes, a particular contemplated application of the present invention is its use in the formation of a multilevel keying waveform of the so-called "sandcastle" type (for application to an input terminal of an integrated circuit, bearing, inter alia, a sandcastle decoder from which a plurality of different keying waves may be derived). Reference may be made to the coiled European Patent Application EP-A-145490 corresponding to the aforementioned US Patent Application Serial No. 561,280 of R. Shanley et al., for an example of a trilevel sandcastle pulse encoding/decoding system in which a gating pulse generator of the herein described type may be used to advantage.

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 - a source (50) of periodic line-rate timing pulses (TP);
 - a source (24) of periodic field-rate pulses (DP); and
 - a source (+VCC) of DC potential; said generator being characterized by:
 - means (51,52,78), responsive to said line-rate timing pulses, for developing gating



pulses (BG) with leading edges normally determined by the leading edges of said timing pulses (TP); and

a gating pulse width control circuit (25,62,63,64, 65,70,74,75) for controlling the widths of the said gating pulses (BG) the control circuit being subject to keying by said field-rate pulses and including a first resistor (62), a capacitor (63), and a second resistor (64) serially connected across said DC potential source; said gating pulse width control circuit (25,62,63,64,65,70) operating in a first mode during periods intervening between successive field-rate pulse appearances, in which first mode said second resistor (64) is effectively bypassed and the RC time constant of said first resistor and said capacitor is determinative of a substantially fixed, finite width for said gating pulses (BG); and said gating pulse width control circuit (25,62,63,64,65,70,74,75) operating in a second mode during appearances of said field-rate pulses, in which second mode said second resistor is not bypassed and the width of said gating pulses (BG) is reduced to zero so as to effect a desired field-rate suppression of gating pulse appearances.

2. A receiver as claimed in Claim 1, wherein said gating pulse developing means (51,52,78) includes:

an output load (52) across which said gating pulses (BG) are developed;

a first (51) transistor having a base coupled to the source (50) of timing pulses and having a normally conducting emitter-collector path, the emitter-collector path of said first transistor (51) being serially coupled with said output load, the emitter-collector path of said first transistor being non-conductive during each timing pulse appearance; and

a second transistor (78) having a normally non-conductive emitter-collector path connected in shunt with the emitter-collector path of said first transistor (51).

3. A receiver as claimed in Claim 2, wherein the gating pulse width control circuit comprises:-

an additional transistor (61) having a normally conducting emitter-collector path in shunt with the series combination of the capacitor (63) and second resistor (64), and a base coupled to the source (50) of timing pulses, the emitter-collector path of said additional transistor (61) being non-conductive during each timing pulse appearance;

means (70) for rendering the emitter-collector path of the second transistor (78) con-

ductive when the voltage across the series combination of the capacitor (63) and second resistor (64) exceeds a reference level ($+V_{cc}$, 74,75); and

a diode (65) connected to the junction of the capacitor (63) and second resistor (64), the diode being rendered non-conductive upon each appearance of a field rate pulse.

4. A receiver in accordance with Claim 3, including a further transistor (25) having an emitter-collector path which is non-conductive during said field-rate pulse appearances, the series combination of the emitter-collector path of said further transistor (25) and said diode (65) being connected in shunt with said second resistor.

5. A receiver in accordance with Claim 4, wherein during each field-rate pulse appearance, each initiation of a cutoff of said additional transistor (61) is accompanied by a step rise of the voltage across said series combination of said capacitor (63) and said second (64) resistor; the resistance value of said second resistor (64) being such as to ensure that the magnitude of said step rise exceeds the magnitude of said reference level.

6. A receiver in accordance with Claim 4 or 5, wherein the charging time constant of a charging circuit formed by the series combination of said first resistor (62), said capacitor (63), said diode (65) in its conductive state, and the emitter-collector path of said further transistor (25) in its conductive state is determinative of the width of the gating pulses appearing during said intervening periods.

7. A receiver in accordance with any one of Claims 4 to 6 wherein said television receiver receives composite video signals inclusive of respective line and field deflection synchronizing components, said field deflection synchronizing components occupying periodically recurring vertical sync intervals;

said periodic field-rate pulses being indicative of the timing of said recurring vertical sync intervals; and

said source of timing pulses (50) is responsive to said line deflection synchronization component of said composite video signals.

8. A receiver in accordance with Claim 7, wherein said field-rate pulses comprise vertical drive pulses generated in response to said field deflection synchronization component of said composite video signals.



Revendications

1. Récepteur de télévision comprenant un générateur d'impulsions de déclenchement à la fréquence horizontale soumis à une inhibition périodique à la fréquence verticale, comprenant :
 - une source (50) d'impulsions périodiques de temporisation à la fréquence horizontale (TP) ;
 - une source (24) d'impulsions périodiques à la fréquence verticale (DP) ; et
 - une source (+VCC) de courant continu, ledit générateur étant caractérisé par :
 - un moyen (51, 52, 78) répondant auxdites impulsions de temporisation à la fréquence horizontale pour développer des impulsions de déclenchement (BG) dont les flancs menants sont normalement déterminés par les flancs menants desdites impulsions de temporisation (TP) ; et
 - un circuit de contrôle de la largeur des impulsions de déclenchement (25, 62, 63, 64, 65, 70, 74, 75) pour contrôler les largeurs desdites impulsions de déclenchement (BG), le circuit de contrôle étant soumis à une manipulation par lesdites impulsions à la fréquence verticale et comprenant une première résistance (62), un condensateur (63) et une seconde résistance (64) liés en série aux bornes de ladite source de courant continu ; ledit circuit de contrôle de la largeur des impulsions de déclenchement (25, 62, 63, 64, 65, 70) opérant dans un premier mode pendant les périodes entre les apparitions successives des impulsions à la fréquence verticale, premier mode dans lequel ladite seconde résistance (64) est efficacement by-passée et la constante de temps RC de ladite première résistance et dudit condensateur détermine une largeur sensiblement fixe définie desdites impulsions de déclenchement (BG) ; et ledit circuit de contrôle de la largeur des impulsions de déclenchement (25, 62, 63, 64, 65, 70, 74, 75) opérant dans un second mode pendant les apparitions desdites impulsions à la fréquence verticale, second mode dans lequel ladite seconde résistance n'est pas by-passée et la largeur desdites impulsions de déclenchement (BG) est réduite à zéro afin d'effectuer une suppression souhaitée à la fréquence verticale des apparitions des impulsions de déclenchement.
2. Récepteur selon la revendication 1, où ledit moyen développant des impulsions de déclenchement (51, 52, 78) comprend :
 - une charge de sortie (52) à travers laquelle sont développées lesdites impulsions de déclenchement (BG) ;

un premier transistor (51) ayant une base couplée à la source (50) d'impulsions de temporisation et ayant un trajet émetteur-collecteur normalement conducteur, le trajet émetteur-collecteur dudit premier transistor (51) étant couplé en série à ladite charge de sortie, le trajet émetteur-collecteur dudit premier transistor étant non conducteur pendant chaque apparition d'une impulsion de temporisation ; et

un second transistor (78) ayant un trajet émetteur-collecteur normalement non conducteur connecté en shunt avec le trajet émetteur-collecteur dudit premier transistor (51).

3. Récepteur selon la revendication 2, où le circuit de contrôle de la largeur des impulsions de déclenchement comprend :

un transistor additionnel (61) ayant un trajet émetteur-collecteur normalement conducteur en shunt avec la combinaison en série du condensateur (63) et de la seconde résistance (64) et une base couplée à la source (50) d'impulsions de temporisation, le trajet émetteur-collecteur dudit transistor additionnel (61) étant non conducteur pendant chaque apparition d'une impulsion de temporisation ;

Un moyen (70) pour rendre le trajet émetteur-collecteur du second transistor (78) conducteur quand la tension dans la combinaison en série du condensateur (63) et de la seconde résistance (64) dépasse un niveau de référence (+Vcc, 74, 75) ; et

une diode (65) connectée à la jonction du condensateur (63) et de la seconde résistance (64), la diode étant rendue non conductrice lors de chaque apparition d'une impulsion à la fréquence verticale.

4. Récepteur selon la revendication 1, comprenant un autre transistor (25) ayant un trajet émetteur-collecteur qui est non conducteur pendant lesdites apparitions d'impulsions à la fréquence verticale, la combinaison en série du trajet émetteur-collecteur dudit autre transistor (25) et de ladite diode (65) étant connectée en shunt avec ladite seconde résistance.

5. Récepteur selon la revendication 4, où, pendant chaque apparition d'une impulsion à la fréquence verticale, chaque amorce d'une coupure dudit transistor additionnel (61) est accompagnée d'une augmentation échelonnée de la tension dans la combinaison en série dudit condensateur (63) et de ladite seconde résistance (64) ; la valeur de ladite seconde résistance (64) étant telle que cela assure que la grandeur de ladite augmentation échelonnée dépassera la grandeur dudit niveau de référen-



ce.

6. Récepteur selon la revendication 4 ou 5, où la constante de temps de charge d'un circuit de charge formé de la combinaison en série de ladite première résistance (62), du condensateur (63), de ladite diode (65) à son état conducteur et du trajet émetteur-collecteur dudit autre transistor (25) à son état conducteur détermine la largeur des impulsions de déclenchement apparaissant pendant lesdites périodes intermédiaires.
7. Récepteur selon l'une quelconque des revendications 4 à 6, où ledit récepteur de télévision reçoit des signaux vidéo composites comprenant toutes les composantes de synchronisation de déviation horizontale et verticale respectives, lesdites composantes de synchronisation de déviation verticale occupant des intervalles périodiquement récurrents de synchronisation verticale ; et
lesdites impulsions périodiques à la fréquence verticale indiquant la temporisation desdits intervalles récurrents de synchronisation verticale ; et
ladite source d'impulsions de temporisation (50) répond à ladite composante de synchronisation de déviation horizontale desdits signaux vidéo composites.
8. Récepteur selon la revendication 7, où lesdites impulsions à la fréquence verticale comprennent des impulsions d'attaque verticale produites en réponse à ladite composante de synchronisation de déviation verticale desdits signaux vidéo composites.

Ansprüche

1. Fernsehempfänger mit einem Generator für zeilenfrequente Tastimpulse, der periodisch teilbildfrequent sperrbar ist, mit
einer Quelle (50) für periodische zeilenfrequente Zeitsteuerpulse (TP);
einer Quelle (24) für periodische teilbildfrequente Pulse (DP); und
einer Quelle (+ VCC) für ein Gleichpotential; dadurch gekennzeichnet, daß der genannte Generator gekennzeichnet ist durch
eine auf die zeilenfrequenten Zeitsteuerpulse ansprechende Anordnung (51, 52, 78) zur Erzeugung von Tastpuls (GB) deren Vorderflanken gewöhnlich durch die Vorderflanken der Zeitsteuerpulse (TP) bestimmt werden; und
eine Tastpulsbreiten-Steuerschaltung (25, 62, 63, 64, 65, 70, 74, 75) zum Steuern der

Breiten der Tastpulse (BG), wobei die Steuerschaltung durch die teilbildfrequenten Pulse tastbar ist und einen ersten Widerstand (62), einen Kondensator (63) und einen zweiten Widerstand (64), die in Reihe miteinander an die Gleichpotentialquelle angeschlossen sind, enthält; wobei ferner die Tastpulsbreiten-Steuerschaltung (25, 62, 63, 64, 65, 70) während Perioden, die zwischen dem Auftreten aufeinanderfolgender teilbildfrequenter Pulse liegen, in einem ersten Betriebszustand arbeitet, in dem der zweite Widerstand (64) effektiv überbrückt ist und die RC-Zeitkonstante des ersten Widerstandes und des Kondensators eine im wesentlichen feste, begrenzte Breite für die Tastpulse (GB) bestimmt; und die Tastpulsbreiten-Steuerschaltung (25, 62, 63, 64, 65, 70, 74, 75) während des Auftretens der teilbildfrequenten Pulse in einem zweiten Betriebszustand arbeitet, in dem der zweite Widerstand nicht überbrückt ist und die Breite der Tastpulse (BG) auf null reduziert ist, so daß eine gewünschte teilbildfrequente Unterdrückung des Auftretens der Tastpulse bewirkt wird.

2. Empfänger nach Anspruch 1, bei welchem die Anordnung (51, 52, 78) zum Erzeugen der Tastpulse enthält:
eine Ausgangslast (52), an der die Tastpulse (BG) erzeugt werden;
einen ersten Transistor (51), der mit seiner Basis mit der Quelle (50) für die Zeitsteuerpulse gekoppelt ist und der eine normalerweise leitende Emitter-Kollektor-Strecke aufweist, welche der Ausgangslast in Reihe geschaltet ist und während jedes Auftretens eines Zeitsteuerpulses nicht leitfähig ist; und
einen zweiten Transistor (78) mit einer normalerweise nicht leitfähigen Emitter-Kollektor-Strecke, die der Emitter-Kollektor-Strecke des ersten Transistors (51) parallelgeschaltet ist.
3. Empfänger nach Anspruch 2, bei welchem die Tastpulsbreiten-Steuerschaltung enthält:
einen zusätzlichen Transistor (61), dessen normalerweise leitende Emitter-Kollektor-Strecke der Reihenschaltung aus dem Kondensator (63) und dem zweiten Widerstand (64) parallelgeschaltet sowie während jedes Auftretens eines Zeitsteuerimpulses nichtleitfähig ist, und dessen Basis mit der Quelle (50) für die Zeitsteuerpulse gekoppelt ist;
eine Anordnung (70) zum Leitfähigmachen der Emitter-Kollektor-Strecke des zweiten Transistors (78), wenn die Spannung an der Reihenschaltung aus dem Kondensator (63) und dem zweiten Widerstand (64) einen Referenzwert erreicht;



renzwert (+ Vcc, 74, 75) überschreitet; und
eine Diode (65), die an die Verbindung des
Kondensators (63) und des zweiten Widerstan-
des (64) angeschlossen ist und bei jedem Auf-
treten eines teilbildfrequenten Pulses nichtleit-
fähig gemacht wird.

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4. Empfänger nach Anspruch 3, mit einem weite-
ren Transistor (25), dessen Emitter-Kollektor-
Strecke während des Auftretens der teilbildfre-
quenten Pulse nichtleitfähig ist, wobei die Rei-
henschaltung aus der Emitter-Kollektor-Strecke
des weiteren Transistors (25) und der Diode
(65) dem zweiten Widerstand parallelgeschaltet
ist.

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5. Empfänger nach Anspruch 4, bei welchem
während jedes Auftretens eines teilbildfrequenten
Impulses jede Einleitung einer Sperrung
des zusätzlichen Transistors (61) von einem
steilen Anstieg der Spannung an der Reihenschaltung
aus dem Kondensator (63) und dem
zweiten Widerstand (64) begleitet ist; und der
Widerstandswert des zweiten Widerstandes
(64) gewährleistet, daß die Größe des steilen
Anstieges die Größe des Referenzwertes über-
schreitet.

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6. Empfänger nach Anspruch 4 oder 5, bei wel-
chem die Ladezeitkonstante eines Ladekreises
aus der Reihenschaltung des ersten Wider-
standes (62), des Kondensators (63), der Diode
(65) in ihrem leitfähigen Zustand und der
Emitter-Kollektor-Strecke des weiteren Transi-
stors (25) in ihrem leitfähigen Zustand die
Breite der Tastimpulse bestimmt, die während
der erwähnten Zwischenperioden auftreten.

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7. Empfänger nach einem der Ansprüche 4 bis 6,
welcher ein Videosignalgemisch einschließlich
entsprechender Zeilen- und Teilbildablen-
kungssynchronisieranteile, welche periodisch
wiederkehrende Vertikalsynchronisierintervalle
einnehmen, empfängt;

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die periodischen teilbildfrequenten Pulse
die Zeit der wiederkehrenden Vertikalsynchro-
nisierintervalle angeben; und

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die Quelle (50) für die Zeitsteuerepulse auf
den Zeilenablenksynchronisieranteil des Video-
signalgemisches anspricht.

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8. Empfänger nach Anspruch 7, bei welchem die
teilbildfrequenten Pulse Vertikaltreiberpulse
enthalten, die als Reaktion auf den Teilbildab-
lenksynchronisieranteil des Videosignalgemi-
sches erzeugt werden.

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