

ABSTRACT OF THE DISCLOSURE

Provided is a bit error rate equalizing method of a memory device. The memory device selectively performs an error correction code (ECC) interleaving operation according to resistance distribution characteristics of memory cells, when writing a codeword including information data and a parity bit of the information data to a memory cell array. In the ECC interleaving operation according to one example, an ECC sector including information data is divided into a first ECC sub-sector and a second ECC sub-sector, the first ECC sub-sector is written to memory cells of a first memory area having a high bit error rate (BER), and the second ECC sub-sector is written to memory cells of a second memory area having a low BER.

FIG. 11A