

WHAT IS CLAIMED IS:

1. A three-dimensional semiconductor memory device, comprising:
 - a substrate including a cell array region and a connection region;
 - an electrode structure including a plurality of electrodes vertically stacked on the substrate, each of the electrodes having a pad portion on the connection region;
 - a plurality of electrode separation structures penetrating the electrode structure, the electrode separation structures extending in a first direction and spaced apart from each other in a second direction intersecting the first direction; and
 - a plurality of contact plugs coupled to the pad portions of the electrodes, wherein the contact plugs comprise:
 - a plurality of first contact plugs along the first direction; and
 - a plurality of second contact plugs apart in the second direction from the first contact plugs,
 - wherein the electrode separation structures comprise:
 - a first electrode separation structure between the first contact plugs and the second contact plugs;
 - a second electrode separation structure apart from the first electrode separation structure in the second direction, the first contact plugs between the first and second electrode separation structures; and
 - a third electrode separation structure apart from the first electrode separation structure in the second direction, the second contact plugs between the first and third electrode separation structures,
 - wherein the first contact plugs are apart in the second direction at a first distance from the first electrode separation structure, and apart from the second electrode separation structure at a second distance less than the first distance, and

wherein the second contact plugs are apart in the second direction from the first electrode separation structure at a third distance different from the first distance, and apart from the third electrode separation structure at a fourth distance less than the third distance.

2. The three-dimensional semiconductor memory device of claim 1, wherein each of the pad portions of the electrodes is between the electrode separation structures adjacent to each other in the second direction.

3. The three-dimensional semiconductor memory device of claim 1 or claim 2, wherein

top surfaces of the first and second contact plugs are at the same level, and
bottom surfaces of the first and second contact plugs are at different levels.

4. The three-dimensional semiconductor memory device of any one of claims 1 to 3, wherein the contact plugs further comprise a plurality of third contact plugs apart in the second direction from the second contact plugs,

wherein the second electrode separation structure is between the second contact plugs and the third contact plugs, and

wherein the third contact plugs are apart in the second direction from the second electrode separation structure at a fifth distance, different from the third distance.

5. The three-dimensional semiconductor memory device of claim 4, wherein the fifth distance is different from the first distance.

6. The three-dimensional semiconductor memory device of any one of claims 1 to 5, further comprising a plurality of dummy vertical structures on the connection region, the

dummy vertical structures penetrating corresponding pad portions of the electrodes and when viewed in plan being disposed to surrounding a corresponding one of the contact plugs,

wherein the dummy vertical structures have a major axis in a diagonal direction to the first and second directions.

7. The three-dimensional semiconductor memory device of any one of claims 1 to 5, further comprising a plurality of dummy vertical structures on the connection region, the dummy vertical structures penetrating corresponding pad portions of the electrodes and when viewed in plan being disposed to surround a corresponding one of the contact plugs,

wherein each of the contact plugs deviates from a central point spaced at the same distance from the dummy vertical structures that are diagonally across the each of the contact plugs.

8. The three-dimensional semiconductor memory device of any one of claims 1 to 7, further comprising:

an interlayer dielectric layer on top surfaces of the first and second contact plugs;
and

a connection line group in the interlayer dielectric layer and includes a plurality of lower connection lines extending in the first direction,

wherein, when viewed in plan, the connection line group is between the first contact plugs and the second contact plugs.

9. A three-dimensional semiconductor memory device, comprising:

a substrate including a cell array region and a connection region;

an electrode structure including a plurality of electrodes vertically stacked on the substrate, each of the electrodes having a pad portion on the connection region;

an electrode separation structure penetrating the electrode structure and extending in a first direction;

a plurality of contact plugs coupled to corresponding pad portions of the electrodes, the contact plugs including a first contact plug and a second contact plug apart in a second direction intersecting the first direction, the electrode separation structure between the first contact plug and the second contact plug, and the plurality of electrodes being vertically stacked in a third direction intersecting the first and second directions; and

a connection line group between the first contact plug and the second contact plug, the connection line group including a plurality of lower connection lines that extend in the first direction,

wherein the first contact plug is apart in the second direction at a first distance from the electrode separation structure, and

wherein the second contact plug is apart from the electrode separation structure at a second distance, different from the first distance.

10. The three-dimensional semiconductor memory device of claim 9, wherein the contact plugs have a width greater than a line width of the lower connection lines.

11. The three-dimensional semiconductor memory device of claim 9 or claim 10, further comprising:

an interlayer dielectric layer on the contact plugs; and

a plurality of upper connection lines on the interlayer dielectric layer,

wherein the lower connection lines are between the contact plugs and the upper connection lines.

12. The three-dimensional semiconductor memory device of any one of claims 9 to 11, wherein bottom surfaces of the lower connection lines are at the same level as that of top surfaces of the contact plugs.

13. The three-dimensional semiconductor memory of any one of claims 9 to 12, wherein

top surfaces of the first and second contact plugs are at the same level, and
bottom surfaces of the first and second contact plugs are at different levels.

14. The three-dimensional semiconductor memory device of any one of claims 9 to 13, wherein the pad portions of the electrodes are correspondingly between the electrode separation structures adjacent to each other in the second direction.

15. A three-dimensional semiconductor memory device, comprising:
a substrate including a cell array region and a connection region;
an electrode structure including a plurality of electrodes that are vertically stacked on the substrate, the electrode structure having on the connection region a plurality of first pad portions and a plurality of second pad portions;

a plurality of first contact plugs along a first direction and coupled to corresponding first pad portions;

a plurality of second contact plugs coupled to corresponding second pad portions and apart in a second direction from the first contact plugs, the second direction intersecting the first direction;

an electrode separation structure penetrating the electrode structure and extending along the first direction between the first contact plugs and the second contact plugs;

a plurality of first dummy vertical structures penetrating corresponding first pad portions between the electrode separation structure and the first contact plugs; and

a plurality of second dummy vertical structures penetrating corresponding second pad portions between the electrode separation structure and the second contact plugs,

wherein the first and second dummy vertical structures are apart in the second direction at a first distance from the electrode separation structure,

wherein the first contact plugs are apart in the second direction at a second distance from the electrode separation structure, and

wherein the second contact plugs are apart in the second direction from the electrode separation structure at a third distance, different from the second distance.

16. The three-dimensional semiconductor memory device of claim 15, further comprising a connection line group between the first contact plugs and the second contact plugs when viewed in plan,

wherein the connection line group comprises a plurality of lower connection lines extending in the first direction.

17. The three-dimensional semiconductor memory device of claim 16, further comprising:

an interlayer dielectric layer on top surfaces of the first and second contact plugs; and

a plurality of upper connection lines on the interlayer dielectric layer,

wherein the lower connection lines are between the upper connection lines and the first contact plugs and between the upper connection lines and the second contact plugs.

18. The three-dimensional semiconductor memory device of claim 16 or claim 17, wherein

the first and second dummy vertical structures have a first width greater than a line width of the lower connection lines, and

the first and second contact plugs have a second width greater than the first width.

19. The three-dimensional semiconductor memory device of any one of claims 15 to 18, wherein top surfaces of the first and second dummy vertical structures are at a lower level than that of top surfaces of the first and second contact plugs.

20. The three-dimensional semiconductor memory device of any one of claims 15 to 19, wherein the first and second contact plugs are spaced apart differently in the second direction from the electrode separation structure.