

ABSTRACT

A semiconductor memory device according to an embodiment includes a plurality of planes, and a sequencer. The plurality of planes include a plurality of blocks each being a set of memory cells. The sequencer execute a first operation and a second operation shorter than the first operation. Upon receiving a first command set that instructs execution of the first operation, the sequencer executes the first operation. Upon receiving a second command set that instructs execution of the second operation while the first operation is being executed, the sequencer suspends the first operation and execute the second operation or executes the second operation in parallel with the first operation, based on an address of a block that is a target of the first operation and an address of a block that is a target of the second operation.