

Abstract

A non-volatile semiconductor memory device that achieves downsizing as compared to conventional cases is disclosed. A non-volatile semiconductor memory device 1 has a configuration in which a memory cell 3a (3b) is disposed between a programming bit line PGP0 (PGP1) and a reading bit line BLP. The reading bit line BLP provided between the memory cells 3a and 3b adjacent to each other is shared by the memory cells 3a and 3b adjacent to each other. This configuration of the non-volatile semiconductor memory device 1, in which the reading bit line BLP is shared by the memory cells 3a and 3b adjacent to each other, leads to reduction of the number of reading bit lines as compared to that in a conventional configuration, and further leads to reduction of the area of a control circuit and a sense amplifier circuit connected with the reading bit line, thereby achieving downsizing as compared to conventional cases accordingly.