

CLAIMS

1. A computer system, comprising:

a configuration comprising a core configurable between a single thread (ST) mode and a multithreading (MT) mode, the ST mode addressing a primary thread and the MT mode addressing the primary thread and one or more secondary threads on shared resources of the core; and

a multithreading facility configured to control utilization of the configuration to perform a method comprising:

accessing the primary thread in the ST mode using a core address value;

switching from the ST mode to the MT mode;

forming an expanded address value as a shifted core address value by shifting the core address value by an amount based on a requested maximum thread identifier and concatenating the shifted core address value with a thread address value;

accessing the primary thread or one of the one or more secondary threads in the MT mode using the expanded address value;

switching between the MT mode and the ST mode;

selecting the core address value to access the primary thread based on the core being in the ST mode; and

selecting the expanded address value to access the primary thread or one of the one or more secondary threads based on the core being in the MT mode.

2. The computer system according to claim 1, wherein a standard- format address is used in the ST mode, and the core reverts from the MT mode to the ST mode based on disabling the MT mode.

3. The computer system according to claim 2, wherein only the primary thread and not the one or more secondary threads is accessible based on disabling the MT mode.

4. A computer implemented method for address adjustment in a configuration comprising a core configurable between a single thread (ST) mode and a multithreading (MT) mode, the ST mode addressing a primary thread and the MT mode addressing the primary thread and one or more secondary threads on shared resources of the core, the method comprising:

accessing the primary thread in the ST mode using a core address value;

switching from the ST mode to the MT mode;

forming an expanded address value as a shifted core address value by shifting the core address value by an amount based on a requested maximum thread identifier and concatenating the shifted core address value with a thread address value;

accessing the primary thread or one of the one or more secondary threads in the MT mode using the expanded address value;

switching between the MT mode and the ST mode;

selecting the core address value to access the primary thread based on the core being in the ST mode; and

selecting the expanded address value to access the primary thread or one of the one or more secondary threads based on the core being in the MT mode.

5. The method according to claim 1, wherein a standard- format address is used in the ST mode, and the core reverts from the MT mode to the ST mode based on disabling the MT mode.

6. The method according to claim 5, wherein only the primary thread and not the one or more secondary threads is accessible based on disabling the MT mode.

7. A computer program product for address adjustment in a configuration comprising a core configurable between a single thread (ST) mode and a multithreading (MT) mode, the ST mode addressing a primary thread and the MT mode addressing the primary thread and one or more secondary threads on shared resources of the core, the computer program product comprising:

a computer readable storage medium having program instructions embodied therewith, wherein the computer readable storage medium is not a signal, the program instructions readable by a processing circuit to cause the processing circuit to perform a method comprising:

accessing the primary thread in the ST mode using a core address value;

switching from the ST mode to the MT mode;

forming an expanded address value as a shifted core address value by shifting the core address value by an amount based on a requested maximum thread identifier and concatenating the shifted core address value with a thread address value;

accessing the primary thread or one of the one or more secondary threads in the MT mode using the expanded address value;

switching between the MT mode and the ST mode;

selecting the core address value to access the primary thread based on the core being in the ST mode; and

selecting the expanded address value to access the primary thread or one of the one or more secondary threads based on the core being in the MT mode.

8. The computer program product according to claim 7, wherein a standard- format address is used in the ST mode, and the core reverts from the MT mode to the ST mode based on disabling the MT mode, and only the primary thread and not the one or more secondary threads is accessible based on disabling the MT mode.