

Description

The invention relates to an amplifier arrangement for amplifying an input signal and for providing a first output signal which is an amplified version of the input signal, the amplifier arrangement comprising:

a first amplifier having a first supply input terminal for carrying a boosting voltage, the first supply input terminal being coupled to a first supply voltage terminal via a unidirectional element to receive a first supply voltage, a second supply input terminal coupled to a second supply voltage terminal to receive a second supply voltage, a first signal input terminal for receiving the input signal, and a first output terminal for supplying the first output signal, the first output signal being superimposed on a specific direct voltage level,

a second amplifier for varying the boosting voltage on the first supply input terminal in response of the input signal, the second amplifier having a third supply input terminal coupled to the first supply voltage terminal, a fourth supply input terminal coupled to the second supply voltage terminal, a second input signal terminal for receiving a signal which is indicative of the momentary amplitude of the input signal and a second output terminal for supplying a second output signal, the second output terminal being coupled to the first supply input terminal by means of a capacitor.

Such an amplifier arrangement is suitable for boosting the output power of an amplifier operating with a small voltage difference between the two supply voltage terminals, as employed, for example, in car radios.

Such an amplifier arrangement is known from United States Patent 4,752,747. In this known arrangement a similar input signal is applied to both the first and the second signal input terminal. This input signal is amplified by the first amplifier, the amplified signal appearing on the first output terminal, which is coupled to a load. However, the input signal is amplified by the second amplifier only if it exceeds a threshold value, the amplifier signal then being available on the second output terminal. Since the second output terminal is coupled to the first supply input terminal via a capacitor, the boosting voltage on the first supply input terminal will track the variations of the second output signal. In relation to the second supply voltage this boosting voltage determines the voltage difference at which the first amplifier is operated. The coupling of the first supply input terminal to the first supply voltage terminal via the uni-directional element imposes a minimum value on the boosting voltage, which value is substantially equal to the first supply voltage. The boosting voltage is equal to said minimum value if the input signal does not exceed the threshold value and varies if the first output signal tends to be limited by the first supply voltage and the input signal consequently ex-

ceeds the threshold value. The boosting voltage can then become equal to at the most two times the voltage difference between the first and the second supply voltage terminal. This results in the maximum output power being quadrupled. In order to reach this maximum output power the direct voltage level on the first output terminal should be equal to the first supply voltage, so that the first output signal is centred relative to the maximum output voltage swing. However, for comparatively small input signals such a direct voltage level has the disadvantage that the first output signal tends to be limited unnecessarily by the first supply voltage during on an average half the time and that, consequently, boosting voltage variations occur, attend with a comparatively high distortion. This can be reduced by another setting of the direct voltage level on the first supply input terminal but this results in a reduced maximum output power owing to the off-centred position relative to the output voltage swing.

Therefore, it is an object of the invention to provide an amplifier arrangement capable of supplying a maximal output power but having a minimal distortion as a result of boosting voltage variations.

An amplifier arrangement in accordance with the invention is characterized in that the amplifier arrangement further comprises:

a signal-follower circuit coupled to the first output terminal for establishing the direct voltage level on the first output terminal and

a third amplifier having differential signal input terminals of which a first differential signal input terminal is coupled to the first output terminal to receive the first output signal and of which a second differential input signal terminal is coupled to receive a reference voltage, a fifth supply input terminal coupled to the first supply voltage terminal, a sixth supply input terminal coupled to the second supply voltage terminal, and a third signal output terminal for supplying a third output signal which is coupled to an input terminal of the signal-follower circuit for changing the direct voltage level in response of a comparison between the first output signal and the reference voltage.

UK Patent Application GB-A-2 084 420 discloses an amplifier arrangement having a signal-follower which provides a fixed direct-voltage level at the output terminal of the arrangement. The direct-voltage level, however, is not changed in response of the output signal and a reference voltage.

The invention is based on the recognition of the fact that the direct voltage level on the first output terminal should be constantly set to a central level between the boosting voltage and the second supply voltage. This is achieved by locking the first output signal to the direct voltage level, which level is varied if the first output signal tends to be limited by the second supply voltage. For this purpose the first output signal is compared with the ref-

erence signal, which is a measure of a maximum permissible first output signal without a variation of the boosting voltage. This comparison results in the third output signal, which drives the signal-follower circuit. A comparatively small first output signal resulting from a comparatively small first input signal will therefore neither effect the direct voltage level nor give rise to boosting voltage variations. However, as soon as an increase of the first input signal results in the reference signal being exceeded the direct voltage level on the first output terminal will track the boosting voltage proportionally. This ensures that the direct voltage level is constantly centred relative to the first output signal swing, so that boosting voltage variations are minimized and the maximum output power is obtained.

A first embodiment of an amplifier arrangement in accordance with the invention may be characterized in that the signal-follower circuit comprises first means, second means and a current-mirror circuit having an input terminal and an output terminal, the input terminal of the current-mirror circuit being coupled both to the first supply voltage terminal by the first means and to the third output terminal and the output terminal of the current-mirror circuit being coupled to the first output terminal by the second means. The signal on the input terminal of the current-mirror circuit then determines the direct voltage level on the first output terminal depending on the current mirror ratio of the current-mirror circuit and the construction of the second means. If the boosting voltage does not vary the magnitude of this signal is related to the construction of the first means. If the boosting voltage exhibits variations the magnitude of the signal is dictated by the third output signal.

The first embodiment is further characterized in that the first means comprise at least a unidirectional element and a resistor, which are coupled in series between the input terminal of the current-mirror circuit and the first supply voltage terminal. The voltage drop across the unidirectional element, which may be provided in multiple depending on the construction of the first amplifier, and the value of the resistor then dictate the signal of the input terminal of the current-mirror circuit in the absence of boosting voltage variations.

The first embodiment is further characterized in that the second means comprise at least a resistor, which is coupled between the output terminal of the current-mirror circuit and the first output terminal. The value of the resistor then dictates the direct voltage level on the first output terminal depending on the signal on the output terminal of the current-mirror circuit, for example an output current.

A second embodiment of an amplifier arrangement in accordance with the invention may be characterized in that the third amplifier comprises inter alia a differential stage comprising at least two transistors each having a first main electrode, a control electrode and a second main electrode, a current source circuit and a reference-signal circuit, the first main electrodes being cou-

pled both to one another and to the current source circuit, one control electrode being coupled to the first output terminal, the other control electrode being coupled to the reference-signal circuit to receive the reference signal, and one second main electrode being coupled to the third output terminal. The differential stage operates as a threshold circuit for varying the third output signal on the third output terminal. The reference signal constitutes the threshold, which is related to the maximum permissible first output signal in the absence of boosting voltage variations. When the threshold is exceeded the third amplifier will take over the drive of the current-mirror circuit from the first means.

A further embodiment of an amplifier arrangement in accordance with the invention may be characterized in that the arrangement further comprises a fourth and a fifth amplifier, which are coupled and constructed similarly to the first and the second amplifier, the fourth amplifier consequently comprising a fourth output terminal for supplying a fourth output signal superimposed on a further direct voltage level, in that the signal-follower circuit is further adapted to establish the further direct voltage level on the fourth output terminal, and in that the third amplifier is further adapted to drive the signal-follower circuit depending on a comparison between the fourth output signal and the reference signal, the third amplifier comprising a further input terminal, which is coupled to the fourth output terminal. In this embodiment the first and the fourth amplifier constitute a bridge amplifier circuit, whose direct voltage levels on the output terminals are set by the signal-follower circuit via the third amplifier, depending upon the first and the fourth output signal. Owing to the use of an OR gate both direct voltage levels will be corrected if one of said output signals exceeds the reference signal. In this embodiment the second means are provided in duplicate.

The invention will now be described in more detail, by way of example, with reference to the accompanying drawings in which

Fig. 1 shows an embodiment of an amplifier arrangement in accordance with the invention, and
Fig. 2 shows an example of the third amplifier of an amplifier arrangement in accordance with the invention.

In these Figures like parts bear the same reference numerals.

Fig. 1 shows an embodiment of an amplifier arrangement in accordance with the invention. The arrangement comprises a first amplifier A1, which has a terminal 1 and a terminal 2, which are respectively coupled to a supply voltage terminal Vdd by a diode D1 and to a supply voltage terminal Vss, and which has an input terminal 5 for receiving an input signal Vin1 and an output terminal 6 for supplying an output signal Vout1, and a second amplifier A2, which has a terminal 3 and a terminal 4, which are coupled to the supply voltage terminals Vdd and Vss

respectively, and which has as an input terminal 7 for receiving an input signal V_{in} and an output terminal 8 for supplying the output signal V_{uit2} . A capacitor C1 couples the output terminal 8 to the terminal 1, which carries a boosting voltage V_t . The arrangement further comprises a third amplifier A3 and a signal-follower circuit comprising first means M1, second means M2 and a current-mirror circuit S. The third amplifier A3 is coupled to the supply voltage terminal V_{dd} via a terminal 9 and to the supply voltage terminal V_{ss} via a terminal 10. The third amplifier A3 further comprises an inverting input terminal 11, which is coupled to the output terminal 6, a non-inverting input terminal 12, which carries a reference signal V_{ref} , and an output terminal 13, which carries an output signal V_{uit3} . The means M1 are coupled to the supply voltage terminal V_{dd} and, via a terminal 17, to the current-mirror circuit S, and the means M2 are coupled to the output terminal 6 and, via a terminal 18, to the current-mirror circuit S, which circuit is also coupled to the supply voltage terminal V_{ss} . The input signals V_{in1} and $V_{in1'}$ are related to one another. $V_{in1'}$ may be substantially equal to V_{in1} or may be a rectified replica of V_{in1} . The amplifier A1 amplifies the input signal V_{in} to form the output signal V_{uit1} , which is applied to a load via the output terminal 6. The amplifier A2, however, only amplifies the input signal $V_{in1'}$ to form the output signal V_{uit2} when a threshold value is exceeded. The output signal V_{uit2} is then applied to the terminal 1 via the capacitor C1, which terminal will consequently track the variations of the output signal V_{uit2} . If the input signal $V_{in1'}$ does not exceed said threshold value the amplifier A1 will supply the output signal V_{uit1} without being limited by the supply voltage on the supply voltage terminal V_{dd} or V_{ss} . For this purpose the direct voltage level on the output terminal 6 is centred between the boosting voltage V_t and the supply voltage V_{ss} . Thus, the amplifier A1 can be operated fairly deep in the output voltage swing without causing the boosting voltage V_t to be varied. When the input signal $V_{in1'}$ increases the threshold value will be exceeded, causing the output signal V_{uit2} to become non-zero and the boosting voltage to vary proportionally. However, in order to ensure that the output voltage V_{uit1} is not limited by the supply voltage V_{ss} the direct voltage level should also vary. For this purpose the output signal V_{uit1} is compared with the reference signal V_{ref} . If said threshold value is exceeded this comparison results in the drive of the current-mirror circuit S being taken over. The diode D2 and the means M1 will then be cut off and the amplifier A3 will drive the current-mirror circuit S. This current-mirror circuit S corrects the direct voltage level on the output terminal 6 via the means M2. Fig. 1 shows a possible construction for the means M1 and M2 and for the current-mirror circuit S. The means M1 comprise a diode D2 and a resistor R1 coupled in series. The diode D2 serves to provide a voltage drop which is related to that between the supply voltage terminal V_{dd} and the output terminal 13. For this purpose a plurality of diodes may be employed, which also cause an identical temperature de-

pendence for the two drives of the current-mirror circuit S. The means M2 comprise a resistor R2 and the current-mirror circuit S comprises two transistors T1 and T2 arranged as a current mirror. The resistor R1 mainly defines the direct voltage setting. In the absence of variations of the boosting voltage V_t on the terminal 1 the diode D2 and the resistor R1 together with the diode-connected transistor T1 effect a voltage division, the current mirror (T1, T2) being driven by the signal on the terminal 17. Both the values and the ratio between the values of the resistors R1 and R2 can be optimized by selecting unequal surface areas for the transistors T1 and T2. The value of the resistor R2 determines the direct voltage level on the output terminal 6 on the basis of the current through the transistor T2. Moreover, the means M2 can provide feedback of the output signal V_{uit1} to the input signal V_{in1} . This is possible for example by applying the input signal V_{in1} to an input buffer, which by means of a further resistor is coupled to the terminal 18. The resistor R2 together with the further resistor then determines the feedback factor.

Fig. 2 shows an example of the third amplifier of an amplifier arrangement in accordance with the invention. In this amplifier a transistor T3 and a transistor T4 constitute a differential pair, whose mutually coupled first main electrodes are connected to a current source circuit. This circuit is realized by coupling a transistor T5 and a transistor T6 to form a current mirror. The first main electrodes of the two transistors are connected to the supply voltage terminal V_{dd} and the second main electrode of the transistor T5 is coupled to the differential pair (T3, T4). The second main electrode of the transistor T6 is coupled to the control electrodes of the current mirror (T5, T6) and, via a series arrangement of the main current path of a transistor T7 and a resistor R5, to the supply voltage terminal V_{ss} . The transistor T7 is of a conductivity type opposite to that of the other transistors in the present example of the third amplifier A3. The control electrode of the transistor T7 is connected to the two supply voltage terminals V_{dd} and V_{ss} by a resistor R3 and a resistor R4 respectively. The ratio between the values of these resistors R3 and R4 determines the voltage between the control electrode and the first main electrode of the transistor T7 and the voltage across the resistor R5. As a result of this, the current supplied to the differential pair (T3, T4) is proportional to the voltage difference between the supply voltage terminals V_{dd} and V_{ss} . The control electrode of the transistor T3 is coupled to the two supply voltage terminals V_{dd} and V_{ss} by a current source J1 and the main current path of a transistor T8 respectively. The control electrode of this transistor T8 is also coupled to the two supply voltage terminals V_{dd} and V_{ss} by means of a number of series-connected diodes D3, D4, D5 and a current source J2 respectively. In addition, the control electrode of the transistor T3 is coupled to the terminal 11 by a diode D6, which terminal carries the output signal V_{uit1} , as is shown in Fig. 1. If the third amplifier A3 is employed in a bridge amplifier

arrangement the control electrode of the transistor T3 is also coupled to a terminal 11' by means of a diode D6'. The two output terminals of the bridge amplifier, between which a load is coupled, are then connected to the terminals 11 and 11', the diodes D6 and D6' operating as an OR gate. They are turned on when the output signal on the terminal 11 or the terminal 11' tends to be limited by the supply voltage on the supply voltage terminal Vss. The turn-on instant depends on the reference signal Vref on the control electrode of the transistor T4. This reference signal Vref is obtained by coupling said control electrode to the supply voltage terminals Vdd and Vss by a current source J3 and a series arrangement of a diode D7 and a resistor R6 respectively. It is possible to arrange a plurality of diodes in series with the diode D7 but the number of the diodes should be equal to the number of diodes between the control electrode of the transistor T3 and the terminal 11. This requirement is based on the function of the resistor R6. The voltage across this resistor determines the threshold at which the output signal Vuit1, which appears on the terminal 11, tends to be limited and the signal-follower circuit should be driven. If the boosting voltage Vt does not vary the reference signal Vref will be smaller than the voltage on the control electrode of the transistor T3. Consequently, the transistor T4 will be turned on and the transistor T3 will be cut off. The voltage on the control electrode of the transistor T3 is then dictated by the diodes D3, D4 and D5, the current sources J1 and J2, and the transistor T8. The diode D6 will be cut off because the voltage on the terminal 11 will remain higher than the voltage across the resistor R6. If the output signal Vuit1 tends to be limited, resulting in variations of the boosting voltage Vt, the voltage on the terminal 11 will become smaller than the voltage across the resistor R6. The diode D6 will be turned on and for this purpose it will receive current from the current source J1. The transistors T8 and T4 will be cut off as a result of the voltage drop on the control electrode of the transistor T3. This transistor now drives the signal-follower circuit via the output signal Vuit3 on the terminal 13. As a result of capacitive effects or the provision of a capacitance between the terminal 13 and the supply voltage Vss, the drive acts with a specific delay, so that rapid fluctuations are precluded and the direct voltage level on the terminal 6 is corrected gradually. When the third amplifier A3 is employed in a bridge amplifier arrangement the operation is similar. The transistor T3 can then also be turned on by the voltage on the terminal 11'. In order to control the further direct voltage level on a further output terminal the current-mirror circuit S will then comprise a further transistor arranged in parallel with the transistor T2. This further transistor is then also coupled to the further output terminal by the means M2. For controlling the two direct voltage levels said means comprise two similar circuits, each comprising for example a resistor.

The invention is not limited to the embodiments disclosed herein, but to the scope of the claims. Several

modifications to the embodiments are conceivable to those skilled in the art. For example, the means as well as the third amplifier and the current-mirror circuit may be constructed in various manners. Both current control and voltage control of the current-mirror circuit is possible. In addition, it is possible to drive the signal-follower circuit via the third amplifier with a signal proportional to the first output signal, such as for example the input signal or the boosting voltage.

Claims

1. An amplifier arrangement for amplifying an input signal (Vin1) and for providing a first output signal (Vuit1) which is an amplified version of the input signal, the amplifier arrangement comprising:

a first amplifier (A1) having a first supply input terminal (1) for carrying a boosting voltage (Vt), the first supply input terminal (1) being coupled to a first supply voltage terminal (Vdd) via a unidirectional element (D1) to receive a first supply voltage, a second supply input terminal (2) coupled to a second supply voltage terminal (Vss) to receive a second supply voltage, a first signal input terminal (5) for receiving the input signal, and a first output terminal (6) for supplying the first output signal, the first output signal being superimposed on a specific direct voltage level, a second amplifier (A2) for varying the boosting voltage on the first supply input terminal in response of the input signal, the second amplifier (A2) having a third supply input terminal (3) coupled to the first supply voltage terminal (Vdd), a fourth supply input terminal (4) coupled to the second supply voltage terminal (Vss), a second input signal terminal (7) for receiving a signal (Vin1') which is indicative of the momentary amplitude of the input signal and a second output terminal (8) for supplying a second output signal (Vuit2), the second output terminal (8) being coupled to the first supply input terminal (1) by means of a capacitor (C1), characterized in that

the amplifier arrangement further comprises: a signal-follower circuit (M1, S, M2) coupled to the first output terminal (6) for establishing the direct voltage-level on the first output terminal (6) and

a third amplifier (A3) having differential signal input terminals (11, 12) of which a first differential signal input terminal (11) is coupled to the first output terminal (6) to receive the first output signal and of which a second differential input signal terminal (12) is coupled to receive a reference voltage (Vref), a fifth supply input terminal (9) coupled to the first supply voltage terminal

arrangement the control electrode of the transistor T3 is also coupled to a terminal 11' by means of a diode D6'. The two output terminals of the bridge amplifier, between which a load is coupled, are then connected to the terminals 11 and 11', the diodes D6 and D6' operating as an OR gate. They are turned on when the output signal on the terminal 11 or the terminal 11' tends to be limited by the supply voltage on the supply voltage terminal Vss. The turn-on instant depends on the reference signal Vref on the control electrode of the transistor T4. This reference signal Vref is obtained by coupling said control electrode to the supply voltage terminals Vdd and Vss by a current source J3 and a series arrangement of a diode D7 and a resistor R6 respectively. It is possible to arrange a plurality of diodes in series with the diode D7 but the number of the diodes should be equal to the number of diodes between the control electrode of the transistor T3 and the terminal 11. This requirement is based on the function of the resistor R6. The voltage across this resistor determines the threshold at which the output signal Vuit1, which appears on the terminal 11, tends to be limited and the signal-follower circuit should be driven. If the boosting voltage Vt does not vary the reference signal Vref will be smaller than the voltage on the control electrode of the transistor T3. Consequently, the transistor T4 will be turned on and the transistor T3 will be cut off. The voltage on the control electrode of the transistor T3 is then dictated by the diodes D3, D4 and D5, the current sources J1 and J2, and the transistor T8. The diode D6 will be cut off because the voltage on the terminal 11 will remain higher than the voltage across the resistor R6. If the output signal Vuit1 tends to be limited, resulting in variations of the boosting voltage Vt, the voltage on the terminal 11 will become smaller than the voltage across the resistor R6. The diode D6 will be turned on and for this purpose it will receive current from the current source J1. The transistors T8 and T4 will be cut off as a result of the voltage drop on the control electrode of the transistor T3. This transistor now drives the signal-follower circuit via the output signal Vuit3 on the terminal 13. As a result of capacitive effects or the provision of a capacitance between the terminal 13 and the supply voltage Vss, the drive acts with a specific delay, so that rapid fluctuations are precluded and the direct voltage level on the terminal 6 is corrected gradually. When the third amplifier A3 is employed in a bridge amplifier arrangement the operation is similar. The transistor T3 can then also be turned on by the voltage on the terminal 11'. In order to control the further direct voltage level on a further output terminal the current-mirror circuit S will then comprise a further transistor arranged in parallel with the transistor T2. This further transistor is then also coupled to the further output terminal by the means M2. For controlling the two direct voltage levels said means comprise two similar circuits, each comprising for example a resistor.

The invention is not limited to the embodiments disclosed herein, but to the scope of the claims. Several

modifications to the embodiments are conceivable to those skilled in the art. For example, the means as well as the third amplifier and the current-mirror circuit may be constructed in various manners. Both current control and voltage control of the current-mirror circuit is possible. In addition, it is possible to drive the signal-follower circuit via the third amplifier with a signal proportional to the first output signal, such as for example the input signal or the boosting voltage.

Claims

1. An amplifier arrangement for amplifying an input signal (Vin1) and for providing a first output signal (Vuit1) which is an amplified version of the input signal, the amplifier arrangement comprising:

a first amplifier (A1) having a first supply input terminal (1) for carrying a boosting voltage (Vt), the first supply input terminal (1) being coupled to a first supply voltage terminal (Vdd) via a unidirectional element (D1) to receive a first supply voltage, a second supply input terminal (2) coupled to a second supply voltage terminal (Vss) to receive a second supply voltage, a first signal input terminal (5) for receiving the input signal, and a first output terminal (6) for supplying the first output signal, the first output signal being superimposed on a specific direct voltage level, a second amplifier (A2) for varying the boosting voltage on the first supply input terminal in response of the input signal, the second amplifier (A2) having a third supply input terminal (3) coupled to the first supply voltage terminal (Vdd), a fourth supply input terminal (4) coupled to the second supply voltage terminal (Vss), a second input signal terminal (7) for receiving a signal (Vin1') which is indicative of the momentary amplitude of the input signal and a second output terminal (8) for supplying a second output signal (Vuit2), the second output terminal (8) being coupled to the first supply input terminal (1) by means of a capacitor (C1), characterized in that

the amplifier arrangement further comprises: a signal-follower circuit (M1, S, M2) coupled to the first output terminal (6) for establishing the direct voltage-level on the first output terminal (6) and

a third amplifier (A3) having differential signal input terminals (11, 12) of which a first differential signal input terminal (11) is coupled to the first output terminal (6) to receive the first output signal and of which a second differential input signal terminal (12) is coupled to receive a reference voltage (Vref), a fifth supply input terminal (9) coupled to the first supply voltage terminal



nal (Vdd), a sixth supply input terminal (4) coupled to the second supply voltage terminal (Vss), and a third signal output terminal (13) for supplying a third output signal (Vuit3) which is coupled to an input terminal (17) of the signal-follower circuit for changing the direct voltage level in response of a comparison between the first output signal and the reference voltage.

2. An amplifier arrangement as claimed in Claim 1, characterized in that the signal-follower circuit comprises first mean (M1), second means (M2) and a current-mirror circuit (5) having an input terminal (17) and an output terminal (18), the input terminal (17) of the current-mirror circuit (5) being coupled both to the first supply voltage terminal (Vdd) by the first means (M1) and to the third signal output terminal (13), and the output terminal (18) of the current-mirror circuit (5) being coupled to the first signal output terminal (6) by the second means (M2),

the first means comprising at least a unidirectional element (D2) and a resistor (R1), which are coupled in series between the input terminal (17) of the current-mirror circuit (5) and the first supply voltage terminal (Vdd), the second means comprising at least a resistor (R2), which is coupled between the output terminal (18) of the current-mirror circuit (5) and the first signal output terminal (6).

3. An amplifier arrangement as claimed in Claim 2, characterized in that the third amplifier (A3) comprises inter alia a differential stage comprising at least two transistors (T3, T4) each having a first main electrode, a control electrode and a second main electrode, a current source circuit (T5) and a reference-signal circuit (R6, D7), the first main electrodes being coupled both to one another and to the current source circuit (T5), one control electrode being coupled to the first signal output terminal (6), the other control electrode being coupled to the reference-signal circuit (R6, D7) to receive the reference signal, and one second main electrode being coupled to the third signal output terminal (13).

4. An amplifier arrangement as claimed in any one of the preceding Claims, characterized in that the arrangement further comprises a fourth and a fifth amplifier, which are coupled and constructed similarly to the first (A1) and the second amplifier (A2), the fourth amplifier consequently comprising a fourth output terminal for supplying a fourth output signal superimposed on a further direct voltage level, in that the signal-follower circuit is further adapted to establish the further direct voltage level on the fourth output terminal, and in that the third amplifier (A3) is further adapted to drive the sig-

nal-follower circuit depending on a comparison between the fourth output signal and the reference signal, the third amplifier (A3) comprising a further input terminal, which is coupled to the fourth output terminal.

Patentansprüche

1. Verstärkeranordnung zum Verstärken eines Eingangssignals (Vin1) und zum Verschaffen eines ersten Ausgangssignals (Vuit1), das eine verstärkte Version des Eingangssignals ist, wobei die Verstärkeranordnung umfaßt:

einen ersten Verstärker (A1) mit einem ersten Speiseeingangsanschluß (1) zum Führen einer Zusatzspannung (Vt), wobei der erste Speiseeingangsanschluß (1) über ein unidirektionales Element (D1) mit einem ersten Versorgungsspannungsanschluß (Vdd) gekoppelt ist, um eine erste Versorgungsspannung zu empfangen, mit einem mit einem zweiten Versorgungsspannungsanschluß (Vss) gekoppelten zweiten Speiseeingangsanschluß (2), um eine zweite Versorgungsspannung zu empfangen, und mit einem ersten Ausgangsanschluß (6) zum Liefern des ersten Ausgangssignals, wobei das erste Ausgangssignal einem bestimmten Gleichspannungspegel überlagert ist, einen zweiten Verstärker (A2) zum Verändern der Zusatzspannung am ersten Speiseeingangsanschluß in Reaktion auf das Eingangssignal, wobei der zweite Verstärker (A2) einen mit dem ersten Versorgungsspannungsanschluß (Vdd) gekoppelten dritten Speiseeingangsanschluß (3), einen mit dem zweiten Versorgungsspannungsanschluß (Vss) gekoppelten vierten Speiseeingangsanschluß (4), einen zweiten Eingangssignalanschluß (7) zum Empfangen eines Signals (Vin1), das eine Angabe für die momentane Amplitude des Eingangssignals ist, und einen zweiten Ausgangsanschluß (8) zum Liefern eines zweiten Ausgangssignals (Vuit2) hat, wobei der zweite Ausgangsanschluß (8) mittels eines Kondensators (C1) mit dem ersten Speiseeingangsanschluß (1) gekoppelt ist, dadurch gekennzeichnet, daß die Verstärkeranordnung weiterhin umfaßt: eine mit dem ersten Ausgangsanschluß (6) gekoppelte Signalfolgerschaltung (M1, S, M2) zum Ausbauen des Gleichspannungspegels am ersten Ausgangsanschluß (6) und einen dritten Verstärker (A3) mit Differenzsignaleingangsanschlüssen (11, 12), von denen ein erster Differenzsignaleingangsanschluß (11) mit dem ersten Ausgangsanschluß (6) zum



Empfangen des ersten Ausgangssignals gekoppelt ist und von denen ein zweiter Differenzsignaleingangsanschluß (12) zum Empfangen einer Bezugsspannung (V_{ref}) geschaltet ist, mit einem fünften mit dem ersten Versorgungsspannungsanschluß (V_{dd}) gekoppelten Speiseeingangsanschluß (9), einem sechsten mit dem zweiten Versorgungsspannungsanschluß (V_{ss}) gekoppelten Speiseeingangsanschluß (4) und einem dritten Signalausgangsanschluß (13) zum Liefern eines dritten Ausgangssignals (V_{uit3}), der mit einem Eingangsanschluß (17) der Signalfolgerschaltung gekoppelt ist, zum Ändern des Gleichspannungspegels in Reaktion auf einen Vergleich zwischen dem ersten Ausgangssignal und der Bezugsspannung.

2. Verstärkeranordnung nach Anspruch 1, dadurch gekennzeichnet, daß die Signalfolgerschaltung erste Mittel (M1), zweite Mittel (M2) und eine Stromspiegelschaltung (5) mit einem Eingangsanschluß (17) und einem Ausgangsanschluß (18) umfaßt, wobei der Eingangsanschluß (17) der Stromspiegelschaltung (5) sowohl mit dem ersten Versorgungsspannungsanschluß (V_{dd}) über die ersten Mittel (M1) als auch mit dem dritten Signalausgangsanschluß (13) gekoppelt ist, und der Ausgangsanschluß (18) der Stromspiegelschaltung (5) mit dem ersten Signalausgangsanschluß (6) über die zweiten Mittel (M2) gekoppelt ist, wobei die ersten Mittel zumindest ein unidirektionales Element (D2) und einen Widerstand (R1) umfassen, die zwischen dem Eingangsanschluß (17) der Stromspiegelschaltung (5) und dem ersten Versorgungsspannungsanschluß (V_{dd}) in Reihe geschaltet sind, wobei die zweiten Mittel zumindest einen Widerstand (R2) umfassen, der zwischen den Ausgangsanschluß (18) der Stromspiegelschaltung (5) und den ersten Signalausgangsanschluß (6) gekoppelt ist.

3. Verstärkeranordnung nach Anspruch 2, dadurch gekennzeichnet, daß der dritte Verstärker (A3) unter anderem eine Differenzstufe umfaßt, die zumindest zwei Transistoren (T3, T4) umfaßt, von denen jeder eine erste Hauptelektrode, eine Steuerelektrode und eine zweite Hauptelektrode hat, sowie eine Stromquellenschaltung (T5) und eine Bezugssignalschaltung (R6, D7), wobei die ersten Hauptelektroden sowohl miteinander als auch mit der Stromquellenschaltung (T5) gekoppelt sind, die eine Steuerelektrode mit dem ersten Signalausgangsanschluß (6), die andere Steuerelektrode mit der Bezugssignalschaltung (R6, D7) zum Empfangen des Bezugssignals gekoppelt ist, und eine der zweiten Hauptelektroden mit dem dritten Signalausgangsanschluß (13) gekoppelt ist.

4. Verstärkeranordnung nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, daß die Anordnung weiterhin einen vierten und einen fünften Verstärker umfaßt, die entsprechend dem ersten (A1) und dem zweiten (A2) Verstärker geschaltet und aufgebaut sind, wobei der vierte Verstärker demzufolge einen vierten Ausgangsanschluß zum Liefern eines einem weiteren Gleichspannungspegel überlagerten vierten Ausgangssignals umfaßt, daß die Signalfolgerschaltung weiterhin zum Aufbauen des weiteren Gleichspannungspegels an dem vierten Ausgangsanschluß eingerichtet ist, und daß der dritte Verstärker (A3) weiterhin zum Ansteuern der Signalfolgerschaltung in Abhängigkeit von einem Vergleich zwischen dem vierten Ausgangssignal und dem Bezugssignal eingerichtet ist, wobei der dritte Verstärker (A3) einen mit dem vierten Ausgangsanschluß gekoppelten weiteren Eingangsanschluß umfaßt.

Revendications

1. Circuit amplificateur pour amplifier un signal d'entrée (V_{in1}) et pour fournir un premier signal de sortie (V_{uit1}) qui est une version amplifiée du signal d'entrée, le circuit d'amplification comprenant:

un premier amplificateur (A1) présentant une première borne d'entrée d'alimentation (1) pour présenter une surtension (V_t), la première borne d'entrée d'alimentation étant couplée à une première borne de tension d'alimentation (V_{dd}) par l'intermédiaire d'un élément unidirectionnel (D1) pour recevoir une première tension d'alimentation, une deuxième borne d'entrée d'alimentation (2) couplée à une deuxième borne de tension d'alimentation (V_{ss}) pour recevoir une deuxième tension d'alimentation, une première borne d'entrée de signal (5) pour recevoir le signal d'entrée et première borne de sortie (6) pour l'amenée du premier signal de sortie, le premier signal de sortie étant superposé à un niveau de tension continue spécifique,

un deuxième amplificateur (A2) pour la variation de la surtension sur la première borne d'entrée d'alimentation en réponse au signal d'entrée, le deuxième amplificateur (A2) présentant une troisième borne d'entrée d'alimentation (3) couplée à la première borne de tension d'alimentation (V_{dd}), une quatrième borne d'entrée d'alimentation (4) couplée à la deuxième borne de tension d'alimentation (V_{ss}), une deuxième borne de signal d'entrée (7) pour recevoir un signal (V_{in1}) qui est indicatif de l'amplitude momentanée du signal d'entrée et une deuxième borne de sortie (8) pour amener un



deuxième signal de sortie (Vuit2), la deuxième borne de sortie (8) étant couplée à la première borne d'entrée d'alimentation (1) à l'aide d'un condensateur (C1), caractérisé en ce que le circuit amplificateur comporte en outre:

un circuit suiveur de signal (M1, S, M2) couplé à la première borne de sortie (6) pour établir le niveau de tension continue sur la première borne de sortie (6) et

un troisième amplificateur A3 présentant des bornes d'entrée de signal différentiel (11, 12) dont une première borne d'entrée de signal différentiel (11) est couplée à la première borne de sortie (6) pour recevoir le premier signal de sortie et dont une deuxième borne de signal d'entrée différentielle (12) est couplée de façon à recevoir une tension de référence (Vref), une cinquième borne d'entrée d'alimentation (9) couplée à la première borne de tension d'alimentation (Vdd), une sixième borne d'entrée d'alimentation (4) couplée à la deuxième borne de tension d'alimentation (Vss), et une troisième borne de sortie de signal (13) pour amener un troisième signal de sortie (Vuit3) qui est couplé à une borne d'entrée (17) du circuit suiveur de signal pour changer le niveau de tension continue en réponse à une comparaison entre le premier signal de sortie et la tension de référence.

2. Circuit amplificateur selon la revendication 1, caractérisé en ce que le circuit suiveur de signal est muni de premiers moyens (M1), de deuxièmes moyens (M2) et d'un circuit de miroir de courant (5) présentant une borne d'entrée (17) et une borne de sortie (18), la borne d'entrée (17) du circuit de miroir de courant (5) étant couplée à la première borne de tension d'alimentation (Vdd) par les premiers moyens (M1) et à la troisième borne de sortie de signal (13), et la borne de sortie (18) du circuit de miroir de courant (5) étant couplée à la première borne de sortie de signal (6) par les deuxièmes moyens (M2),

les premiers moyens comprennent au moins un élément unidirectionnel (D2) et une résistance (R1) qui sont montés en série entre la borne d'entrée (17) du circuit miroir de courant (5) et la première borne de tension d'alimentation (Vdd),

les deuxièmes moyens comprenant au moins une résistance (R2) qui est couplée entre la borne de sortie (18) du circuit miroir de courant (5) et la première borne de sortie de signal (6).

3. Circuit amplificateur selon la revendication 2, caractérisé en ce que le troisième amplificateur (A3) est entre autres muni d'un étage différentiel comprenant au moins deux transistors (T3, T4) présentant cha-

cun une première électrode principale, une électrode de commande et une deuxième électrode principale, un circuit de source de courant (T5) et un circuit de signal de référence (R6, D7), les premières électrodes principales étant couplées entre elles et au circuit de source de courant (T5), une électrode de commande étant couplée à la première borne de sortie de signal (6), l'autre électrode de commande étant couplée au circuit de signal de référence (R6, D7) pour recevoir le signal de référence et une deuxième électrode principale étant couplée à la troisième borne de sortie de signal (13).

4. Circuit amplificateur selon l'une des revendications précédentes, caractérisé en ce que le circuit est en outre muni d'un quatrième amplificateur et d'un cinquième amplificateur, qui sont couplés et réalisés d'une façon analogue à celle des premier (A1) et deuxième (A2) amplificateurs, le quatrième amplificateur comprenant par conséquent une quatrième borne de sortie pour amener un quatrième signal de sortie superposé à un autre niveau de tension continue, en ce que le circuit suiveur de signal est en outre conçu pour établir l'autre niveau de tension continue à la quatrième borne de sortie, en ce que le troisième amplificateur (A3) est en outre conçu pour commander le circuit suiveur de signal en fonction d'une comparaison entre le quatrième signal de sortie et le signal de référence, le troisième amplificateur (A3) étant muni d'une autre borne d'entrée, qui est couplée à la quatrième borne de sortie.

