RELIABLE INTERCONNECTS

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application is a divisional application which claims benefit of copending U.S. patent application Ser. No. 12/196,291, filed on August 22, 2008. All disclosures are incorporated herewith by reference.

BACKGROUND

[0002] The fabrication of integrated circuits (ICs) involves the formation of features on a substrate that make up circuit components, such as transistors, resistors and capacitors. The devices are interconnected, enabling the IC to perform the desired functions. Interconnections are formed by forming contacts and conductive lines in a dielectric layer using, for example, damascene techniques. A damascene structure, for example, includes a via or contact hole in a lower portion and a trench which is generally wider than the contact hole in an upper portion. The via serves as a contact to a device while the trench contains the conductive line for connecting the device to, for example, other devices.

[0003] As critical dimensions (CD) continue to shrink, time dependent dielectric breakdown (TDDB) has become an important reliability issue. For example, the destruction of the dielectric layer can cause interconnects to short, rendering the IC defective.

[0004] From the foregoing discussion, it is desirable to improve TDDB to increase IC reliability.

SUMMARY

[0005] Embodiments generally relate to a semiconductor devices and methods of forming a semiconductor device. In one embodiment, a method for forming a semiconductor device is presented. The method includes providing a substrate prepared with a dielectric layer formed thereon. The dielectric layer has a conductive line disposed in an upper portion of the dielectric layer. The method includes processing the substrate to produce a top surface of the dielectric

layer that is not coplanar with a top surface of the conductive line to form a stepped topopgraphy. In another embodiment, the top surface of the dielectric layer is below or above the top surface of the conductive wherein such configuration improves TDDB.

[0006] A semiconductor device is disclosed in one embodiment. The semiconductor device includes a substrate and a dielectric layer on the substrate. The dielectric layer has a conductive line in an upper portion thereof. A top surface of the dielectric layer and a top surface of the conductive line form a stepped topography.

[0007] These and other objects, along with advantages and features of the present invention herein disclosed, will become apparent through reference to the following description and the accompanying drawings. Furthermore, it is to be understood that the features of the various embodiments described herein are not mutually exclusive and can exist in various combinations and permutations.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] In the drawings, like reference characters generally refer to the same parts throughout the different views. Also, the drawings are not necessarily to scale, emphasis instead generally being placed upon illustrating the principles of the invention. In the following description, various embodiments of the present invention are described with reference to the following drawings, in which:

[0009] Fig. 1 shows a cross-sectional view of a portion of an embodiment of an IC;

[0010] Fig. 2 shows a cross-sectional view of a portion of another embodiment of an IC;

[0011] Figs. 3a-d show a process for forming an embodiment of an IC in accordance with one embodiment of the invention;

[0012] Fig. 4 shows a cross-sectional view of a portion of yet another embodiment of an IC;

[0013] Fig. 5 shows a cross-sectional view of a portion of another embodiment of an IC; and

[0014] Figs. 6a-d show a process for forming another embodiment of an IC in accordance with one embodiment of the invention.

DETAILED DESCRIPTION

[0015] Embodiments generally relates to ICs. More particularly, the present invention relates to interconnections and processes for forming such ICs. The ICs can be any type of IC, for example dynamic or static random access memories, signal processors, or system-on-chip devices. The ICs can be incorporated into, for example, consumer electronic products, such as computers, cell phones, and personal digital assistants (PDAs).

[0016] Fig. 1 shows a cross-sectional view of a portion of an integrated circuit (IC) 100 in accordance with one embodiment. As shown, the portion includes a substrate 105. The substrate, for example, comprises a silicon substrate. Other types of substrates, such as silicon germanium or silicon-on-insulator (SOI), are also useful. The substrate may include circuit components (not shown) such as transistors, capacitors, or resistors formed thereon. Other types of circuit components are also useful.

[0017] A dielectric layer 130 is disposed on the substrate. The dielectric layer, for example, serves as an interconnect dielectric (ICD) layer in which interconnections are formed. In one embodiment, the ICD includes lower and upper portions. The lower portion serves as an inter-level dielectric (ILD) layer while the upper portion serves as an intra-metal dielectric (IMD) layer. The dielectric layer can be a single layer or multi-layered stack. For example, a single layer can be used to serve as both the ILD and IMD or separate layers are used for the ILD and IMD. In some cases, an etch stop layer can be disposed between the ILD and IMD.

[0018] The dielectric layer can comprise, for example, silicon oxide. Other types of dielectric materials are also useful. For example, the dielectric layer can comprise doped silicon

oxide such as fluorinated silicon oxide (FSG), undoped or doped silicate glasses such as boron phosphate silicate glass (BPSG) and phosphate silicate glass (PSG), undoped or doped thermally grown silicon oxide, undoped or doped TEOS deposited silicon oxide, and low-k or ultra low-k dielectric materials such as organo-silicate glass (OSG) and fluorine-doped silicate glass (FSG). Preferably, at least the IMD layer comprises a low-k or ultra low-k dielectric material.

[0019] Conductive lines 150 are formed in the IMD portion of the ICD layer. The conductive lines comprise a conductive material such as copper. Other types of metals, alloys or conductive materials are also useful. Contacts (not shown) can be provided in the ILD portion, connecting the conductive lines to contact regions below. Depending on the ICD level, the contact regions can be other metal lines or devices, such as diffusion or gates of transistors. The conductive lines and contacts can comprise the same or different materials. The conductive lines and/or contacts can be provided with slanted sidewalls. The slanted sidewall profile improves sidewall barrier and seed coverage during processing. The slanted sidewalls, for example, comprise an angle of about 85 - 90°. Other sidewall angles, including non-slanted sidewalls, are also useful.

[0020] The conductive lines can include a barrier 155 lining sidewalls and bottoms thereof. The barrier prevents the diffusion of the conductive line material, for e.g. Cu, into the ICD layer. The barrier also serves as an adhesion layer for other conductive line material to better adhere to the dielectric material. The barrier, for example, can comprise tantalum nitride (TaN). Other types of barrier materials, such as tantalum, titanium nitride, ruthenium or a combination thereof, are also useful.

[0021] In accordance with one embodiment, a top surface 158 of the conductive lines is disposed below a top surface 132 of the ICD layer by a distance H. Recessing the top surface of the conductive lines below the top surface of the ICD layer increases the effective distance between the conductive lines. This has been found to increase the reliability of the dielectric

layer by improving TDDB. In one embodiment, H is sufficient to improve TDDB. In one embodiment, H is about 250 - 450Å. Other values of H are also useful.

[0022] In one embodiment, an etch stop layer 170 is disposed over the surface of the ICD layer. The etch stop layer covers the ICD and top of the conductive lines. The etch stop layer, in one embodiment, comprises a dielectric material, such as silicon nitride. The etch stop layer can also be a conductive layer, for example a metal layer such as CoWP, or CVD Ru, or a composite of dielectric and conductive material layers. The conductive layer can be deposited by electro-less plating or CVD. Other types of etch stop materials or techniques for forming the etch stop layer are also useful. The etch stop layer can also serve as a barrier layer to protect the conductive lines from oxidation. Additionally, it may also be used as an adhesion layer for subsequent layers deposited thereon.

[0023] Fig. 2 shows a cross-sectional view of a portion of an integrated circuit (IC) 200 in accordance with one embodiment. The portion, similar to the portion of Fig. 1, includes an ICD layer 130 with interconnects 150 disposed over a substrate 105, wherein a top surface 158 of the conductive lines is recessed below the top surface of the ICD layer 132 by a distance H. In one embodiment, an etch stop layer 170 is disposed over the surface of the ICD layer. The etch stop layer covers the ICD and top of the conductive lines.

[0024] Above the ICD layer is disposed a dielectric layer 275. In one embodiment, the dielectric layer serves as another ICD layer of another interconnect level. For example, the first ICD layer 130 serves as the first interconnect level and the second ICD layer 275 serves as the second interconnect level. Additional ICD layers can be provided, corresponding to additional interconnect levels.

[0025] The second ICD layer 275, like the first ICD layer 130, includes lower and upper portions corresponding to ILD and IMD. Second ICD layer may comprise a single dielectric layer or multi-layered stack. Conductive lines 260 are disposed in the upper portion of the

second ICD layer. Contacts 263 can be provided in the ILD, for example, to couple the conductive lines in the IMD of the second ICD layer to conductive lines or contact regions below. To ensure that the contacts are in electrical communication with the conductive lines below, they extend through the etch stop.

[0026] The conductive lines and contacts can include a barrier 265 lining sidewalls and bottoms thereof. The barrier, for example, can comprise TaN. Other types of barrier materials, such as tantalum, titanium nitride, ruthenium or a combination thereof, are also useful. As shown, the top surface of the second ICD layer 275 is coplanar with the top surface of the conductive lines 268. In one embodiment, the top surface of the second ICD layer can be recessed similar to that of the first ICD layer. Additionally, an etch stop layer can be provided over the top surface of the second ICD layer and conductive lines. Furthermore, additional ICD layers can be provided over the second ICD layer corresponding to additional interconnect levels.

[0027] Figs. 3a-d show a process for forming a portion 300 of an IC in accordance with one embodiment. Referring to Fig. 3a, a substrate 305 is provided. The substrate, in one embodiment, comprises a p-type silicon substrate. Other types of substrates, such as a germanium-based, gallium arsenide, silicon-on-insulator (SOI), or sapphire substrate, are also useful. The substrate can be prepared with circuit components (not shown). Circuit components can include, for example, transistors, capacitors and/or resistors. Other types of circuit components are also useful.

[0028] The substrate is further prepared with an ICD layer 330. The ICD layer includes an upper or IMD portion and a lower or ILD portion. The ICD can be a single layer or multi-layered stack. For example, a single layer can be used to serve as both the ILD and IMD or separate layers are used for the ILD and IMD. In some cases, an etch stop layer can be disposed between the ILD and IMD. The ICD layer can comprise, for example, silicon oxide. Other

types of dielectric materials are also useful. For example, the dielectric layer can comprise doped silicon oxide such as fluorinated silicon oxide (FSG), undoped or doped silicate glasses such as boron phosphate silicate glass (BPSG) and phosphate silicate glass (PSG), undoped or doped thermally grown silicon oxide, undoped or doped TEOS deposited silicon oxide, and low-k or ultra low-k dielectric materials such as organo-silicate glass (OSG) and fluorine-doped silicate glass (FSG). Preferably, at least the IMD layer comprises a low-k or ultra low-k dielectric material.

[0029] The ICD layer or layers can be deposited using various types of deposition techniques. For example, chemical vapor deposition (CVD) processes such as plasma enhanced (PECVD), high density (HDCVD), atmospheric pressure (APCVD) can be used. Other techniques such as spin-on processes are also useful. The specific process, for example, can depend on the type of material used and application. The ICD layer may be planarized to improve subsequent processing, such as pattern transfer processes.

[0030] Conductive lines 350 and contacts (not shown) are formed in the IMD and ILD portions, respectively, of the ICD layer. Various techniques such as damascene or dual damascene techniques can be used. Other techniques, such as reactive ion etching (RIE), can also be useful. The conductive lines and contacts can be formed from the same material or from different materials. The conductive lines and/or contacts can be provided with slanted sidewalls. The slanted sidewalls, for example, comprise an angle of about 85 - 90°. Providing conductive lines and/or contacts with non-slanted sidewalls is also useful.

[0031] For example, in a dual damascene process, via openings and trenches are formed in the ICD layer to produce dual damascene structures. A barrier 355 can be deposited on the substrate, lining the surface of the ICD and dual damascene structures. The barrier, for example, can comprise TaN. Other types of barrier materials, such as tantalum, titanium nitride, ruthenium or a combination thereof, are also useful. The barrier can be formed by, for example,

PVD, CVD or atomic layer deposition (ALD). Other techniques for forming the barrier are also useful.

[0032] A conductive material is deposited on the substrate covering barrier and filling the dual damascene structure. The conductive material, for example, comprises copper, aluminum, tungsten, alloys such as Al doped Cu, Mn doped Cu, or a combination thereof. Other types of conductive materials, including metals and alloys, are also useful. In one embodiment, the conductive material comprises copper. The conductive material can be deposited by electro-plating. Other techniques, such as electro-less plating, CVD, PVD or sputtering, are also useful.

[0033] Excess material on the surface of the ICD layer is removed by a planarizing process to form a planar surface with the top of the ICD layer. For example, excess conductive and barrier materials on the surface of the ICD layer are removed by a polishing process, such as chemical mechanical polishing. Other types of planarizing or polishing processes are also useful. The polishing process may include multiple polishing steps to remove the different materials, such as conductive and barrier materials. Similar to dual damascene process, a planarizing process can be used to form a planar surface between the vias and ILD and a planar surface between the conductive lines and IMD.

[0034] Referring to Fig. 3b, the conductive lines are recessed, wherein a top surface 358 of the conductive lines are recessed below the top surface 332 of the ICD layer by a distance H, creating a stepped topography. In one embodiment, H is about 250-450Å. Other values of H are also useful. By creating a stepped topography, the effective distance between metal lines can be increased. This improves the TDDB of the ICD, thereby enhancing reliability.

[0035] In one embodiment, a reverse electrochemical plating is performed to recess the conductive lines below the surface of the ICD layer. For example, e-CMP can be used to recess the conductive lines. Other techniques can also be used to recess the conductive lines. The

conductive material can be over polished by CMP. Alternatively, etch back techniques, for example, selective etch back, are also useful.

[0036] Referring to Fig. 3c, an etch stop layer 370 is deposited on the substrate, covering the top of the ICD and conductive lines. In one embodiment, the etch stop layer comprises silicon nitride. The etch stop layer can also be a conductive layer, for example a metal layer such as CoWP, or a composite of dielectric and metal layers. The etch stop layer, for example, is deposited by CVD or electroless-plating. Other techniques for depositing the etch stop layer is also useful. The thickness of the etch stop layer is about 350 - 450Å for dielectric material such as silicon nitride or 40 - 60Å for conductive material such as CoWP. Other thicknesses are also useful. An additional dielectric layer 375 as shown in Fig. 3d can be formed over the etch stop layer 370. The dielectric layer, for example, serves as an additional ICD layer corresponding to an additional interconnect level. For example, conductive lines and contacts can be formed in the additional ICD layer.

[0037] The process continues to form the IC. For example, additional processing can include forming more ICD layers and interconnections, final passivation, dicing, assembly and packaging. Other processes are also useful.

[0038] Fig. 4 shows a cross-sectional view of another embodiment of a portion of an IC 400. As shown, the portion includes a substrate 405. The substrate, for example, comprises a silicon substrate. Other types of substrates, such as silicon germanium or SOI, are also useful. The substrate may include circuit components (not shown) such as transistors, capacitors, or resistors formed thereon. Other types of circuit components are also useful.

[0039] A dielectric layer 430 is disposed on the substrate. The dielectric layer, for example, serves as an ICD layer in which interconnections are formed. In one embodiment, the ICD includes lower and upper portions. The lower portion serves as an ILD layer while the upper portion serves as an IMD layer. The dielectric layer can be a single layer or multi-layered stack.

For example, a single layer can be used to serve as both the ILD and IMD or separate layers are used for the ILD and IMD. In some cases, an etch stop layer can be disposed between the ILD and IMD.

[0040] The dielectric layer can comprise, for example, silicon oxide. Other types of dielectric materials are also useful. For example, the dielectric layer can comprise doped silicon oxide such as FSG, undoped or doped silicate glasses such as BPSG and PSG, undoped or doped thermally grown silicon oxide, undoped or doped TEOS deposited silicon oxide, and low-k or ultra low-k dielectric materials such as OSG and FSG. Preferably, at least the IMD layer comprises a low-k or ultra low-k dielectric material.

[0041] Interconnect lines 450 are formed in the IMD portion of the ICD layer. The interconnect lines comprise a conductive material such as copper. Other types of metals, alloys or conductive materials are also useful. Contacts (not shown) can be provided in the ILD portion, connecting the interconnect lines to contact regions below. Depending on the ICD level, the contact regions can be other metal lines or devices, such as diffusion or gates of transistors. The conductive lines and contacts can comprise the same or different materials. The conductive lines and/or contacts can be provided with vertical or substantially vertical sidewalls. Providing conductive lines and/or contacts with slanted sidewalls is also useful.

[0042] The interconnect lines can include a barrier 455 lining sidewalls and bottoms thereof. The barrier prevents the diffusion of the conductive line material, for e.g. Cu, into the ICD layer. The barrier also serves as an adhesion layer for other conductive line material to better adhere to the dielectric material. The barrier, for example, can comprise tantalum nitride (TaN). Other types of barrier materials, such as tantalum, titanium nitride, ruthenium or a combination thereof, are also useful. A cap layer 458 can be provided over the interconnect lines to passivate the conductive lines. It may also be used as an adhesion layer for subsequent layers form thereon.

The cap layer may comprise cobalt tungsten phosphide (CoWP). Other types of capping materials, for example silicon nitride, are also useful.

[0043] In accordance with one embodiment, a top surface 432 of the ICD layer is disposed below top surfaces of the interconnect lines by a distance H. Providing the top surface of the ICD layer below the top surface of the interconnect line increases the effective distance between the interconnect lines. This has been found to increase the reliability of the dielectric layer by improving TDDB. In one embodiment, H is sufficient to improve TDDB. In one embodiment, H is about 250 - 450Å. Other values of H are also useful.

[0044] In one embodiment, an etch stop layer 470 is disposed over the surface of ICD layer. The etch stop layer covers the ICD and top of the interconnect lines. The etch stop layer, in one embodiment, comprises a dielectric material, such as silicon nitride. Other types of etch stop materials are also useful. The etch stop layer can also serve as a barrier layer to protect the interconnect lines from oxidation.

[0045] Fig. 5 shows a cross-sectional view of yet another portion of an IC 500. The portion, similar to the portion of Fig. 4, includes an ICD layer 430 with interconnects 450 disposed over a substrate 405, wherein a top surface 432 of the ICD layer is recessed below a top surface of the interconnect lines by a distance H. In one embodiment, an etch stop layer 470 is disposed over the surface of the ICD layer. The etch stop layer covers the ICD and top of the interconnect lines.

[0046] Above the ICD layer is disposed a dielectric layer 575. In one embodiment, the dielectric layer serves as another ICD layer of another interconnect level. For example, the first ICD layer 430 serves as the first interconnect level and the second ICD layer 575 serves as the second interconnect level. Additional ICD layers can be provided, corresponding to additional interconnect levels.

[0047] The second ICD layer 575, like the first ICD layer 430, includes lower and upper portions corresponding to ILD and ICD. Second ICD layer may comprise a single dielectric layer or multi-layered stack. Conductive lines 560 are disposed in the upper portion of the second ICD layer. Contacts 563 can be provided in the lower portion, for example, to couple the conductive lines in the second ICD layer to conductive lines or contact regions below. To ensure that the contacts are in electrical communication with the conductive lines below, they extend through the etch stop and cap layers. The conductive lines and contacts preferably comprise the same material. Providing conductive lines and contacts comprising different materials is also useful. The conductive lines and/or contacts can be provided with vertical or substantially vertical sidewalls. Providing conductive lines and/or contacts with slanted sidewalls is also useful.

[0048] The interconnect lines and contacts can include a barrier 565 lining sidewalls and bottoms thereof. The barrier, for example, can comprise TaN. Other types of barrier materials, such as tantalum, titanium nitride, ruthenium, are also useful. A cap layer can also be provided over the interconnect lines. The cap layer, for example, comprises CoWP. Other types of capping materials are also useful.

[0049] As shown, the top surface of the second ICD layer 575 is coplanar with the top surface of the conductive lines 560. In one embodiment, the top surface of the second ICD layer can be recessed similar to that of the first ICD layer. Additionally, an etch stop layer can be provided over the top surface of the second ICD layer and conductive lines. Furthermore, additional ICD layers can be provided over the second ICD layer corresponding to additional interconnect levels.

[0050] Figs. 6a-d show a process for forming an embodiment of a portion 600 of an IC. Referring to Fig. 6a, a substrate 605 is provided. The substrate, in one embodiment, comprises a p-type silicon substrate. Other types of substrates, such as a germanium-based, gallium arsenide,

SOI, or sapphire substrate, are also useful. The substrate can be prepared with circuit components (not shown). Circuit components can include, for example, transistors, capacitors and/or resistors. Other types of circuit components are also useful.

[0051] The substrate is further prepared with an ICD layer 630. The ICD layer includes an upper or IMD portion and a lower or ILD portion. The ICD can be a single layer or multi-layered stack. For example, a single layer can be used to serve as both the ILD and IMD or separate layers are used for the ILD and IMD. In some cases, an etch stop layer can be disposed between the ILD and IMD. The ICD layer can comprise, for example, silicon oxide. Other types of dielectric materials are also useful. For example, the dielectric layer can comprise doped silicon oxide such as FSG, undoped or doped silicate glasses such as BPSG and PSG, undoped or doped thermally grown silicon oxide, undoped or doped TEOS deposited silicon oxide, and low-k or ultra low-k dielectric materials such as OSG and FSG. Preferably, at least the IMD layer comprises a low-k or ultra low-k dielectric material.

[0052] The ICD layer or layers can be deposited using various types of deposition techniques. For example, CVD processes such as PECVD, HDCVD or APCVD can be used. Other techniques such as spin-on processes are also useful. The specific process, for example, can depend on the type of material used and application.

[0053] Conductive lines 650 and contacts (not shown) are formed in the IMD and ILD portions, respectively, of the ICD layer. The conductive lines and contacts can be formed from a conductive material, such as copper, aluminum, tungsten, alloys thereof or a combination thereof. Other types of conductive materials, including metals and alloys, such as Al doped Cu or Mn doped Cu, are also useful. The conductive lines and contacts can be formed using damascene or dual damascene processes. Other techniques, such as RIE, can also be useful. The conductive lines and contacts can be formed from the same material or from different materials.

The conductive lines and/or contacts can be provided with vertical or substantially vertical sidewalls. Providing conductive lines and/or contacts with slanted sidewalls is also useful.

[0054] A barrier 655 can be provided to line the conductive lines and/or contacts. The barrier, for example, can comprise TaN. Other types of barrier materials are also useful. The barrier can be formed by, for example, CVD. Other types of techniques for forming the barrier layer are also useful. To produce a planar top surface between the ICD and conductive lines, a planarizing process, such as chemical mechanical polish, can be employed. Other types of planarizing processes can also be useful.

[0055] A cap layer 658 is optionally formed over the surface of the conductive lines 650, as shown in Fig. 6b. The cap layer, for example, comprises CoWP. Other types of cap materials are also useful. The cap layer, for example, passivates the conductive lines. It can also serve as an adhesion layer for subsequent layers formed thereon. In one embodiment, the cap layer is formed by selective electroless plating. Other techniques for forming the cap layer are also useful.

[0056] Referring to Fig. 6c, the top surface 632 of the ICD layer is recessed by H to produce a stepped topography. The top surface 632, in one embodiment, is recessed sufficiently to improve TDDB. In one embodiment, H is about 250 - 450Å. Other values of H are also useful. In one embodiment, the top surface of the ICD is recessed by over polishing during the CMP step. For example, the top surface is over-buffed to recess it. Alternatively, a RIE can be performed to remove the ICD selective to the conductive lines. The cap layer, for example, protects the copper from damage during RIE. Employing both over-polishing and RIE to form the recess can also be useful. Other techniques for forming the stepped topography are also useful.

[0057] Referring to Fig. 6d, an etch stop layer 670 is deposited on the substrate, covering the top of the ICD and conductive lines. In one embodiment, the etch stop layer comprises

silicon nitride. The etch stop layer can comprise a conductive layer, for example a metal layer such as CoWP or a composite of dielectric and metal material layers. The etch stop layer, for example, is deposited by CVD or electroless-plating. Other techniques for depositing the etch stop layer is also useful. The thickness of the etch stop layer is about 350 - 450 Å for dielectric material such as silicon nitride or 40 - 60Å for metallic material such as CoWP. Other thicknesses are also useful. An additional ICD layer 675 can be formed over the etch stop layer 670 corresponding to an additional interconnect level. For example, conductive lines and contacts can be formed in the additional ICD layer 675.

[0058] The process continues to form the IC. For example, additional processing can include forming more ICD layers and interconnections, final passivation, dicing, assembly and packaging. Other processes are also useful.

[0059] The invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. The foregoing embodiments, therefore, are to be considered in all respects illustrative rather than limiting the invention described herein. Scope of the invention is thus indicated by the appended claims, rather than by the foregoing description, and all changes that come within the meaning and range of equivalency of the claims are intended to be embraced therein.

What is claimed is:

CLAIMS

1. A semiconductor device comprising:

a dielectric layer;

a conductive line in an upper portion of the dielectric layer, wherein a top surface of the dielectric layer is non-coplanar with a top surface of the conductive line, thereby forming a stepped topography; and

a conformal etch stop/cap layer covering and directly contacting the top surface of the dielectric layer and the top surface of the conductive line thereby covering and maintaining the stepped topography, wherein the stepped topography is configured to increase effective distance between conductive lines, to enhance interconnect reliability.

2. The semiconductor device of claim 1 wherein the top surface of the dielectric layer is lower than the top surface of the conductive line.

3. The semiconductor device of claim 1 wherein the top surface of the dielectric layer is lower than the top surface of the conductive line by a distance H, to improve time dependent dielectric breakdown (TDDB).

4. The semiconductor device of claim 3 wherein the distance H is about 250 – 450 Å.

5. The semiconductor device of claim 1 wherein the top surface of the dielectric layer is higher than the top surface of the conductive line.

6. The semiconductor device of claim 1 wherein the top surface of the dielectric layer is higher than the top surface of the conductive line by a distance H, to improve time dependent dielectric breakdown (TDDB).

7. The semiconductor device of claim 6 wherein the distance H is about 250 – 450 Å.

8. The semiconductor device of claim 1 further comprising a barrier lining sidewalls and bottom of the conductive line.

9. The semiconductor device of claim 1 wherein a top of the conformal etch stop/cap layer over the dielectric layer is non-coplanar with a top of the conformal dielectric etch stop/cap layer over the conductive line.

10. The semiconductor device of claim 1 further comprising a second dielectric layer on top of the conformal etch stop/cap layer;

wherein the second dielectric layer comprises a second conductive line and a contact; and

wherein the contact couples the second conductive line of the second dielectric layer to the first conductive line below.

11. The semiconductor device of claim 1 wherein the conformal etch stop/cap layer contacts the conductive line.

12. A semiconductor device comprising:

a dielectric layer;

a conductive line in an upper portion of the dielectric layer, wherein a top surface of the dielectric layer is non-coplanar with a top surface of the conductive line, thereby forming a stepped topography; and

a conformal etch stop/cap layer covering the stepped topography, wherein a top of the conformal etch stop/cap layer over the dielectric layer is non-coplanar with a top of the conformal etch stop/cap layer over the conductive line, the conformal etch stop/cap layer directly contacting the conductive line and the dielectric layer, wherein the stepped topography is configured to increase the effective distance between conductive lines to enhance interconnect reliability.

13. The semiconductor device of claim 12 wherein the top surface of the dielectric layer is higher than the top surface of the conductive line by a distance H, to improve time dependent dielectric breakdown (TDDB).

14. The semiconductor device of claim 13 wherein the distance H is about 250 – 450 Å.

15. The semiconductor device of claim 12 wherein the top surface of the dielectric layer is lower than the top surface of the conductive line by a distance H, to improve time dependent dielectric breakdown (TDDB).

16. The semiconductor device of claim 15 wherein the distance H is about 250 – 450 Å.

17. The semiconductor device of claim 12 further comprising a barrier lining sidewalls and bottom of the conductive line.

18. The semiconductor device of claim 12 wherein the conformal etch stop/cap layer comprises a dielectric layer.

19. The semiconductor device of claim 12 further comprising a second dielectric layer on top of the conformal etch stop/cap layer;

wherein the second dielectric layer comprises a second conductive line and a contact; and

wherein the contact couples the second conductive line of the second dielectric layer to the first conductive line below.

20. The semiconductor device of claim 19 further comprising a second cap layer between the conformal etch stop/cap layer and the top surface of the first conductive line.