

ABSTRACT OF THE DISCLOSURE

CLOCK ENABLE CIRCUIT FOR USE IN A HIGH SPEED REPROGRAMMABLE DELAY LINE INCORPORATING 5 GLITCHLESS ENABLE/DISABLE FUNCTIONALITY

A clock qualification circuit (50) used to selectively enable a clock edge to transfer
new delay data from a first-in-first-out (FIFO) circuit (14) in a precision delay line circuit
(11). The circuit (50) qualifies the clock without generating undesirable pulses (glitches)
10 and causing false loading of new delay data in a timing on the fly delay line
implementation.

Figure 4