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ABSTRACT

SEMICONDUCTOR PACKAGE HAVING INCREASED SOLDER JOINT STRENGTH

A packaged semiconductor having increased solder joint strength. The packaged semiconductor includes a semiconductor chip and a plurality of bond pads on the semiconductor chip. A leadframe includes a chip paddle, a plurality of tie bars connected to corners of the chip paddle and a plurality of dam bars. A plurality of leads connect to the leadframe, and are radially formed at regular intervals along and spaced apart from the chip paddle, and extend towards the chip paddle. A plurality of conductive wires electrically connect the leads and the semiconductor chip. Encapsulation material encapsulates the semiconductor chip, wires, chip paddle, and leads to form a package body, wherein dam bars formed on the leadframe limit flow of the encapsulation material. The chip paddle, plurality of leads and plurality of tie bars are externally exposed at peripheral side and bottom surfaces to allow depressions to be formed thereon. In one embodiment, at least one depression is formed on the bottom surface of at least one of the tie bars. In a second embodiment, at least one depression is formed on the bottom surface of the chip paddle. In a third embodiment, at least one of the leads has at least one depression formed on the bottom surface of the respective lead. The depressions may also be formed on the chip paddle, leads and tie bars simultaneously, or in combination to increase the friction required to readily maintain a sufficient solder joint strength when the package is mounted to a motherboard.

FIGURE 1