WHAT IS CLAIMED IS:

1. A semiconductor memory device, comprising:

horizontal patterns disposed on a peripheral circuit structure and spaced apart from each other in a first direction;

memory structures disposed on the horizontal patterns, the memory structures comprising source structures and electrode structures;

a division structure disposed between adjacent horizontal patterns in the first direction, the division structure configured to separate the source structures of adjacent memory structures from each other; and

an etch stop pattern disposed between the horizontal patterns and disposed at a level lower than a level of the source structures, the etch stop pattern connected to a lower portion of the division structure,

wherein the etch stop pattern comprises a first sub-pattern extending in the first direction and a second sub-pattern extending in a second direction crossing the first direction.

2. The semiconductor memory device of claim 1, wherein:

each of the horizontal patterns comprises a first edge parallel to the first direction and a second edge parallel to the second direction;

the first sub-pattern is extended along the first edge; and

the second sub-pattern is extended along the second edge.

3. The semiconductor memory device of claim 2, wherein:

the first sub-pattern comprises a plurality of first sub-patterns;

the second sub-pattern comprises a plurality of second sub-patterns; and

the etch stop pattern has a grid shape formed by the plurality of first sub-patterns and the plurality of second sub-patterns crossing each other.

4. The semiconductor memory device of any one of claims 1 to 3, wherein the etch stop pattern is formed of a non-metallic material having an etch selectivity with respect to a silicon oxide layer and a silicon nitride layer.

5. The semiconductor memory device of any one of claims 1 to 4, wherein the etch stop pattern comprises polysilicon.

6. The semiconductor memory device of any one of claims 1 to 5, wherein a width of the etch stop pattern in the first direction is greater than a width of the division structure in the first direction.

7. The semiconductor memory device of any one of claims 1 to 6, wherein a width of the etch stop pattern in the second direction is greater than a width of the division structure in the second direction.

8. The semiconductor memory device of any one of claims 1 to 7, wherein the division

structure has a bar or rectangular shape.

9. The semiconductor memory device of any one of claims 1 to 8, wherein a top surface of the etch stop pattern is positioned at a level lower than bottom surfaces of the horizontal patterns.

10. The semiconductor memory device of any one of claims 1 to 8, wherein:

a top surface of the etch stop pattern is positioned at a same level as top surfaces of the horizontal patterns; and

a bottom surface of the etch stop pattern is positioned at a same level as bottom surfaces of the horizontal patterns.

11. The semiconductor memory device of any one of claims 1 to 10, further comprising:

remaining mold patterns disposed between adjacent horizontal patterns in the first direction and between the source structures and the etch stop pattern in a direction of a thickness of the semiconductor memory device,

wherein the division structure is configured to separate the remaining mold patterns in the first direction.

12. The semiconductor memory device of claim 11, wherein:

the source structures comprise first conductive source patterns disposed on the horizontal patterns and second conductive source patterns disposed between the first

conductive source patterns and the horizontal patterns, and

the second conductive source patterns are positioned at a same level as a level of the remaining mold patterns.

13. The semiconductor memory device of claim 12, wherein top surfaces of the remaining mold patterns are in contact with bottom surfaces of the first conductive source patterns.

14. The semiconductor memory device of claim 12 or 13, wherein:

sidewalls of the second conductive source patterns are disposed on the horizontal patterns; and

sidewalls of the first conductive source patterns are in contact with sidewalls of the division structure.

15. The semiconductor memory device of any one of claims 1 to 14, further comprising:

penetration plugs connecting the memory structures to the peripheral circuit structure,

wherein the penetration plugs are spaced apart from the etch stop pattern and the division structure in the first direction.

16. The semiconductor memory device of claim 15, wherein a bottom surface of the division structure is positioned at a level higher than bottom surfaces of the penetration plugs.

17. The semiconductor memory device of any one of claims 1 to 16, wherein a thickness of the etch stop pattern is in a range of about 800 Å to about 2000 Å.

18. A semiconductor memory device, comprising:

horizontal patterns disposed on a peripheral circuit structure and spaced apart from each other with a division region interposed therebetween in a first direction, the division region including a first insulating penetration layer;

memory structures disposed on the horizontal patterns, the memory structures comprising source structures and electrode structures on the source structures;

vertical structures penetrating the electrode structures and connected to the source structures;

a division structure disposed in the division region, the division structure configured to separate the source structures of adjacent memory structures from each other;

an etch stop pattern disposed between the horizontal patterns and disposed at a level lower than a level of the horizontal patterns, the etch stop pattern connected to a lower portion of the division structure, wherein the etch stop pattern comprises a first sub-pattern extending in the first direction and a second sub-pattern extending in a second direction crossing the first direction; and

penetration plugs configured to connect the memory structures to the peripheral circuit structure,

wherein the source structures comprise first conductive source patterns disposed on

the horizontal patterns and second conductive source patterns disposed between the first conductive source patterns and the horizontal patterns, and

the first conductive source patterns extend to the division region and are connected to sidewalls of the division structure.

19. The semiconductor memory device of claim 18, further comprising:

remaining mold patterns disposed between the first conductive source patterns and the first insulating penetration layer and at a same level as the second conductive source patterns,

wherein the division structure separates the remaining mold patterns in a horizontal direction.