WHAT IS CLAIMED IS:

1. An integrated circuit device, comprising:

a gate stack structure on a base layer, the gate stack structure including:

a gate insulating layer, the gate insulating layer including a first dielectric layer on the base layer and having first relative permittivity, and

a gate structure on the gate insulating layer; and

a gate spacer structure on opposite side walls of the gate stack structure and on the base layer, the gate spacer structure including a buried dielectric layer buried in a recess hole of the gate insulating layer at a lower portion of the gate spacer structure on the base layer, and the buried dielectric layer including a same material as the first dielectric layer,

wherein the gate insulating layer further includes a second dielectric layer on the first dielectric layer and having second relative permittivity greater than the first relative permittivity, and

the first dielectric layer includes a sub-dielectric layer and an interface layer, and the interface layer is formed between the sub-dielectric layer and the second dielectric layer.

2. The integrated circuit device as claimed in claim 1, wherein:

the base layer includes at least one of a semiconductor substrate and a semiconductor layer, and a memory cell area and a peripheral circuit area on the at least one of the semiconductor substrate and the semiconductor layer, and

the gate insulating layer, the gate structure, and the gate spacer structure are in the peripheral circuit area.

3. The integrated circuit device as claimed in claim 1 or claim 2, wherein the first dielectric layer has a greater thickness than the second dielectric layer.

4. The integrated circuit device as claimed in any one of claims 1 to 3, wherein each of the first dielectric layer and the buried dielectric layer includes a silicon oxide layer.

5. The integrated circuit device as claimed in any one of claims 1 to 4, wherein the gate structure has a metal gate structure including a metal layer.

6. The integrated circuit device as claimed in any one of claims 1 to 5, wherein the gate structure includes a work function control layer, a first gate layer, and a second gate layer sequentially positioned on the gate insulating layer.

7. The integrated circuit device as claimed in any one of claims 1 to 6, wherein the gate spacer structure includes:

a first spacer on opposite side walls of the gate structure, the first spacers including a third dielectric layer having third relative permittivity greater than the first relative permittivity, and having a linear bar shape;

a second spacer on a side wall of the first spacer, on a side wall of the buried dielectric layer, and on the base layer, the second spacer being integral with the buried dielectric layer in an L-shape, and including a same material as the buried dielectric layer;

a third spacer on a side wall and on an upper portion of the second spacer, the third spacer including a same material as the first spacer, and having an L-shape; and

a fourth spacer on a side wall and on an upper portion of the third spacer, the fourth spacer including a same material as the second spacer.

8. The integrated circuit device as claimed in claim 7, wherein each of the first spacer and the third spacer includes a silicon nitride layer, and each of the buried dielectric layer, the second spacer, and the fourth spacer includes a silicon oxide layer.

9. The integrated circuit device as claimed in any one of claims 1 to 6, wherein the gate spacer structure includes:

a first spacer on both opposite walls of the gate structure, including a third dielectric layer having third relative permittivity greater than the first relative permittivity, and having a linear bar shape;

a second spacer on a side wall of the first spacer and on a side wall of the buried dielectric layer, integral with the buried dielectric layer in a linear bar shape, and including a same material as the buried dielectric layer;

a third spacer on a side wall of the second spacer and on the base layer, including a same material as the first spacer, and having an L-shape; and

a fourth spacer on a side wall and on an upper portion of the third spacer, and including a same material as the second spacer.

10. The integrated circuit device as claimed in claim 9, wherein each of the first spacer and the third spacer includes a silicon nitride layer, and each of the buried dielectric layer, the second spacer, and the fourth spacer includes a silicon oxide layer.

11. The integrated circuit device as claimed in any one of claims 1 to 6, wherein the gate spacer structure includes:

a first spacer on opposite side walls of the gate structure, including a third dielectric layer having third relative permittivity greater than the first relative permittivity, and having a linear bar shape;

a second spacer on a side wall of the first spacer, on a side wall of the buried dielectric layer, and on the base layer, including a same material as the first spacer, and having an L-shape; and

a third spacer on a side wall and on an upper portion of the second spacer, and including a same material as the buried dielectric layer.

12. The integrated circuit device as claimed in claim 11, wherein each of the first spacer and the second spacer includes a silicon nitride layer, and each of the buried dielectric layer and the third spacer includes a silicon oxide layer.

13. An integrated circuit device, comprising:

a gate stack structure including:

a gate insulating layer, the gate insulating layer having a first dielectric layer on a base layer and having first relative permittivity, and a second dielectric layer on the first dielectric layer and having second relative permittivity greater than the first relative permittivity, and

a gate structure on the gate insulating layer, the gate structure including a metal layer; and

a gate spacer structure on opposite side walls of the gate stack structure and on the base layer, the gate spacer structure including:

a first spacer on opposite side walls of the gate structure, including a third dielectric layer having third relative permittivity greater than the first relative permittivity, and having a linear bar shape,

a second spacer including a buried dielectric layer buried in a recess hole in the first dielectric layer, the second spacer including a same material as the first dielectric layer at a lower portion of the first spacer, on a side wall of the first spacer and a side wall of the buried dielectric layer, integrally disposed with the buried dielectric layer, and including a same material as the buried dielectric layer,

a third spacer on a side wall of the second spacer, including a same material as the first spacer, and having an L shape, and

a fourth spacer on a side wall and an upper portion of the third spacer and including a same material as the second spacer,

wherein the first dielectric layer includes a sub-dielectric layer and an interface layer, and the interface layer is formed between the sub-dielectric layer and the second dielectric layer.

14. The integrated circuit device as claimed in claim 13, wherein the second spacer is connected to the buried dielectric layer and is on the base layer so that the second spacer has an L shape, and the third spacer is on the second spacer on the base layer.

15. The integrated circuit device as claimed in claim 13, wherein the second spacer is on a side wall of the first spacer and on a side wall of the buried dielectric layer in a linear bar shape, and the third spacer is on a side wall of the second spacer and on the base layer.

16. The integrated circuit device as claimed in any one of claims 13 to 15, wherein each of the first spacer and the third spacer includes a silicon nitride layer, and each of the first dielectric layer, the buried dielectric layer, the second spacer, and the fourth spacer includes a silicon oxide layer.

17. The integrated circuit device as claimed in any one of claims 13 to 16, wherein a width of the fourth spacer is greater than widths of the first spacer and the third spacer.

18. An integrated circuit device, comprising:

a gate stack structure including a gate insulating layer and a gate structure on the gate insulating layer, the gate insulating layer including a first dielectric layer on a base layer and having first relative permittivity and a second dielectric layer on the first dielectric layer and having second relative permittivity greater than the first relative permittivity, and the gate structure including a metal layer; and

a gate spacer structure on opposite side walls of the gate stack structure on the base layer, the gate spacer structure including:

a first spacer on opposite side walls of the gate structure, including a third dielectric layer having third relative permittivity greater than the first relative permittivity, and having a linear bar shape,

a buried dielectric layer buried in a recess hole in the first dielectric layer and having a same material as the first dielectric layer at a lower portion of the first spacer,

a second spacer on a side wall of the first spacer and a side wall of the buried dielectric layer and the base layer, and including a same material as the first spacer, and

a third spacer on a side wall and an upper portion of the second spacer, and including a same material as the buried dielectric layer,

wherein the first dielectric layer includes a sub-dielectric layer and an interface layer, and the interface layer is formed between the sub-dielectric layer and the second dielectric layer.

19. The integrated circuit device as claimed in claim 18, wherein:

each of the first spacer and the second spacer includes a silicon nitride layer,

each of the first dielectric layer, the buried dielectric layer, and the third spacer includes a silicon oxide layer, and

a width of the third spacer is greater than widths of the first spacer and the second spacer.