MEMORY

CROSS-REFERENCE

[0001] The present disclosure claims priority to Chinese Patent Application No. 202411689800.9 filed with China National Intellectual Property Administration on November 22, 2024, and entitled “MEMORY”, the content of which is incorporated herein by reference in its entirety.

TECHNICAL FIELD

[0002] Embodiments of the present disclosure relate to the field of semiconductors, and in particular, to a memory.

BACKGROUND

[0003] In memory design, especially in the design of a dynamic random access memory (Dynamic Random Access Memory, DRAM), how to increase the density of memory cells in a memory is a problem that has attracted much attention. There are generally two ways to increase the density of the memory cells in the memory. One is to reduce the area of the control circuit corresponding to the memory cells of the same capacity, and the other is to increase the number of memory cells corresponding to a unit control circuit. The former is advantageous for reducing the overall size of a chip due to the reduction in the area of the control circuit, thereby increasing the number of complete dies that can be successfully processed and finally cut on each wafer.

SUMMARY

[0004] Embodiments of the present disclosure provide a memory, which is at least beneficial to improving the storage efficiency of the memory.

[0005] According to some embodiments of the present disclosure, in one aspect, the embodiments of the present disclosure provide a memory. The memory at least includes: a memory array, where the memory array includes a plurality of word lines; and a word line

contact structure, including a first word line contact structure and a second word line contact structure located on opposite sides of the memory array, where the first word line contact structure is configured to be connected to a first word line driver, the second word line contact structure is configured to be connected to a second word line driver, and each of the plurality of word lines in the memory array is driven by both the first word line driver and the second word line driver.

[0006] In some embodiments, each of the plurality of word lines is provided with a first end and a second end opposite to each other, the first end of at least one of the plurality of word lines is directly connected to the first word line contact structure, and the second end is directly connected to the second word line contact structure.

[0007] In some embodiments, the at least one word line includes two word lines connected end to end, and the two word lines connected end to end form a closed ring surrounding a memory cell.

[0008] In some embodiments, each memory array includes a plurality of memory rows, all memory cells in a same memory row share a same word line, adjacent memory rows in a same memory array are connected to different local bit lines, and at least two adjacent word lines are simultaneously connected to the first word line contact structure and the second word line contact structure.

[0009] In some embodiments, the plurality of word lines extend in a first horizontal direction, and all word lines simultaneously connected to the first word line contact structure and the second word line contact structure are continuously arranged in a second horizontal direction, the second horizontal direction being perpendicular to the first horizontal direction and a vertical direction.

[0010] In some embodiments, each memory array includes a plurality of memory rows, all memory cells in a same memory row share a same word line, and every two memory cells arranged in a second horizontal direction share one local bit line, the second horizontal direction being perpendicular to the first horizontal direction; the word line contact structure further includes: a third word line contact structure and a fourth word line contact structure, where the first word line contact structure, the second word line contact structure, the third word line contact structure, and the fourth word line contact structure correspond to a same memory array, the third word line contact structure is configured to be connected to a third word line driver, the fourth word line contact structure is configured to be connected to a fourth word line driver, the first word line contact structure and the third word line contact structure are located on a same side of the corresponding memory array, the second word line

contact structure and the fourth word line contact structure are located on a same side of the corresponding memory array, the third word line contact structure and the fourth word line contact structure are oppositely arranged, and adjacent word lines corresponding to a same local bit line are connected to different word line contact structures on the same side.

[0011] In some embodiments, the memory includes a plurality of layers of memory arrays vertically stacked, and different memory cells vertically stacked share the local bit line extending in a vertical direction, the vertical direction being perpendicular to the first horizontal direction.

[0012] In some embodiments, in adjacent word lines corresponding to a same set of local bit lines, one of the adjacent word lines is connected to the word line contact structure only at one end, and the other is connected to two opposite word line contact structures at two ends, respectively.

[0013] In some embodiments, the memory array is provided with an edge word line, the edge word line and an adjacent word line correspond to different local bit lines, and the edge word line and the adjacent word line are at least connected to a same word line contact structure.

[0014] In some embodiments, the edge word line and the adjacent word line are simultaneously connected to two opposite word line contact structures.

BRIEF DESCRIPTION OF DRAWINGS

[0015] One or more embodiments are illustrated by images in corresponding drawings, and these exemplary explanations are not to be construed as limiting the embodiments. Unless expressly stated otherwise, the images in the drawings do not constitute a proportion limitation.

[0016] FIG. 1 is a schematic diagram of a connection relationship between a word line contact structure and a word line in a memory;

[0017] FIGS. 2 to 4 are schematic diagrams of connection relationships between word line contact structures and word lines in a memory according to an embodiment of the present disclosure; and

[0018] FIG. 5 is a schematic diagram of a relationship between a memory array and a memory block according to an embodiment of the present disclosure.

DESCRIPTION OF EMBODIMENTS

[0019] The embodiments of the present disclosure will be described in detail below with reference to the drawings. Those of ordinary skill in the art can understand that, in the embodiments of the present disclosure, numerous technical details are set forth in order to enable readers to better understand the present disclosure. However, the technical solutions claimed by the present disclosure can also be implemented even without these technical details and the various changes and modifications based on the following embodiments.

[0020] FIG. 1 is a schematic diagram of a connection relationship between a word line contact structure and a word line in a memory. Referring to FIG. 1, the memory includes: a memory array subMat, where the memory array subMat includes a plurality of word lines WL, the word lines WL extend in a first direction D1, and the plurality of word lines are arranged in a second direction D2, the second direction D2 being perpendicular to the first direction D1; and a word line contact structure, including a first word line contact structure SC1 and a second word line contact structure SC2 located on opposite sides of the memory array subMat, where the first word line contact structure SC1 is connected to a first word line driver SWD1, the second word line contact structure SC2 is connected to a second word line driver SWD2, the first word line contact structure SC1 is connected to odd word lines (indicated by dashed lines) in an adjacent memory array subMat, and the second word line contact structure SC2 is connected to even word lines (indicated by solid lines) in an adjacent memory array subMat. That is, the first word line driver SWD1 simultaneously drives odd word lines in two adjacent memory arrays subMat through the first word line contact structure SC1, and the second word line driver SWD2 simultaneously drives even word lines in two adjacent memory arrays subMat through the second word line contact structure SC2.

[0021] In the embodiment shown in FIG. 1, the memory array subMat includes four memory rows, each memory row corresponds to the same word line WL, each memory row includes N memory cells, and every two memory cells arranged in the second direction D2 share a bit line BL. Since each word line driver needs to drive two memory arrays simultaneously, for a certain memory array, it can be considered that only half of the driving capability of the first word line driver SWD1 and half of the driving capability of the second word line driver SWD2 are received. In other words, each memory array only receives the driving capability of one complete word line driver. In this case, the ratio of the number of memory cells in the memory array to the number of word line drivers (or the number of word line contact structures) that the memory array receives is 4N/1. This ratio represents the storage density and storage efficiency of the memory to a certain extent.

[0022] It should be noted that the number of memory cells included in each memory row is limited by the driving capability of the word line driver, or limited by the driving capability that the word line receives. The stronger the driving capability that the word line receives, the longer the length of the word line may be, and the larger the number of memory cells included in the memory rows sharing the same word line may be.

[0023] FIGS. 2 to 4 are schematic diagrams of connection relationships between word line contact structures and word lines in a memory according to an embodiment of the present disclosure.

[0024] Referring to FIGS. 2 to 3, the memory includes: a memory array subMat, where the memory array subMat includes a plurality of word lines WL; and a word line contact structure SC, including a first word line contact structure SC1 and a second word line contact structure SC2 located on opposite sides of the memory array subMat, where the first word line contact structure SC1 is configured to be connected to a first word line driver SWD1, the second word line contact structure SC2 is configured to be connected to a second word line driver SWD2, and each word line WL in the memory array subMat is driven by both the first word line driver SWD1 and the second word line driver SWD2.

[0025] In the embodiments of the present disclosure, by controlling each word line WL to be driven by both the first word line driver SWD1 and the second word line driver SWD2 located on opposite sides of the memory array subMat, compared to the word line being driven by only one word line driver, this helps to extend the length of the word line WL, ensure that a longer word line can also be effectively driven, and increase the number of memory cells sharing the same word line, thereby increasing the storage density of the memory.

[0026] The embodiments of the present disclosure are described in more detail below with reference to the drawings. It can be understood that the drawings show merely some embodiments included in the present disclosure, and cannot be used to limit the actual protection scope of the present disclosure. In addition, in FIGS. 2, 3, and 4, word lines are represented in two forms of solid lines and dashed lines, which are merely for clarity of comparison and do not represent odd word lines and even word lines.

[0027] In the embodiments of the present disclosure, the memory further includes word line drivers, and the word line drivers are in one-to-one correspondence with the word line contact structures. The word line driver drives the word line connected to the word line contact structure through the corresponding word line contact structure. Therefore, the connection between the word line and the word line contact structure represents that the word line is driven by the word line driver connected to the word line contact structure. The word line

driver can control the electric potential state of the word line by outputting a high level or a low level, thereby pulling the electric potential of the word line up or down.

[0028] It should be noted that "connection" in the present disclosure includes a direct connection and an indirect connection, and the indirect connection includes a complete indirect connection and a partial indirect connection. In a direct connection scenario, the word line may be connected to the word line contact structure through an endpoint position or a non-endpoint position. In an indirect connection scenario, a certain word line may be indirectly connected to the word line contact structure through another word line. The complete indirect connection means that the word line itself is not directly connected to any word line contact structure, but is completely indirectly connected through another word line. The partial indirect connection means that the word line is directly connected to some word line contact structures and indirectly connected to some other word line contact structures, which is equivalent to the simultaneous existence of the direct connection and the partial connection.

[0029] In the embodiment shown in FIG. 2, the memory array subMat is provided with a first word line WL1. A first end T1 of the first word line WL1 is connected to the first word line contact structure SC1, and a second end T2 is connected to the second word line contact structure SC2; that is, the first word line WL1 is directly connected to the first word line contact structure SC1 and the second word line contact structure SC2 through different endpoints. In the embodiment shown in FIG. 3, the memory array is provided with a first word line WL1 and a second word line WL2. A first end T1 of the first word line WL1 is connected to the first word line contact structure SC1 and is connected to a first end T1 of the second word line WL2, and a second end T2 of the second word line WL2 is connected to the second word line contact structure SC2; that is, the first word line WL1 is directly connected to the first word line contact structure SC1 through an endpoint position and is indirectly connected to the second word line contact structure SC2 through the second word line WL2, and the second word line WL2 is directly connected to the first word line contact structure SC1 and the second word line contact structure SC2 through different endpoints.

[0030] In the embodiments of the present disclosure, the first word line contact structure SC1 and the second word line contact structure SC2 are merely general terms representing two word line contact structures SC located on opposite sides of any one memory array subMat, rather than referring to a specific word line contact structure SC. Word line contact structures are disposed on opposite sides of each non-edge memory array, or word line contact structures are disposed between adjacent memory arrays. In the discussion of the connection

relationship between a word line and an adjacent word line contact structure in any one memory array, the word line contact structures on opposite sides thereof may be defined as the first word line contact structure and the second word line contact structure.

[0031] The word line contact structure and the corresponding word line driver may be on the same wafer or on different wafers. When the word line contact structure and the word line driver are on different wafers, the two wafers may be manufactured separately and then connected together by hybrid bonding or the like.

[0032] In some embodiments, when the memory reads and writes data, a plurality of memory blocks arranged in the extension direction of the word line may be turned on at one time, and each memory block outputs part of the data. Referring to FIG. 5, at least part of the memory blocks (e.g., a first memory block Mat1 and a second memory block Mat2) are arranged in the extension direction of the word line, each memory block includes N memory arrays sub Mat (subMat1 to subMatN), and the arrangement direction of the memory arrays subMat is perpendicular to the extension direction of the word line. A word line contact region SCR may be provided between adjacent memory blocks, and the word line contact structures SC shown in FIGS. 2 to 4 are disposed in the word line contact region SCR.

[0033] In some embodiments, in the memory array subMat, each word line WL is provided with a first end and a second end opposite to each other, the first end of at least one word line WL is directly connected to the first word line contact structure SC1, and the second end is directly connected to the second word line contact structure SC2. This helps to prevent the electric potential at an end, distal to the word line contact structure SC, of the word line WL from being pulled up or down slowly, or even failing to be pulled to a preset level, thereby ensuring that the electric potential at any position of at least part of the word line WL can be adjusted in time and ensuring that the data access path of the memory cell is turned on or off in time.

[0034] In the embodiment shown in FIG. 2, the first ends T1 of the first word line WL1, the second word line WL2, and the third word line WL3 are all directly connected to the first word line contact structure SC1, and the second ends T2 are all directly connected to the second word line contact structure SC2. In the embodiment shown in FIG. 3, the first end T1 of the second word line WL2 is directly connected to the first word line contact structure SC1, and the second end T2 is directly connected to the second word line contact structure SC2. In the embodiment shown in FIG. 4, the first ends T1 of the first word line WL1 and the second word line WL2 are both directly connected to the first word line contact structure SC1, and the second ends T2 are both directly connected to the second word line contact structure SC2.

[0035] It should be noted that, with respect to the case that a certain end of each of the two or more word lines is directly connected to a certain word line contact structure, it may be that certain segments of a plurality of word lines are connected together first and then connected to the word line contact structure through a common connection point, or may be that different word lines are connected to the word line contact structure, separately. The former is illustrated as an example in the embodiments shown in FIGS. 2 to 4.

[0036] In some embodiments, the storage structure includes at least two word lines connected end to end. The two word lines connected end to end form a closed ring surrounding a memory cell, and first ends of the two word lines connected end to end are both directly connected to the first word line contact structure, and second ends are both directly connected to the second word line contact structure. The two word lines being connected end to end means that the first ends of the two word lines are connected to each other and the second ends of the two word lines are connected to each other. This helps to further balance the driving capability of the word line driver for different word lines and ensure that different positions of each word line can be effectively driven.

[0037] In the embodiment shown in FIG. 2, the second word line WL2 and the third word line WL3 are connected end to end to form a closed ring surrounding the memory cell, and further form a closed ring surrounding at least one memory row. In the embodiment shown in FIG. 4, the first word line WL1 and the second word line WL2 are connected end to end to form a closed ring surrounding the memory cell, and further form a closed environment surrounding at least one memory row. “Surrounding” means that in the vertical direction Z, the projection of two word lines connected end to end surrounds the projection of the memory cell. The memory cell refers to a device configured to store data information, such as a storage capacitor, a storage resistor, and the like, and does not include an access transistor whose switch is controlled by a word line.

[0038] It should be noted that only the second word line WL2 and the third word line WL3 in FIG. 2 and the first word line WL1 and the second word line WL2 in FIG. 4 are taken as examples for description here. In fact, in the memory arrays shown in FIGS. 2 and 4, other word line pairs connected end to end may form a closed ring surrounding the memory cell.

[0039] In some embodiments, each memory array subMat includes a plurality of memory rows, all memory cells in the same memory row share the same word line WL, adjacent memory rows in the same memory array are connected to different local bit lines LBL, and at least two adjacent word lines are simultaneously connected to the first word line contact structure SC1 and the second word line contact structure SC2.

[0040] Further, the word line WL extends in a first horizontal direction X, and all word lines WL simultaneously connected to the first word line contact structure SC1 and the second word line contact structure SC2 are continuously arranged in a second horizontal direction Y, the second horizontal direction Y being perpendicular to the first horizontal direction X.

[0041] Referring to FIG. 2, the first word line WL1, the second word line WL2, and the third word line WL3 are continuously arranged in the second horizontal direction Y. The first word line WL1 is adjacent to the second word line WL2, and the second word line WL2 is adjacent to the third word line WL3. The first ends of the first word line WL1, the second word line WL2, and the third word line WL3 are all connected to the first word line contact structure SC1, and the second ends are all connected to the second word line contact structure SC2.

[0042] In the embodiment shown in FIG. 2, the word line contact structure further includes a third word line contact structure SC3 and a fourth word line contact structure SC4, and a plurality of memory rows are disposed between the third word line contact structure SC3 and the fourth word line contact structure SC4. It can be considered that the memory cells located between the first word line contact structure SC1 and the second word line contact structure SC2 form one memory array, and the memory cells located between the third word line contact structure SC3 and the fourth word line contact structure SC4 form another memory array, or it can be considered that the memory cells located between the first word line contact structure SC1 and the second word line contact structure SC2 and the memory cells located between the third word line contact structure SC3 and the fourth word line contact structure SC4 jointly form one memory array. In the subsequent description of the embodiment shown in FIG. 2, the latter is taken as an example, and the whole formed by the memory cells located between the first word line contact structure SC1 and the second word line contact structure SC2 is denoted as a first memory sub-array, and the whole formed by the memory cells located between the third word line contact structure SC3 and the fourth word line contact structure SC4 is denoted as a second memory sub-array.

[0043] As can be seen from FIG. 2, the connection relationship between the word line and the adjacent word line contact structure in the second memory sub-array is the same as the connection relationship between the word line and the adjacent word line contact structure in the first memory sub-array, and the status of the second memory sub-array can be completely equivalent to the status of the first memory sub-array without interaction. The first ends of all the word lines in the second memory sub-array may be connected to each other and connected to the first word line contact structure SC1, and the second ends may be connected to each other and connected to the second word line contact structure SC2.

[0044] Since the three word lines in each of the first memory sub-array and the second memory sub-array are activated simultaneously, but the word lines in the first memory sub-array and the word lines in the second memory sub-array are not activated at the same time, the local bit lines of the first memory sub-array cannot be connected to the same shared bit line CBL, but can only be connected to the same shared bit line CBL of the local bit lines in the second memory sub-array. For example, the first memory cell of the first memory row in the first memory sub-array and the first memory cell of the first memory row in the second memory sub-array are simultaneously connected to the first shared bit line CBL1. For example, the first memory cell of the second memory row in the first memory sub-array and the first memory cell of the second memory row in the second memory sub-array are simultaneously connected to the second shared bit line CBL2. For example, the first memory cell of the third memory row in the first memory sub-array and the first memory cell of the third memory row in the second memory sub-array are simultaneously connected to the third shared bit line CBL3.

[0045] In some embodiments, the shared bit line CBL may be connected to a bit line amplifier, the bit line amplifier being configured to sense and amplify a voltage difference between the shared bit line CBL and the reference shared bit line.

[0046] In addition, in the embodiment shown in FIG. 2, the memory cells disposed at the outermost periphery of the memory array are valid memory cells that operate normally, i.e., capable of storing data information. In the embodiments shown in FIGS. 3 and 4, the memory cells disposed at the outermost periphery of the memory array are dummy cells or dummy access transistors, so as to prevent the local bit lines from being located at the outermost side of the memory array, which would otherwise cause crosstalk of signals of the local bit lines between adjacent memory arrays in the second horizontal direction Y, thereby ensuring the stability of data transmission. Meanwhile, the bit lines are relatively fragile, and providing the dummy cells or the dummy access transistors at the outermost periphery helps to avoid damage to the local bit lines. The size of the dummy cell is generally the same as the size of a normal memory cell, except that the dummy cell does not have a data storage function. The size of the dummy access transistor is generally the same as the size of a conventional access transistor, except that the dummy access transistor does not have a data transmission function. The word line is configured to control the turn-on and turn-off of the conventional access transistor.

[0047] In some embodiments, referring to FIGS. 3 and 4, each memory array includes a plurality of memory rows, all memory cells in the same memory row share the same word

line, and every two memory cells arranged in the second horizontal direction Y share one local bit line LBL, the second horizontal direction Y being perpendicular to the first horizontal direction X (i.e., the extension direction of the word line). The word line contact structure further includes: a third word line contact structure SC3 and a fourth word line contact structure SC4, where the first word line contact structure SC1, the second word line contact structure SC2, the third word line contact structure SC3, and the fourth word line contact structure SC4 correspond to the same memory array, the third word line contact structure SC3 is configured to be connected to a third word line driver SWD3, the fourth word line contact structure SC4 is configured to be connected to a fourth word line driver SWD4, the first word line contact structure SC1 and the third word line contact structure SC3 are located on the same side of the corresponding memory array, the second word line contact structure SC2 and the fourth word line contact structure SC4 are located on the same side of the corresponding memory array, the third word line contact structure SC3 and the fourth word line contact structure SC4 are oppositely disposed, and adjacent word lines corresponding to the same local bit line are connected to different word line contact structures on the same side.

[0048] The first word line contact structure SC1 and the third word line contact structure SC3 both extend in the second horizontal direction Y, and the first word line contact structure SC1 and the third word line contact structure SC3 are arranged in the second horizontal direction Y; every two memory cells arranged in the second horizontal direction Y refer to every two non-repeating memory cells. In addition, the memory rows on the opposite sides of the memory array in the second horizontal direction Y may be defined as edge memory rows. The edge memory rows are memory rows that operate normally, but the memory cells in the edge memory rows do not share the local bit line LBL with any normally operating memory cell.

[0049] In some embodiments, the first word line contact structure SC1 and the second word line contact structure SC2 are directly opposite to each other, and the third word line contact structure SC3 and the fourth word line contact structure SC4 are directly opposite to each other. Being directly opposite means that the two are aligned in the second horizontal direction without misalignment. In other embodiments, the first word line contact structure SC1 and the second word line contact structure SC2 are misaligned in the second horizontal direction Y, and the third word line contact structure SC3 and the fourth word line contact structure SC4 are misaligned in the second horizontal direction Y.

[0050] In the embodiments shown in FIGS. 3 and 4, every two memory cells arranged in the second horizontal direction Y share one local bit line, and two memory rows arranged in the

second horizontal direction Y share the same set of local bit lines. Therefore, two adjacent word lines corresponding to the same set of local bit lines cannot be connected to the same word line contact structure, but can only be connected to different word line contact structures on the same side. Otherwise, the two memory cells sharing the local bit line will read data simultaneously, thereby leading to data errors. The case where two adjacent word lines can only be connected to different word line contact structures on the same side does not mean that each word line can only be connected to one word line contact structure, as long as the word line contact structures connected by the two adjacent word lines are different.

[0051] In some embodiments, in adjacent word lines WL corresponding to the same set of local bit lines LBL, one of the adjacent word lines is connected to the word line contact structure only at one end, or one is connected to only one word line contact structure, and the other is connected to two opposite word line contact structures at two ends, respectively. Illustratively, referring to FIG. 3, the memory array includes a third word line WL3 and a fourth word line WL4. The third word line WL3 and the fourth word line WL4 correspond to the same set of local bit lines LBL. The first end T1 of the third word line WL3 is connected to the third word line contact structure SC3, and the second end T2 is connected to the fourth word line contact structure SC4. Only the second end of the fourth word line WL4 is connected to the second word line contact structure SC2, with the first end being idle.

[0052] It should be noted that, as can be seen from the plan view shown in FIG. 3, the reason why the first end of the fourth word line WL4 is idle is that the first end is surrounded by the word line connected to the third word line contact structure, such that the first end of the fourth word line WL4 cannot be connected to the first end of the second word line WL2 in the plane. Then, in other embodiments, the first end of the fourth word line WL4 may be connected to the first end of the second word line WL2 via wiring in another plane. Similarly, the second end of the fifth word line WL5 may be connected to the second end of the third word line WL3 via wiring in another plane, i.e., in a jumper manner.

[0053] It can be understood that FIGS. 2, 3, and 4 are schematic plane layout diagrams. The storage structure in the memory for storing data may be only a single-layer structure, or may be a multi-layer structure stacked in the vertical direction, and each layer of the structure may have the characteristics shown in FIGS. 2, 3, and 4. In some embodiments, the memory includes a plurality of layers of memory arrays vertically stacked, and different memory cells vertically stacked share the local bit line LBL extending in a vertical direction Z, the vertical direction Z being perpendicular to a first horizontal direction X (i.e., the extension direction of the word line) and a second horizontal direction Y.

[0054] It should be noted that the projections of the word line contact structures in the vertical direction Z corresponding to different layers of memory arrays subMat stacked in the vertical direction Z need to be at least partially misaligned, such that the word line contact structures of different layers can be externally connected through different contact holes extending in the vertical direction Z, thereby connecting to different word line drivers.

[0055] In some embodiments, the memory array is provided with an edge word line, or in other words, the word line located at the outermost edge of the same memory array is defined as an edge word line. Each memory array is provided with two opposite edge word lines. The edge word line and an adjacent word line correspond to different local bit lines, and the edge word line and the adjacent word line are at least connected to the same word line contact structure. Taking FIG. 3 as an example, the first word line WL1 is an edge word line, and the word line adjacent to the first word line WL1 is the second word line WL2. Since the second word line WL2 is connected to both the first word line contact structure SC1 and the second word line contact structure SC2 and blocks the path for the first word line WL1 to be connected to other word lines in the plane, in the case that the first word line WL1 and the second word line WL2 are not connected to at least the same word line contact structure, i.e., are not activated or turned off simultaneously, the first word line WL1 needs to be connected to other word lines or other word line contact structures in a jumper manner, which will greatly increase the complexity of the connecting lines. Meanwhile, in the case that the storage structure is a multi-layer structure, the difficulty of routing jumpers for memory arrays located in non-edge layers becomes extremely high. Therefore, allowing the edge word line and the adjacent word line to be connected to at least the same word line contact structure helps reduce the complexity of the connecting lines.

[0056] In some embodiments, for example, in the embodiment shown in FIG. 3, the edge word line is connected to only one word line contact structure. Specifically, the second word line WL2 is connected to both the first word line contact structure SC1 and the second word line contact structure, and the first word line WL1 is connected to only the first word line contact structure SC1. In the embodiment shown in FIG. 4, the edge word line and an adjacent word line are simultaneously connected to two opposite word line contact structures. Specifically, the first word line WL1 and the second word line WL2 are connected to both the first word line contact structure SC1 and the second word line contact structure SC2.

[0057] In some embodiments, for example, in the embodiments shown in FIGS. 3 and 4, since every two memory rows share the same set of local bit lines LBL, it is inevitable that three word lines continuously arranged cannot be connected to the same word line contact

structure. In other words, among a plurality of word lines connected to the same word line contact structure, at least one word line is not adjacent to other word lines in the second horizontal direction.

[0058] Taking FIGS. 2, 3, and 4 as examples, the improvement of the embodiments of the present disclosure over the embodiment shown in FIG. 1 is analyzed. In the embodiments of the present disclosure, since each word line is driven by two word line drivers, the degree to which the word line is driven is higher, such that the length of each word line can be longer, and the number of memory cells corresponding to each word line can be greater. According to experimental measurements, the number of memory cells in a memory row can be increased from the original N to 1.6N. Since the number of memory rows in the memory array becomes 6, and the number of word line drivers that can be fully utilized in each memory array is 2, the ratio of the number of memory cells in the memory array to the number of corresponding fully utilized word line drivers/the number of word line contact structures is $6 \times 1.6N/2 = 4.8N$. Compared to the original ratio of 4N, it can be seen that the ratio is increased by a factor of 1.2.

[0059] The area of the word line contact structure corresponding to the memory array is only related to the number of layers in which the memory array is located. In the case that the number of layers of the memory array in the embodiments shown in FIGS. 2, 3, and 4 does not change compared to FIG. 1, the area of the word line contact structure corresponding to each layer of the memory array also does not change. Assuming that the area of each word line contact structure is 1, the ratio of the number of memory cells in the memory array to the area of the corresponding word line contact structure is 4.8N. In this way, it is equivalent to reducing the area proportion of the word line contact structure within the entire memory, thereby improving the storage efficiency. Meanwhile, since the projected area of the memory array with the same capacity in the vertical direction Z is a fixed value, the area proportion of the word line contact structures is reduced, which is equivalent to reducing the sum of the area of the improved memory array per unit capacity and the area of the corresponding word line contact structure, thus facilitating the increase in the number of dies that can be cut from each wafer.

[0060] In addition, the time required to activate the word line is long. After measurement, compared to the embodiment shown in FIG. 1, the time required to pull up the voltage of the word line to 90% of the target voltage is reduced by 1.98 ns in the improved memory. In fact, in the embodiments shown in FIGS. 2 to 4, each word line in the memory array is driven not only by the word line driver connected to the adjacent word line contact structure but also by

the word line driver connected to a farther word line contact structure, such that the word lines of different memory arrays in the first horizontal direction X are driven to a more uniform and consistent degree.

[0061] Those of ordinary skill in the art can understand that the above implementations are specific embodiments of practicing the present disclosure, while in practical applications, various changes can be made to the implementations in form and detail without departing from the spirit and scope of the present disclosure. Any person skilled in the art can make respective changes and modifications without departing from the spirit and scope of the present disclosure, and the protection scope of the present disclosure is defined by the appended claims.

CLAIMS

What is claimed is:

1. A memory, comprising:

a memory array, wherein the memory array comprises a plurality of word lines; and

a word line contact structure, comprising a first word line contact structure and a second word line contact structure located on opposite sides of the memory array, wherein the first word line contact structure is configured to be connected to a first word line driver, the second word line contact structure is configured to be connected to a second word line driver, and each of the plurality of word lines in the memory array is driven by both the first word line driver and the second word line driver.

2. The memory according to claim 1, wherein each of the plurality of word lines is provided with a first end and a second end opposite to each other, the first end of at least one of the plurality of word lines is directly connected to the first word line contact structure, and the second end is directly connected to the second word line contact structure.

3. The memory according to claim 2, wherein the at least one word line comprises two word lines connected end to end, and the two word lines connected end to end form a closed ring surrounding a memory cell.

4. The memory according to claim 1, wherein each memory array comprises a plurality of memory rows, all memory cells in a same memory row share a same word line, adjacent memory rows in a same memory array are connected to different local bit lines, and at least two adjacent word lines are simultaneously connected to the first word line contact structure and the second word line contact structure.

5. The memory according to claim 4, wherein the plurality of word lines extend in a first horizontal direction, and all word lines simultaneously connected to the first word line contact structure and the second word line contact structure are continuously arranged in a second horizontal direction, the second horizontal direction being perpendicular to the first horizontal direction and a vertical direction.

6. The memory according to claim 1, wherein each memory array comprises a plurality of memory rows, all memory cells in a same memory row share a same word line, and every two memory cells arranged in a second horizontal direction share one local bit line, the second horizontal direction being perpendicular to an extension direction of the word line; the word line contact structure further comprises: a third word line contact structure and a fourth word line contact structure, wherein the first word line contact structure, the second word line

contact structure, the third word line contact structure, and the fourth word line contact structure correspond to a same memory array, the third word line contact structure is configured to be connected to a third word line driver, the fourth word line contact structure is configured to be connected to a fourth word line driver, the first word line contact structure and the third word line contact structure are located on a same side of the corresponding memory array, the second word line contact structure and the fourth word line contact structure are located on a same side of the corresponding memory array, the third word line contact structure and the fourth word line contact structure are oppositely arranged, and adjacent word lines corresponding to a same local bit line are connected to different word line contact structures on the same side.

7. The memory according to claim 4 or 6, wherein the memory comprises a plurality of layers of memory arrays vertically stacked, and different memory cells vertically stacked share the local bit line extending in a vertical direction, the vertical direction being perpendicular to the extension direction of the word line.

8. The memory according to claim 6, wherein in adjacent word lines corresponding to a same set of local bit lines, one of the adjacent word lines is connected to the word line contact structure only at one end, and the other is connected to two opposite word line contact structures at two ends, respectively.

9. The memory according to claim 6, wherein the memory array is provided with an edge word line, the edge word line and an adjacent word line correspond to different local bit lines, and the edge word line and the adjacent word line are at least connected to a same word line contact structure.

10. The memory according to claim 9, wherein the edge word line and the adjacent word line are simultaneously connected to two opposite word line contact structures.