

SYSTEM AND METHOD FOR EXECUTING A PLURALITY OF
INSTRUCTIONS IN A PROCESSOR HAVING A PIPELINE

ABSTRACT OF THE DISCLOSURE

A method processing a plurality of instructions in a processor having a pipeline is provided. Pipeline includes a first number of stages between a fetch stage and an execute stage. The method includes determining if a condition is met for a conditional call instruction. If the condition is met, the count of a counter is combined with a number associated with the first number of stages to produce an adjusted return address. The method also includes fetching the next instruction having an address designated by the adjusted return address after fetching and executing any instruction associated with the conditional call instruction.

Figure 1(a)