

SEMICONDUCTOR MEMORY DEVICES

ABSTRACT OF THE DISCLOSURE

By setting full group reversal control gates (RVG00), (RVG01) to a logical voltage "H", memory cells on all bit lines of a memory cell array block (BLKn) are connected to a reversal voltage supply circuit (DVS00) so that a group reversal operation is performed. When one of the group reversal control gates (RVG00), (RVG01) is set to the logical voltage "H", the memory cells on the bit lines having either even or odd numbers of the memory cell array block (BLKn) are connected to the reversal voltage supply circuit (DVS00) so that a partial group reversal operation is performed. When one of column selection gates (CG0) to (CG63) is set to the logical voltage "H", the selected bit line is connected to the reversal voltage supply circuit (DVS01). Consequently, a line reversal operation for the memory cell connected to the selected bit line is performed. Thus, the high-speed reversal operation which fully controls the offleak current of the memory cell can be implemented and the low-voltage operation can be realized by changing the operation unit for performing the reversal operation.

FIGURE 1