

SEMICONDUCTOR ENCAPSULATION METHOD AND SEMICONDUCTOR ENCAPSULATION STRUCTURE

TECHNICAL FIELD

Embodiments of this disclosure are directed to a semiconductor packaging method and a semiconductor package structure.

BACKGROUND

In the related art, a packaging process may involve placing, among other components to be packaged, an inductor and a die side by side on a carrier board. Such a parallel package resulting from the process is bulky in size and lacks structural compactness.

In view of the demand for increasingly miniaturized electronics with lighter weights, structurally compact small-size chip packages would become more and more popular in the marketplace.

SUMMARY

At least one embodiment of the present disclosure provides a semiconductor packaging method, including:

fixing a first die, a second die and a conductive post to a carrier board, the first and second dies oriented with their front sides facing the carrier board, the first die provided on its front side with a first bond pad, the second die provided on its front side with a second bond pad, the first die provided on a back side thereof with an inductance element, the inductance element having a first electrical connection point, the first electrical connection point located on the side of the inductance element away from the first die, the conductive post disposed between the first and second dies and extending perpendicular to the first die;

forming a plastic encapsulation layer on the carrier board, the plastic encapsulation layer encapsulating the first die, the second die, the inductance element and the conductive post, with the first electrical connection point of the inductance

element and a first end of the conductive post being both exposed from a first surface of the plastic encapsulation layer, the first surface of the plastic encapsulation layer representing its surface that is disposed closer to the back side of the first die than to the front side of the first die;

forming a first conductive trace on the first surface of the plastic encapsulation layer, the first conductive trace connecting the first electrical connection point of the inductance element to the first end of the conductive post that is exposed from the first surface of the plastic encapsulation layer;

removing the carrier board; and

forming a second conductive trace on a second surface of the plastic encapsulation layer, the second conductive trace connecting the second bond pad on the second die to a second end of the conductive post that is exposed from the second surface of the plastic encapsulation layer, the second surface of the plastic encapsulation layer opposing the first surface thereof.

At least some embodiments of the present disclosure provide a semiconductor package structure, including:

a plastic encapsulation layer;

a first die provided on a front side thereof with a first bond pad, the first die disposed within the plastic encapsulation layer;

a second die provided on a front side thereof with a second bond pad, the second die disposed within the plastic encapsulation layer side by side with the first die, wherein the front side of the first bond pad is oriented in the same direction as the front side of the second bond pad;

an inductance element disposed on the back side of the first die so as to be located between the first die and the plastic encapsulation layer, the inductance element having a first electrical connection point, the first electrical connection point located on the side of the inductance element away from the first die;

a conductive post disposed between the first die and the second die, the conductive post extending through the plastic encapsulation layer;

a first conductive trace disposed on a first surface of the plastic encapsulation

layer and connecting the first electrical connection point of the inductance element to a first end of the conductive post that is exposed from the first surface of the plastic encapsulation layer, the first surface of the plastic encapsulation layer representing its surface that is disposed closer to the back side of the first die than to the front side of the first die; and

a second conductive trace disposed on a second surface of the plastic encapsulation layer and connecting the second bond pad on the second die to a second end of the conductive post that is exposed from the second surface of the plastic encapsulation layer, the second surface of the plastic encapsulation layer opposing the first surface thereof.

According to the embodiments of this disclosure, through disposing the inductance element on the back side of the first die, the first die and the inductance element are stacked together along the thickness direction of the first die. This sensible spatial utilization in the thickness direction of the first die enables the semiconductor package structure to have a compact structure and a reduced size. Therefore, the semiconductor package structure according to the embodiments of the disclosure is small in size, compact in structure and suitable for use in a small-size, lightweight electronic device.

The details of one or more embodiments of this disclosure are set forth in the accompanying drawings and the description below. Other features, objects, and advantages of the disclosure will be apparent from the description and drawings, and from the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

In order to more clearly explain the subject matter of embodiments of the present disclosure, the accompanying drawings, to which reference is to be made in connection with the following description of the embodiments, will be briefed below. Apparently, these drawings show only some embodiments of, but do not imply any limitation on, the disclosure.

Fig. 1 is a schematic diagram showing the structure of a semiconductor package

structure according to an embodiment of the present disclosure.

Fig. 2 is a flowchart of a semiconductor packaging method according to an embodiment of the present disclosure.

Fig. 3 shows a structural schematic of an intermediate structure formed during a process for making a semiconductor package structure according to an embodiment of the present disclosure.

Fig. 4 shows a structural schematic of another intermediate structure formed during a process for making a semiconductor package structure according to an embodiment of the present disclosure.

Fig. 5 shows a structural schematic of a further intermediate structure formed during a process for making a semiconductor package structure according to an embodiment of the present disclosure.

Fig. 6 shows a structural schematic of a further intermediate structure formed during a process for making a semiconductor package structure according to an embodiment of the present disclosure.

Fig. 7 shows a structural schematic of a further intermediate structure formed during a process for making a semiconductor package structure according to an embodiment of the present disclosure.

Fig. 8 shows a structural schematic of a further intermediate structure formed during a process for making a semiconductor package structure according to an embodiment of the present disclosure.

Fig. 9 shows a structural schematic of a further intermediate structure formed during a process for making a semiconductor package structure according to an embodiment of the present disclosure.

Fig. 10 shows a structural schematic of a further intermediate structure formed during a process for making a semiconductor package structure according to an embodiment of the present disclosure.

Fig. 11 shows a structural schematic of a further intermediate structure formed during a process for making a semiconductor package structure according to an embodiment of the present disclosure.

Fig. 12A shows a structural schematic of a further intermediate structure formed during a process for making a semiconductor package structure according to an embodiment of the present disclosure.

Fig. 12B shows a structural schematic of a further intermediate structure formed during a process for making a semiconductor package structure according to an embodiment of the present disclosure.

Fig. 13 shows a structural schematic of a further intermediate structure formed during a process for making a semiconductor package structure according to an embodiment of the present disclosure.

Fig. 14 shows a structural schematic of a further intermediate structure formed during a process for making a semiconductor package structure according to an embodiment of the present disclosure.

Fig. 15 shows a structural schematic of a further intermediate structure formed during a process for making a semiconductor package structure according to an embodiment of the present disclosure.

Fig. 16 shows a structural schematic of a further intermediate structure formed during a process for making a semiconductor package structure according to an embodiment of the present disclosure.

Fig. 17 shows a structural schematic of a further intermediate structure formed during a process for making a semiconductor package structure according to an embodiment of the present disclosure.

Fig. 18 shows a structural schematic of a further intermediate structure formed during a process for making a semiconductor package structure according to an embodiment of the present disclosure.

Fig. 19 shows a structural schematic of a further intermediate structure formed during a process for making a semiconductor package structure according to an embodiment of the present disclosure.

Fig. 20 is a schematic diagram showing dicing of a plastic encapsulation body according to an embodiment of the present disclosure.

DETAILED DESCRIPTION

Here, exemplary embodiments will be described in detail, examples of which are illustrated in the accompanying drawings. When referring to the drawings below, unless otherwise indicated, like numerals throughout different ones of them represent the same or similar elements. The exemplary embodiments described hereunder do not represent all possible embodiments consistent with the present application. Rather, they are merely examples of devices and methods consistent with some aspects of this disclosure as detailed in the appended claims.

The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of this disclosure. As used herein and in the appended claims, the singular forms “a”, “an”, and “the” are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be also understood that, as used herein, the term “and/or” includes any and all combinations of one or more of the associated listed items.

It should be understood that although the terms such as “first”, “second”, “third” and the like may be used herein to describe various types of information, such information is not limited to these terms. These terms serve only to distinguish between information of the same type. For example, without departing from the scope of the present application, “first information” may be alternatively referred to as “second information”. Similarly, “second information” may be alternatively referred to as “first information”. Depending on the context, the term “if” as used herein may be interpreted as “when”, “upon” or “in response to a determination that”.

Several embodiments of the present disclosure will be described in detail below with reference to the accompanying drawings. Whenever there is no conflict, the following embodiments and features thereof can be combined with one another.

At least one embodiment of this disclosure provides a semiconductor package structure including: a plastic encapsulation layer; a first die provided on a front side thereof with a first bond pad and disposed within the plastic encapsulation layer; a second die provided on a front side thereof with a second bond pad and disposed within the plastic encapsulation layer side by side with the first die in such a manner

that the front side of the first bond pad is oriented in the same direction as the front side of the second bond pad; an inductance element provided on a back side of the first die so as to be situated between the first die and the plastic encapsulation layer, the inductance element including a first electrical connection point located on the side of the inductance element away from the first die; a conductive post disposed between the first die and the second die, the conductive post extending through the plastic encapsulation layer in a direction perpendicular to the front side of the first die; a first conductive trace disposed on a first surface of the plastic encapsulation layer and connecting the first electrical connection point of the inductance element to a first end of the conductive post that is exposed from the first surface of the plastic encapsulation layer, wherein the first surface of the plastic encapsulation layer represents its surface that is disposed closer to the back side of the first die than to the front side of the first die; and a second conductive trace disposed on a second surface of the plastic encapsulation layer and connecting the second bond pad on the second die to a second end of the conductive post that is exposed from the second surface of the plastic encapsulation layer, wherein the second surface of the plastic encapsulation layer is opposite to the first surface thereof.

The semiconductor package structure is a chip package and is suitable for use in the packaging of an antenna chip. The semiconductor package structure can be used in an electronic device such as a mobile phone, a computer or the like.

As shown in Fig. 1, the semiconductor package structure 1 according to the at least one embodiment of the present disclosure may include the first die 10, the second die 11, the inductance element 12, the conductive post 13, the plastic encapsulation layer 14, the first conductive trace 15, the second conductive trace 16, a first protective layer 17, a second protective layer 18, a first conductive filled interconnect 19, a second conductive filled interconnect 110, a first dielectric layer 111, a conductive bump 112, a second dielectric layer 113 and a surface finish layer 1121.

In one embodiment of the present disclosure, the first die 10 has the front side and the back side, the front side and the back side are arranged opposite each other. The first bond pad 1001 is provided on the front side of the first die 10. The first bond pad

1001 is configured for external electrical connection.

In one embodiment of the present disclosure, as shown in Fig. 1, the inductance element 12 is provided on the back side of the first die 10. The inductance element 12 is an electromagnetic conversion component. In one embodiment of the present disclosure, the inductance element 12 may be a coil. In one embodiment of the present disclosure, without wishing to be limiting, the inductance element 12 may be made of copper.

In one embodiment of the present disclosure, the second die 11 has the front side and a back side opposing the front side. The second bond pad 1101 is provided on the front side of the second die 11. The second bond pad 1101 is configured for external electrical connection.

In one embodiment of the present disclosure, without wishing to be limiting, two of the second dies 11 may be included, as shown in Fig. 1. The two second dies 11 may function in the same way or not.

In one embodiment of the present disclosure, without wishing to be limiting, the first die 10 may be disposed between the two second dies 11, as shown in Fig. 1.

In one embodiment of the present disclosure, the first connection point 121 of the inductance element 12 is exposed from the first surface of the plastic encapsulation layer 14, the first connection point 121 is configured for external electrical connection. The first surface of the plastic encapsulation layer 14 refers to its surface that is disposed closer to the back side of the first die than to the front side of the first die.

In one embodiment of the present disclosure, as shown in Fig. 1, the conductive post 13 is arranged between the first die 10 and the second die 11. The conductive post 13 extends through the plastic encapsulation layer 14 in the direction perpendicular to the front side of the first die 10. The first end 1301 of the conductive post 13 is exposed from the first surface of the plastic encapsulation layer 14, and the second end 1302 of the conductive post 13 is exposed from the second surface of the plastic encapsulation layer 14. Without wishing to be limiting, the conductive post 13 may be made of copper. Surfaces of the conductive post 13 at the first 1301 and second 1302 ends are exposed from the first and second surfaces of the plastic encapsulation layer

14. As noted above, the first surface of the plastic encapsulation layer 14 refers to its surface that is disposed closer to the back side of the first die than to the front side of the first die. The second surface of the plastic encapsulation layer 14 refers to its surface opposing the first surface.

In one embodiment of the present disclosure, as shown in Fig. 1, the plastic encapsulation layer 14 encapsulates the first die 10, the second die 11, the inductance element 12 and the conductive post 13. The plastic encapsulation layer 14 may be a polymer, a resin, a composite resin material or a composite polymer material. The composite resin material may be a resin embedded with a filler. The filler may be inorganic particles.

In one embodiment of the present disclosure, as shown in Fig. 1, the plastic encapsulation layer 14 has a first opening 131 in which the first electrical connection point 121 of the inductance element 12 is exposed. For example, the first opening 131 is provided in the first surface of the plastic encapsulation layer 14. An orthogonal projection of the first opening 131 on the first die 10 at least partially overlaps with an orthogonal projection of the first electrical connection point 121 of the inductance element 12 on the first die 10, resulting in exposure of the first electrical connection point 121 from the first surface of the plastic encapsulation layer 14. For example, the projection of the first opening 131 on the first die 10 may completely overlap with the projection of the first electrical connection point 121 on the first die 10, resulting in complete exposure of the first electrical connection point 121 from the first surface of the plastic encapsulation layer 14. As another example, the orthogonal projection of the first opening 131 on the first die may partially overlap with the orthogonal projection of the first electrical connection point 121 on the first die, resulting in exposure of part of the first electrical connection point 121 from the first surface of the plastic encapsulation layer 14. The first surface of the plastic encapsulation layer 14 refers to the surface of the plastic encapsulation layer 14 that is disposed closer to the back side of the first die than to the front side of the first die.

In one embodiment of the present disclosure, as shown in Fig. 1, the first conductive filled interconnect 19 is located within the first opening 131. The first

conductive filled interconnect 19 is electrically connected to the first electrical connection point 121 of the inductance element 12, and the first conductive trace 15 is electrically connected to the first conductive filled interconnect 19. Without wishing to be limiting, the first conductive filled interconnect 19 may be formed of copper.

In one embodiment of the present disclosure, as shown in Fig. 1, the first conductive trace 15 is disposed on the first surface of the plastic encapsulation layer 14 and connects the first electrical connection point 121 to the first end 1301 of the conductive post 13 that is exposed from the first surface of the plastic encapsulation layer 14. Without wishing to be limiting, the first conductive trace 15 may be made of copper.

In one embodiment of the present disclosure, as shown in Fig. 1, the first dielectric layer 111 is disposed on the first surface of the plastic encapsulation layer 14 and encapsulates at least the first conductive trace 15. The first dielectric layer 111 may be composed of one or more layers of insulating materials, each of which may be polyimide (PI), polybenzoxazole (PBO), an organic polymer, an organic composite polymer material or another material with similar properties.

In one embodiment of the present disclosure, as shown in Fig. 1, the first protective layer 17 covers the front side of the first die 10, and the second protective layer 18 covers the front side of the second die 11. The first die 10 and the second die 11 may have an equal thickness, and the first protective layer 17 and the second protective layer 18 may have an equal thickness. Alternatively, the first die 10 and the second die 11 may have different thicknesses, and the first protective layer 17 and the second protective layer 18 may have different thicknesses. However, the present disclosure is not so limited. A distance from a surface of the first protective layer 17 away from the inductance element 12 to a surface of the inductance element 12 away from the first protective layer 17 is smaller than a height of the conductive post 13. A distance from a surface of the second protective layer 18 away from the back side of the second die 11 to the back side of the second die 11 is smaller than the height of the conductive post 13.

In one embodiment of the present disclosure, as shown in Fig. 1, the first

protective layer 17 has a second opening 171 in which the first bond pad 1001 on the first die 10 is exposed. An orthogonal projection of the second opening 171 on the first die 10 at least partially overlaps with an orthogonal projection of the first bond pad on the first die 10, resulting in exposure of at least part of the first bond pad from the first protective layer 17. For example, the orthogonal projection of the second opening 171 on the first die 10 may completely overlap with the orthogonal projection of the first bond pad 1001 on the first die 10, resulting in complete exposure of the first bond pad 1001 from the first protective layer 17. As another example, the orthogonal projection of the second opening 171 on the first die 10 may partially overlap with the orthogonal projection of the first bond pad 1001 on the first die 10, resulting in exposure of at least part of the first bond pad 1001 from the first protective layer 17.

In one embodiment of the present disclosure, as shown in Fig. 1, the second protective layer 18 has a third opening 181 in which the second bond pad 1101 on the second die 11 is exposed. An orthogonal projection of the third opening 181 on the second die 11 at least partially overlaps with an orthogonal projection of the second bond pad 1101 on the second die 11, resulting in exposure of at least part of the second bond pad 1101 from the second protective layer 18. For example, the orthogonal projection of the third opening 181 on the second die 11 may completely overlap with the orthogonal projection of the second bond pad 1101 on the second die 11, resulting in exposure of the second bond pad 1101 from the second protective layer 18. As another example, the orthogonal projection of the third opening 181 on the second die 11 may partially overlap with the orthogonal projection of the second bond pad 1101 on the second die 11, resulting in exposure of at least part of the second bond pad 1101 from the second protective layer 18.

In one embodiment of the present disclosure, as shown in Fig. 1, the second conductive filled interconnect 110 is located within the second opening 171, and a third conductive filled interconnect 120 within the third opening 181. The second conductive filled interconnect 110 is electrically connected to the first bond pad 1001 on the first die 10, the third conductive filled interconnect 120 is electrically connected to the second bond pad 1101 on the second die 11. The second conductive trace 16 is

electrically connected to both the second conductive filled interconnect 110 and the third conductive filled interconnect 120. Without wishing to be limiting, the second conductive filled interconnect 110, the third conductive filled interconnect 120 and the second conductive trace 16 may be made of copper.

In one embodiment of the present disclosure, as shown in Fig. 1, the second conductive trace 16 is disposed on the second surface of the plastic encapsulation layer 14 and connects the second bond pad 1101 on the second die 11 to the second end of the conductive post 13 that is exposed from the second surface. The second surface of the plastic encapsulation layer 14 opposes the first surface thereof. The second conductive trace 16 is also electrically connected to the first bond pad on the first die 10.

In one embodiment of the present disclosure, as shown in Fig. 1, the conductive bump 112 is brought into contact with the second conductive trace 16 and located at the second electrical connection point 161. Without wishing to be limiting, the conductive bump 112 may be made of copper.

In one embodiment of the present disclosure, as shown in Fig. 1, the second dielectric layer 113 is disposed on the second surface of the plastic encapsulation layer 14, the second dielectric layer 113 covers at least the second conductive trace 16 and encapsulates the conductive bump 112. A surface of the conductive bump 112 away from the first die 10 is exposed from the second dielectric layer 113. The second dielectric layer 113 may be composed of one or more layers of insulating materials, each of which may be PI, PBO, an organic polymer, an organic composite polymer material or another material with similar properties.

In one embodiment of the present disclosure, the surface finish layer 1121 is disposed on the surface of the conductive bump 112, and the surface finish layer 1121 is configured to slow down oxidation of the conductive bump 112. The surface finish layer may be formed of matte tin or an electroplated composite layer. For example, the electroplated composite layer may include a stack of two metal layers on the surface of the conductive bump 112, which are a nickel (Ni) proximate the surface of the conductive bump 112 and a gold (Au) layer away from the surface of the conductive

bump 112. As another example, the electroplated composite layer may include a stack of three metal layers, which are a nickel (Ni) proximate the surface of the conductive bump 112, an outermost gold (Au) layer and a palladium (Pd) layer sandwiched between the two.

In one embodiment of the present disclosure, as shown in Fig. 1, the inductance element 12 on the back side of the first die 10 is electrically connected to the second die 11 through the first conductive filled interconnect 19, the first conductive trace 15, the conductive post 13, the second conductive trace 16 and the third conductive filled interconnect 120.

According to the embodiments of this disclosure, through disposing the inductance element on the back side of the first die, the first die and the inductance element are stacked together along the thickness direction of the first die. This sensible spatial utilization in the thickness direction of the first die enables the semiconductor package structure to have a compact structure and a reduced size. Therefore, the semiconductor package structure according to the embodiments of the disclosure is small in size, compact in structure and suitable for use in a small-size, lightweight electronic device.

At least one embodiment of the present disclosure also provides a semiconductor packaging method. As shown in Fig. 2, the semiconductor packaging method includes steps S201 to S211 below.

In step S201, a first die, a second die and a conductive post are fixed to a carrier board. The first die 10 and the second die 11 are both oriented with their front sides facing the carrier board 31. A first bond pad 1001 is provided on the front side of the first die 10, and a second bond pad 1101 is provided on the front side of the second die 11. An inductance element 12 is provided on a back side of the first die 10. The inductance element 12 has a first electrical connection point 121 disposed on the side of the inductance element 12 away from the first die 10. The conductive post 13 is arranged between the first die 10 and the second die 11. The conductive post 13 has a first end 1301 and a second end 1302. The first end 1301 is located proximate one end of the inductance element 12, and the second end 1302 is located away from the end of

the inductance element 12.

In one embodiment of the present disclosure, as a result of fixing the first die 10, the second die 11 and the conductive post 13 to the carrier board 31, an intermediate structure as shown in Fig. 3 is obtained. Although Fig. 3 shows only one packaging unit, i.e., a unit that forms one semiconductor (chip) package at the end of the packaging process, in practice, there may be either one or more packaging units on the carrier board 31, and the present disclosure is not limited to any particular number of such packaging units.

In one embodiment of the present disclosure, the carrier board 31 is provided thereon with an adhesive layer configured to fix the first die 10, the second die 11 and the conductive post 13 to the carrier board 31. In one embodiment of the present disclosure, the adhesive layer is a thermally removable layer.

In one embodiment of the present disclosure, step S201 may include: at first, as shown in Fig. 4, forming a second metal layer 41 on the carrier board 31; then, as shown in Fig. 5, etching the second metal layer 41 to form the conductive post 13; and subsequently, bonding the first die 10 and the second die 11 onto the carrier board 31.

In an alternative embodiment of this disclosure, the conductive post may be pre-formed. In this case, step S201 may include: at first, providing the first die 10, the second die 11 and the pre-formed conductive post 13; and then, bonding the first die 10, the second die 11 and the conductive post 13 onto the carrier board 31.

In some embodiments of the present disclosure, prior to step S201, the following steps are included.

At first, a seed layer 60 is formed over a back side of a silicon wafer 62 by a sputtering process. In one embodiment of the present disclosure, the seed layer 60 includes a first seed layer 601 that is a copper layer. In this case, the first seed layer 601 (i.e., the seed layer 60) may be formed on the back side of the silicon wafer 62 by sputtering copper. In one embodiment of the present disclosure, the seed layer 60 further includes a second seed layer 602. In this case, the formation of the seed layer 60 may include: first sputtering titanium over the back side of the silicon wafer 62 to form the second seed layer 602; and then forming the first seed layer 601 on the

second seed layer 602 by sputtering copper. The titanium second seed layer enables increased interlayer adhesion, and the copper first seed layer provides good mechanical properties and electrical conductivity.

Subsequently, a first metal layer 61 is formed on the seed layer by an electroplating process. In one embodiment of the present disclosure, the first metal layer may be a copper layer. As a result of forming the first metal layer 61 on the seed layer, an intermediate structure as shown in Fig. 6 is obtained. The first metal layer 61 is spaced apart from the silicon wafer 62 by the seed layer 60.

It is to be noted that the seed layer between the first metal layer and the back side of the silicon wafer may be omitted. In the remaining drawings, the seed layer is not shown for the sake of simplicity.

Afterward, an etching process is performed on the first metal layer 61 and the seed layer, resulting in the formation of the inductance element 12. In one embodiment of the present disclosure, as shown in Fig. 7, the inductance element 12 is formed by etching the first metal layer 61. For example, the formation of the inductance element (inductor/coil) on the back side of the silicon wafer may involve spin coating of photoresist, exposure, development, stripping of the photoresist and etching. In one embodiment of the present disclosure, the inductance element may be a coil.

After that, the first protective layer 17 is formed on a front side of the silicon wafer. In one embodiment of the present disclosure, as shown in Fig. 8, the first protective layer 17 is formed on the front side of the silicon wafer 62. The first protective layer 17 may be formed by lamination, spin coating, printing, molding or another suitable method. The first protective layer 17 may be formed of a laser-reactive material or a photosensitive material.

The first die 10 is then obtained by dicing the silicon wafer 62. In one embodiment of the present disclosure, as shown in Fig. 9, the first die 10 is obtained by dicing the silicon wafer 62.

In one embodiment of the present disclosure, as shown in Fig. 10, a second protective layer 18 may be formed on the front side of the silicon wafer 11a, and then as shown in Fig. 11, the second die 11 may be obtained by dicing a silicon wafer 11a.

The second protective layer 18 may be formed of a laser-reactive material or a photosensitive material.

In step S202, a plastic encapsulation layer 14 is formed on the carrier board so as to encapsulate the first die 10, the second die 11, the inductance element 12 and the conductive post 13, with a first electrical connection point of the inductance element 12 and a first end face of the conductive post 13 being both exposed from a first surface of the plastic encapsulation layer 14. The first surface of the plastic encapsulation layer 14 refers to its surface that is disposed closer to the back side of the first die than to the front side of the first die.

In one embodiment of the present disclosure, as shown in Fig. 12A, the plastic encapsulation layer 14 encapsulates the first die 10, the second die 11, the inductance element 12 and the conductive post 13, with the first end face of the conductive post 13 be exposed from the first surface of the plastic encapsulation layer 14. A thickness of the plastic encapsulation layer 14 is equal to a height of the conductive post 13.

In one embodiment of the present disclosure, step S202 may include the steps of: at first, as shown in Fig. 12B, forming an encapsulation layer 141 on the carrier board 31, wherein the encapsulation layer 141 encapsulates the first die 10, the second die 11, the inductance element 12 and the conductive post 13, and the encapsulation layer 141 has a thickness greater than the height of the conductive post 13; and then thinning the encapsulation layer 141 into the plastic encapsulation layer 14, the first end of the conductive post 13 is exposed from the first surface of the plastic encapsulation layer 14. The thickness of the plastic encapsulation layer 14 is equal to the height of the conductive post 13. The thinning of the encapsulation layer 141 may be accomplished by mechanical polishing.

In step S203, a first conductive trace connecting the first electrical connection point of the inductance element to the first end of the conductive post is formed on the first surface of the plastic encapsulation layer.

In one embodiment of the present disclosure, prior to step S203, as shown in Fig. 13, a laser drilling process may be performed on the first surface of the plastic encapsulation layer 14 to form a first opening 131. For example, the first opening 131

may be performed in the plastic encapsulation layer 14 by laser irradiation, and the first electrical connection point 121 of the inductance element 12 may be exposed in the first opening 131.

In one embodiment of the present disclosure, as shown in Fig. 14, a first conductive filled interconnect 19 may be formed by filling a first conductive medium in the first opening 131, and a first conductive layer may be formed on the plastic encapsulation layer 14. The first conductive filled interconnect 19 is electrically connected to the first electrical connection point 121 of the inductance element 12, and the first conductive layer is electrically connected to the first conductive filled interconnect 19. The first conductive layer may be formed by metal sputtering, electrolytic plating, electroless plating or another technique. The first conductive filled interconnect 19 and the first conductive layer may be formed in the same process step. After that, the first conductive layer may be patterned to form the first conductive trace 15. In this way, the inductance element 12 is electrically connected to the conductive post 13 via the first conductive filled interconnect 19 and the first conductive trace 15.

In step S204, a first dielectric layer covering at least the first conductive trace is formed on the first surface of the plastic encapsulation layer.

In one embodiment of the present disclosure, as shown in Fig. 15, the first dielectric layer 111 covering at least the first conductive trace 15 is formed on the first surface of the plastic encapsulation layer. The first dielectric layer 111 may be formed by lamination, spin coating, printing, molding or another suitable method. The first dielectric layer 111 may be composed of one or more layers of insulating materials, each of which may be PI, PBO, an organic polymer, an organic composite polymer material or another material with similar properties.

In step S205, the carrier board is removed.

In step S206, a second opening in which the bond pad on the first die is exposed is formed in the first protective layer and a third opening in which the second bond pad on the second die is exposed is formed in the second protective layer. A projection of the second opening on the first die at least partially overlaps with a projection of the first bond pad on the first die, resulting in exposure of at least part of the first bond pad.

A projection of the third opening on the second die at least partially overlaps with a projection of the second bond pad on the second die, resulting in exposure of at least part of the second bond pad.

In one embodiment of the present disclosure, as shown in Fig. 16, at least part of the first bond pad 1001 is exposed in the second opening 171 formed in the first protective layer 17. In case of the first protective layer 17 being formed of a laser-reactive material, the second opening 171 may be formed by a laser drilling process. In case of the first protective layer 17 being formed of photosensitive material, the second opening 171 may be formed by a photolithography process.

It is to be noted that the step of forming the second opening 171 in the first protective layer 17 may be performed after step 205 or the step of forming the first protective layer 17 on the front side of the first die 10, and before the step of fixing the first die 10, the second die 11 and the conductive post 13 to the carrier board 31.

In one embodiment of the present disclosure, as shown in Fig. 16, at least part of the second bond pad 1101 is exposed in the third opening 181 formed in the second protective layer 18. In case of the second protective layer 18 being formed of a laser-reactive material, the third opening 181 may be formed by a laser drilling process. In case of the second protective layer 18 being formed of photosensitive material, the third opening 181 may be formed by a photolithography process.

It is to be noted that the step of forming the third opening 181 in the second protective layer 18 may be performed after step 205 or the step of forming the second protective layer 18 on the front side of the second die 11, and before the step of fixing the first die 10, the second die 11 and the conductive post to the carrier board.

In step S207, a second conductive trace connecting the second bond pad on the second die to the second end of the conductive post is formed on a second surface of the plastic encapsulation layer. The second surface of the plastic encapsulation layer opposes the first surface thereof.

In one embodiment of the present disclosure, as shown in Fig. 17, a second conductive filled interconnect 110 may be formed by filling a second conductive medium in the second opening 171, and a third conductive filled interconnect 120 may

be formed by filling a third conductive medium in the third opening 181. Moreover, a second conductive layer (not shown) may be formed over the second surface of the plastic encapsulation layer 14, the first protective layer 17 and the second protective layer 18. The second surface of the plastic encapsulation layer 14 opposes the first surface of the plastic encapsulation layer 14. The second conductive filled interconnect 110 is electrically connected to the first bond pad 1001 on the first die 10, the third conductive filled interconnect 120 is electrically connected to the second bond pad 1101 on the second die 11, and the second conductive layer is electrically connected to both second conductive filled interconnect 110 and the third conductive filled interconnect 120. The second conductive layer may be formed by metal sputtering, electrolytic plating, electroless plating or another technique. The second conductive filled interconnect 110 and the second conductive layer may be formed in the same process step. The second conductive layer may be then patterned to form the second conductive trace 16.

In step S208, a conductive bump is formed at a second electrical connection point of the second conductive trace.

In one embodiment of the present disclosure, as shown in Fig. 18, the conductive bump 112 is formed at the second electrical connection point 161 of the second conductive trace 16.

In step S209, a second dielectric layer is formed on the second surface of the plastic encapsulation layer 14, resulting in the formation of a plastic encapsulation body. The second dielectric layer encapsulates at least the second conductive trace and the conductive bump, with a surface of the conductive bump away from the first die being exposed from the second dielectric layer.

In one embodiment of the present disclosure, as shown in Fig. 19, the second dielectric layer 113 may be formed on the second surface of the plastic encapsulation layer 14, resulting in the formation of the plastic encapsulation body 20. The second dielectric layer 113 encapsulates at least the second conductive trace 16 and the conductive bump 112, with the surface of the conductive bump 112 away from the first die 10 being exposed from the second dielectric layer 113. A surface of the second

dielectric layer 113 away from the first die 10 is flush with the surface of the conductive bump 112 away from the first die 10.

In practical implementations, the second dielectric layer 113 may be so formed as to have a thickness along the direction perpendicular to the front side of the first die 10, which may be greater than a height of the conductive bump 112 along the direction perpendicular to the front side of the first die 10. The so-formed second dielectric layer 113 may be then thinned until its surface away from the first die 10 becomes flush with the surface of the conductive bump 112 away from the first die 10.

In step S210, a surface finish layer is formed on the exposed surface of the conductive bump.

In one embodiment of the present disclosure, as shown in Fig. 19, the surface finish layer 1121 may be formed on the exposed surface of the conductive bump 112. Of course, in an alternative embodiment, the surface finish layer may not be formed on the surface of the conductive bump 112.

In step S211, a semiconductor package structure is obtained by dicing the plastic encapsulation body.

In one embodiment of the present disclosure, as shown in Fig. 20, the semiconductor package structure as shown in Fig. 1 may be obtained by dicing the plastic encapsulation body 20 at a dicing location L. The semiconductor package structure includes the first die 10, the second die 11, the inductance element 12, the conductive post 13, the plastic encapsulation layer 14, the first conductive trace 15 and the second conductive trace 16.

According to the embodiments of this disclosure, through disposing the inductance element on the back side of the first die, the first die and the inductance element are stacked together along the thickness direction of the first die. This sensible spatial utilization in the thickness direction of the first die enables the semiconductor package structure to have a compact structure and a reduced size. Therefore, the semiconductor package structure according to the embodiments of the disclosure is small in size, compact in structure and suitable for use in a small-size, lightweight electronic device.

In this disclosure, the device embodiments and the method embodiments may supplement each other if there is no conflict therebetween. The foregoing device embodiments are only illustrative, and the modules thereof that have been described as separate components may be physically separated or not, and the components that have been shown as modules may be physical modules or not. They may be deployed in a single location or distributed across a plurality of network devices. As practically required, either all or some of such modules may be selected in accordance with embodiments disclosed herein. Those of ordinary skill in the art can understand and implement them without paying any creative effort.

Presented above are merely several exemplary embodiments of the present disclosure, and they are not intended to limit this disclosure in any way. Any and all alternations, equivalent substitutions, modification and so on made within the spirit and principles of the present disclosure are considered to fall within the scope of protection of this disclosure.

Claims

1. A semiconductor packaging method comprising:

fixing a first die, a second die and a conductive post to a carrier board, a front side of the first die and a front side of the second die facing the carrier board, the front side of the first die provided with a first bond pad, the front side of the second die provided with a second bond pad, a back side of the first die provided with an inductance element, the inductance element having a first electrical connection point, the first electrical connection point located on a side of the inductance element away from the first die, the conductive post disposed between the first die and the second die;

forming a plastic encapsulation layer on the carrier board, the plastic encapsulation layer encapsulating the first die, the second die, the inductance element and the conductive post, the first electrical connection point of the inductance element and a first end of the conductive post being both exposed from the plastic encapsulation layer;

forming a first conductive trace on a first surface of the plastic encapsulation layer, the first conductive trace connecting the first electrical connection point of the inductance element to the first end of the conductive post, the first surface of the plastic encapsulation layer representing a surface thereof that is disposed closer to the back side of the first die than to the front side of the first die;

removing the carrier board; and

forming a second conductive trace on a second surface of the plastic encapsulation layer, the second conductive trace connecting the second bond pad on the second die to a second end of the conductive post, the second surface of the plastic encapsulation layer opposing the first surface thereof.

2. The semiconductor packaging method according to claim 1, before fixing the first die, the second die and the conductive post to the carrier board, the semiconductor packaging method further comprising:

forming a first metal layer on a back side of a silicon wafer by an electroplating

process;

etching the first metal layer by an etching process to form the inductance element;
and

dicing the silicon wafer to form the first die.

3. The semiconductor packaging method according to claim 1, before fixing the first die, the second die and the conductive post to the carrier board, the semiconductor packaging method further comprising:

forming a seed layer on a back side of a silicon wafer by a sputtering process;

forming a first metal layer on the seed layer by an electroplating process;

etching the first metal layer and the seed layer by an etching process to form the inductance element; and

dicing the silicon wafer to form the first die.

4. The semiconductor packaging method according to claim 3, wherein the seed layer comprises a first seed layer, and forming the seed layer on the back side of the silicon wafer by the sputtering process comprises forming the first seed layer on the back side of the silicon wafer by sputtering copper, or

wherein the seed layer comprises a first seed layer and a second seed layer and forming the seed layer on the back side of the silicon wafer by the sputtering process comprises forming the second seed layer on the back side of the silicon wafer by sputtering titanium and forming the first seed layer on the second seed layer by sputtering copper.

5. The semiconductor packaging method according to any one of claims 1 to 4, further comprising:

forming a first protective layer on the front side of the first die, wherein a distance between a surface of the first protective layer away from the inductance element and a surface of the inductance element away from the first protective layer is smaller than a height of the conductive post; and

forming a second protective layer on the front side of the second die, wherein a distance between a surface of the second protective layer away from the inductance element and a surface of the inductance element away from the second protective layer

is smaller than the height of the conductive post.

6. The semiconductor packaging method according to any one of claims 1 to 5, wherein the conductive post is pre-formed, or

forming a second metal layer on the carrier board; and

etching the second metal layer by an etching process to obtain the conductive post.

7. The semiconductor packaging method according to any one of claims 1 to 6, wherein forming the plastic encapsulation layer on the carrier board comprises:

forming an encapsulation layer on the carrier board, the encapsulation layer encapsulating the first die, the second die, the inductance element and the conductive post; and

thinning the encapsulation layer to form the plastic encapsulation layer, wherein the first end of the conductive post is exposed from the plastic encapsulation layer.

8. The semiconductor packaging method according to claim 7, wherein forming the plastic encapsulation layer on the carrier board further comprises:

forming a first opening in which the first electrical connection point of the inductance element is exposed by performing a laser drilling process on the first surface of the plastic encapsulation layer.

9. The semiconductor packaging method according to claim 8, wherein forming first conductive trace on the first surface of the plastic encapsulation layer comprises:

forming a first conductive filled interconnect by filling a first conductive medium in the first opening and forming the first conductive layer on the first surface of the plastic encapsulation layer, wherein the first conductive filled interconnect is electrically connected to the first electrical connection point of the inductance element, and the first conductive layer is electrically connected to the first conductive filled interconnect; and

patterning the first conductive layer to form the first conductive trace,

wherein the first conductive filled interconnect and the first conductive layer are formed in the same process step.

10. The semiconductor packaging method according to any one of claims 1 to 9,

after the first conductive trace is formed on the first surface of the plastic encapsulation layer, the semiconductor packaging method further comprising:

forming a first dielectric layer on the first surface of the plastic encapsulation layer, the first dielectric layer covering at least the first conductive trace.

11. The semiconductor packaging method according to claim 5, further comprising: after the first protective layer is formed, before the first die is fixed to the carrier board, or after the carrier board is removed, forming, in the first protective layer, a second opening in which the first bond pad is exposed; and

after the second protective layer is formed, before the second die is fixed to the carrier board, or after the carrier board is removed, forming, in the second protective layer, a third opening in which the second bond pad is exposed.

12. The semiconductor packaging method according to claim 11, wherein forming the second conductive trace on the second surface of the plastic encapsulation layer comprises:

forming a second conductive filled interconnect by filling a second conductive medium in the second opening, forming a third conductive filled interconnect by filling a third conductive medium in the third opening, and forming a second conductive layer over the plastic encapsulation layer, the first protective layer and the second protective layer, the second conductive filled interconnect electrically connected to the first bond pad on the first die, the third conductive filled interconnect electrically connected to the second bond pad on the second die, the second conductive layer electrically connected to both the second and third conductive filled interconnects; and

patterning the second conductive layer to form the second conductive trace,

wherein the second conductive filled interconnect, the third conductive filled interconnect and the second conductive layer are formed in the same process step.

13. The semiconductor packaging method according to any one of claims 1 to 12, wherein the second conductive trace has a second electrical connection point, the second electrical connection point located on the side of the second conductive trace away from the first die, and wherein after the second conductive trace is formed on the

second surface of the plastic encapsulation layer, the semiconductor packaging method further comprises:

- forming a conductive bump at the second electrical connection point;

- forming a second dielectric layer on the second surface of the plastic encapsulation layer to form a plastic encapsulation body, wherein the second dielectric layer covers at least the second conductive trace and encapsulates the conductive bump, a surface of the conductive bump away from the first die being exposed from the second dielectric layer; and

- dicing the plastic encapsulation body to form a semiconductor package structure.

14. The semiconductor packaging method according to any one of claims 1 to 12, wherein the second conductive trace has a second electrical connection point, the second electrical connection point located on the side of the second conductive trace away from the first die, and wherein after the second conductive trace is formed on the second surface of the plastic encapsulation layer, the semiconductor packaging method further comprises:

- forming a conductive bump at the second electrical connection point;

- forming a second dielectric layer on the second surface of the plastic encapsulation layer to form a plastic encapsulation body, wherein the second dielectric layer covers at least the second conductive trace and encapsulates the conductive bump, a surface of the conductive bump away from the first die being exposed from the second dielectric layer;

- forming a surface finish layer on the exposed surface of the conductive bump; and

- dicing the plastic encapsulation body to form a semiconductor package structure.

15. A semiconductor package structure, comprising:

- a plastic encapsulation layer;

- a first die, a front side of the first die provided with a first bond pad, the first die disposed within the plastic encapsulation layer;

- a second die, a front side of the second die provided with a second bond pad, the second die disposed within the plastic encapsulation layer side by side with the first

die, wherein the front side of the first bond pad is oriented in the same direction as the front side of the second bond pad;

an inductance element disposed on the back side of the first die so as to be located between the first die and the plastic encapsulation layer, the inductance element having a first electrical connection point, the first electrical connection point located on the side of the inductance element away from the first die;

a conductive post disposed between the first die and the second die, the conductive post extending through the plastic encapsulation layer;

a first conductive trace disposed on a first surface of the plastic encapsulation layer and connecting the first electrical connection point of the inductance element to a first end of the conductive post that is exposed from the first surface of the plastic encapsulation layer, the first surface of the plastic encapsulation layer representing a surface thereof that is disposed closer to the back side of the first die than to the front side of the first die; and

a second conductive trace disposed on a second surface of the plastic encapsulation layer and connecting the second bond pad on the second die to a second end of the conductive post that is exposed from the second surface of the plastic encapsulation layer, the second surface of the plastic encapsulation layer opposing the first surface thereof.

16. The semiconductor package structure according to claim 15, further comprising a first protective layer and a second protective layer, the first protective layer covering the front side of the first die, the second protective layer covering the front side of the second die.

17. The semiconductor package structure according to claim 16, wherein the first protective layer is formed of one of a laser-reactive material and a photosensitive material, and wherein the second protective layer is formed of one of a laser-reactive material and a photosensitive material.

18. The semiconductor package structure according to any one of claims 15 to 17, further comprising a first dielectric layer and a second dielectric layer, the first dielectric layer disposed on the first surface of the plastic encapsulation layer so as to

cover at least the first conductive trace, the second dielectric layer disposed on the second surface of the plastic encapsulation layer so as to cover at least the second conductive trace.

19. The semiconductor package structure according to claim 18, further comprising a conductive bump disposed on the second conductive trace and encapsulated within the second dielectric layer, the conductive bump has a surface away from the first die that is exposed from the second dielectric layer.

20. The semiconductor package structure according to claim 19, further comprising a surface finish layer disposed on the exposed surface of the conductive bump.