

DRAM MEMORY CELL HAVING A VERTICAL BIPOLAR INJECTOR

FIELD OF THE INVENTION

The field of the invention is that of semiconductor devices, and more particularly that of memory devices comprising a plurality of memory cells.

The invention relates more particularly to a memory cell formed by a
5 field effect transistor FET with floating body, and a memory array comprising a plurality of memory cells of this type.

BACKGROUND OF THE INVENTION

Figure 1 shows a cross-section of a conventional floating body DRAM
10 (dynamic random access memory) memory cell.

The conventional floating body DRAM cell is formed in a silicon-on-insulator (SOI) substrate comprising a thin film of silicon 3 separated from the base substrate 1 by a buried oxide layer (BOX) 2. A floating body 4, a source region 5 and a drain region 6 are formed in the thin film 3 on top of the
15 BOX 2. A gate dielectric layer 7 and a gate electrode 8 are sequentially deposited on top of the floating body 4. The drain region 6 is connected to a bit line BL, the source region 5 is connected to a source line SL and the gate electrode 8 is connected to a word line WL.

The floating body is electrically insulated by the BOX, the gate dielectric
20 layer, the source region and the drain region. Because of this insulation, the floating body can store an electrical charge.

In a data write operation in such a transistor, the floating body uses an impact ionization phenomenon to store charges, which modifies the threshold voltage of the transistor. In a data read operation, the quantity of the current
25 flowing between the source and the drain of the transistor thus depends on the quantity of charges stored in the floating body.

In order to be able to perform a logic 1 state write operation (operation hereinafter called "write 1"), a relatively high voltage, of around 2.5 times the nominal power supply voltage VDD that has to be applied to the gate
30 electrode, must be applied to the bit line BL. Besides the fact that this high voltage is likely to damage the cell, it can also disrupt the operation of nearby

memory cells. The generation of this high voltage also requires dedicated circuitry implementing charge pumps.

One technique for reducing the surface area occupied by such a floating body DRAM memory cell is described in the document US 2004/0108532. This document proposes creating a memory cell by associating a floating body horizontal FET transistor and a horizontal bipolar transistor suitable for injecting charges into the floating body. The low storage capacity of the floating body is thus increased.

The horizontal bipolar transistor is more specifically arranged laterally to the FET transistor with the emitter (serving as injector) of the bipolar transistor formed in the substrate with a conductivity opposite to the latter, the base of the bipolar transistor being formed by the substrate and the collector of the bipolar transistor serving as floating body for the FET transistor.

With such an arrangement, the surface area of the memory cell is reduced to approximately $10F^2$. However, in this arrangement, the emitter and the base consume surface area so that an even greater reduction of the memory cell surface area remains an objective to those skilled in the art.

Moreover, this memory cell has the drawback that it is difficult to accurately control the voltage of the substrate serving as base for the bipolar transistor. Since the injector is, moreover, shared between two adjacent memory cells, the result is a risk of disturbances between these neighbouring cells.

It will therefore be understood that the memory cell according to the document US 2004/0108532 is not totally satisfactory, and that there is still a need to remedy the abovementioned drawbacks in the prior art.

BRIEF DESCRIPTION OF THE INVENTION

Embodiments of the invention seek to provide an improved memory cell that has a reduced surface area. According to a first aspect of the present invention, there is provided a memory cell produced on a substrate comprising:

- a horizontal FET transistor having a source connected to a source line, a drain connected to a bit line and a floating body between the source and the drain,
- an injector that can be controlled to inject a charge into the floating body of the FET transistor, the injector consisting of a bipolar transistor having an emitter connected to an injection line, a base and a collector formed by the floating body of the FET transistor,

wherein the emitter of the bipolar transistor is arranged so that the emitter/source assembly forms a vertical stack, the source of the FET transistor serving as the base for the bipolar transistor, and wherein the injection line runs below the surface of the substrate.

Some preferred, but nonlimiting, embodiments of this memory cell are as follows:

- the emitter is integrated in the source;
- the emitter is arranged in a bottom region of the source;
- the source comprises a strongly doped central region and a lightly doped peripheral region surrounding the central region, the emitter being arranged within the peripheral region of the source under the central region of the source;
- the emitter is arranged in a top region of the source;
- the source comprises a lightly doped top region and a strongly doped bottom region arranged below the top region, the emitter being integrated in the top region;
- the bottom region of the source is arranged below a buried insulating layer and is linked to the top region of the source via a connecting passage extending through the insulating layer;
- the emitter is arranged below the source;

- the emitter is arranged below a buried insulating layer and is linked to the source via a connecting passage extending through the insulating layer;
- the FET transistor also comprises a gate electrode recessed in the floating body and insulated from the latter by a dielectric layer;
- the emitter comprises a doped semiconductive material of conductivity opposite to that of the source;
- the cell is produced on a semiconductor-on-insulator substrate;
- the FET transistor is formed in a well produced in the top part of a bulk substrate.

According to another aspect of the invention, there is provided a memory array comprising a plurality of memory cells according to the first aspect of the invention.

The memory array can notably comprise a source line coupled to the source of each memory cell along a column of the array and an injection line parallel to the source line coupled to the emitter of each memory cell along said column.

According to yet another aspect of the invention, there is provided a method of controlling a memory cell according to the first aspect, wherein during a WRITE 1 operation for programming a logic 1 state,

a nominal write voltage is applied to the gate of the FET transistor, a voltage less than or equal to the nominal write voltage is applied to the drain of the FET transistor and a positive voltage is applied to the emitter of the bipolar transistor.

In a cell read operation, it is also possible to apply a fraction of the nominal write voltage to the gate of the FET transistor.

BRIEF DESCRIPTION OF THE DRAWING

Other aspects, aims and advantages of the present invention will become more apparent from reading the following detailed description of preferred embodiments of the latter, given by way of nonlimiting example and with reference to the appended drawings in which:

- Figure 1, already mentioned previously, represents a conventional floating body DRAM cell;
- Figure 2a represents a cross-sectional view of a memory cell according to one possible embodiment of the first aspect of the invention;
- Figure 2b represents a possible topology of a memory array employing memory cells of Figure 2a ;
- Figure 2c represents a circuit diagram equivalent to the memory cell of Figure 2a ;
- Figure 3a represents a possible embodiment according to the invention of a memory cell using a partially depleted FET transistor on a semiconductor-on-insulator substrate;
- Figure 3b represents a possible embodiment according to the invention of a memory cell using an FET transistor on a bulk substrate;
- Figure 3c represents another possible embodiment of a memory cell according to the invention in which the injection line is buried below the insulating layer;
- Figure 3d represents another possible embodiment of a memory cell according to the invention in which the source line is buried below the insulating layer;

- Figure 3e represents a possible topology of a memory array employing memory cells of Figure 3d;
- Figures 4a and 4b respectively represent, on the basis of equivalent circuit diagrams, an operation for programming a logic 0 state in a conventional DRAM cell and in a DRAM cell according to the invention;
- Figures 5a and 5b respectively represent, on the basis of equivalent circuit diagrams, an operation for programming a logic 1 state in a conventional DRAM cell and in a DRAM cell according to the invention;
- Figures 6a and 6b respectively represent, on the basis of equivalent circuit diagrams, an operation to read the logic state stored by a conventional DRAM cell and by a DRAM cell according to the invention;
- Figures 7a and 7b respectively represent, on the basis of equivalent circuit diagrams, an operation to hold the logic state stored in a conventional DRAM cell and in a DRAM cell according to the invention;
- Figure 8 represents another possible topology of a memory array employing memory cells according to the invention.

DETAILED DESCRIPTION OF THE INVENTION

Referring to Figure 2a, a cross-sectional view of a memory cell according to a preferred embodiment of the first aspect of the invention is represented. This cell comprises an FET transistor having a source S, a drain D and a floating body FB between the source and the drain, and an injector that can be controlled to inject a charge into the floating body FB of the FET transistor.

The memory cell is, in this case, produced on a semiconductor-on-insulator SeOI substrate, preferentially a silicon-on-insulator SOI substrate.

The drain D and the source S are preferentially in contact with the buried oxide layer BOX so that the FET transistor is fully depleted.

The source S can thus be shared between two adjacent memory cells (along a line of a memory array extending in the plane of Figure 2a; the columns of the memory array extending perpendicularly to the plane of

Figure 2a). Such sharing makes it possible to reduce the surface area occupied by a memory cell.

As can be seen in Figures 3a and 3b, the invention is not, however, limited to a fully depleted memory cell, but also extends to a memory cell on
5 partially depleted SeOI (Figure 3a) and to a memory cell produced on a bulk substrate (Figure 3b).

In the case of Figures 3a and 3b, and in a manner conventionally known per se, it is necessary to isolate the cells along a line of the memory array in order to create the floating body effect.

10 In the case of Figure 3a, this is conventionally done by lateral isolating trenches 13 (according to the shallow trench isolation STI technique) extending depthwise from the surface of the substrate to the BOX.

In the case of Figure 3b, this is conventionally done by lateral isolating trenches 14 extending depthwise from the surface of the substrate, and by
15 isolating the memory cell in a well 15 produced in the top part of the bulk substrate and delimited by the trenches 14. The FET transistor is situated in the semiconductive well 15, the conductivity of which is identical to that of the channel, which makes it possible to isolate it from the substrate. The well can also be arranged on a layer 16 of the substrate having an opposite
20 conductivity.

Returning to the description of Figure 2a, the injector consists of a bipolar transistor having an emitter 15, a base and a collector formed by the floating body FB of the FET transistor.

In the context of the invention, the emitter 15 of the bipolar transistor is
25 arranged so that the source S of the FET transistor serves as the base for the bipolar transistor. It will be noted that controlling the voltage of the source serving as the base for the bipolar transistor is easier than controlling the voltage of the substrate serving as the base for the bipolar transistor of the memory cell presented in the document US 2004/0108532.

The FET transistor is a horizontal transistor and the emitter of the bipolar transistor is more specifically arranged facing the source of the FET transistor so that the emitter/source assembly forms a vertical stack.

In a preferred embodiment, the emitter is connected to an injection line
5 that runs below the surface of the memory cell, thereby not consuming surface area.

The emitter 15 of the bipolar transistor can notably be integrated in the source of the FET transistor. According to a first variant embodiment represented in Figure 2a, the emitter 15 is integrated in the source 21, 22 in a
10 bottom region thereof. According to a second variant embodiment represented in Figure 3d, the emitter 35 is integrated in the source 31, 32 in a top region thereof.

Referring to Figure 2a, the source conventionally comprises in a manner known per se a strongly doped central region 21 (for example N+) and a lightly doped peripheral region 22 (for example N-) surrounding the
15 central region. The main purpose of the strongly doped central region 21 is to ensure the contact with the source line SL while the lightly doped peripheral region 22 mainly contributes to the operation of the FET transistor. Thus, it is the lightly doped region 22 which is used in the context of the invention as
20 the base for the bipolar transistor.

In the context of this variant, the emitter 15 is arranged so as to be positioned below the central region 21 of the source while being in contact with the peripheral region 22 of the source and isolated from the floating body FB by the peripheral 22 of the source. The emitter is, in this case, totally
25 integrated in the source electrode between the central 21 and peripheral 22 regions thereof.

In the case of a memory cell made of fully depleted SeOI (see Figure 2a), and unlike the case of a memory cell made of partially depleted SeOI (Figure 3a) or a memory cell on bulk substrate (Figure 3b), the BOX
30 can help to insulate the emitter 15 from the floating body.

It will be noted that the drain D can also have a strongly doped central region 11 (N+ in the example) and a lightly doped peripheral region 12 (N- in the example) surrounding the central region.

In a manner known conventionally per se, the drain D is linked to a bit line BL. This bit line BL can extend along a line of the memory array, coming into contact with the drain of each of the memory cells arranged along this line.

As can be seen in Figure 2b, the source S is connected to a source line SL. This source line SL typically extends perpendicularly to the bit line BL, coming into contact with the source (typically the strongly doped region of the source) of each of the memory cells arranged along a column of the memory array.

In the case of Figures 2a and 2b, the source line SL therefore runs immediately below the surface of the SeOI substrate.

Moreover, in the case of Figures 2a and 2b in which the source is shared between two adjacent cells, a single source line SL can be used to address the source of the two memory cells.

The emitter 15 is linked to an injection line IL which extends parallel to the source line SL so as to address the memory cells arranged along a column of the memory array.

It will be understood from the foregoing that, in the case of Figure 2a, the injection line IL is arranged below the source line SL. The result of this is a particularly compact arrangement inasmuch as the injection line IL does not consume any surface region.

Figure 2b represents a topology of a memory array according to the invention with the source line SL shared between two adjacent cells. This arrangement is thus even more compact.

Based on the topology of Figure 2b, the surface area of the memory cell can thus be reduced to approximately $4 F^2$ in the case where a standalone memory is being developed. While this cell is not totally insensitive to disturbances, nevertheless the level of disturbances remains low and in any

case less than the level of disturbance encountered with conventional memory cells.

5 In the case of an embedded memory, given that the requirements are greater for the transistors (need to provide spacers to avoid cross-excitation phenomena), the surface area occupied by the transistors is greater. A memory cell surface area of the order of $15 F^2$ to $18 F^2$ is then achieved. It does, however, offer the benefit of being totally insensitive to the disturbances.

10 Another possible topology, less compact but totally insensitive to disturbances, is represented in Figure 8. In this topology, the word line WL controls two adjacent physical rows which share a common source line SL. This particular arrangement eliminates most of the sources of mutual disturbances since the cells situated on this double word line WL are all used and it can be legitimately assumed that the write circuits are more powerful
15 than the disturbances. On the other hand, the two cells situated one on top of the other must, imperatively, be connected to two different bit lines BL1, BL2, otherwise their information would become mixed during the WL access. This has a direct impact on the surface area of the cell since it must be wide enough to leave two lines of metal alongside one another. While the latter
20 point is generally prohibitive for standalone memories, it is, on the other hand, perfectly legitimate in the case of embedded memories inasmuch as the surface area of the cell is around $4F \times 4F = 16 F^2$.

As is represented in Figure 2a, the FET transistor also has a gate electrode positioned above the floating body, on the surface of the memory
25 array, and insulated from the floating body by a dielectric layer. The gate electrode is linked to a word line WL which typically extends along a column of the memory array.

According to another embodiment not represented, the gate electrode is recessed in the floating body and insulated therefrom by a dielectric layer. An
30 RCAT (recessed channel array transistor) type transistor is thus defined.

Figure 2c is a circuit diagram equivalent to the memory cell according to the first aspect of the invention. In this figure, the FET transistor – in this case N – has the reference 9 and the bipolar transistor – in this case PNP – has the reference 10. As previously discussed, the source of the FET transistor 9 connected to the source line SL serves as the base for the bipolar transistor 10, while the body of the FET transistor 9 serves as the collector for the bipolar transistor 10.

Referring to Figure 3d illustrating another variant embodiment, the emitter 25 is integrated in the source 31, 32 in a top region thereof.

In the context of this variant, the source S comprises a lightly doped top region 32 and a strongly doped bottom region 31 arranged below the top region, the emitter 35 being integrated in the top region 32.

As represented in Figure 3d, the bottom region 31 of the source can in particular be arranged below a buried insulating layer in the substrate, for example the BOX layer in the case of an SeOI substrate, while being linked to the top region 32 of the source via a connecting passage 33 extending through the insulating layer.

The strongly doped bottom region 31 of the source (N+ doping in the example concerned) is more specifically arranged, below the insulating layer, in a region 36 of the substrate that has an opposite conductivity (P- region in the example).

In the context of this variant, the source line SL is buried; it can notably be buried directly below the insulating layer BOX as represented in Figure 3d. The emitter 35 of the bipolar transistor is linked to an injection line IL which extends directly below the surface of the substrate (this injection line IL is provided instead of the source line of a conventional cell) and which, because of this, is easier to access. Also in this variant, the vertical stack of the source and the emitter has the particular consequence that the injection line consumes no surface area.

Figure 3e represents a possible topology of a memory array employing memory cells of Figure 3d. In this topology, the source line SL extends

parallel to the injection line IL along a column of the memory array, while being buried below the injection line, under the BOX layer. In this variant embodiment, the injection line IL is simpler to access.

Figure 3c represents another possible embodiment, in which the vertical stack of the source and the emitter is obtained by arranging the emitter 25 below the source 21, 22. It will be noted that this embodiment corresponds to the variant of Figure 3d with the emitter and the strongly doped region of the source simply interchanged.

In practice, in this other embodiment, the emitter 25 (P+) is buried under the insulating layer, in a region 26 of the substrate that has an opposite conductivity (N- in the example) and is linked to the peripheral region 22 of the source via a connecting passage 23 extending through the insulating layer.

The source line SL conventionally extends immediately below the surface of the substrate, while the injection line IL extends under the BOX layer parallel to the source line SL. Thus, the injection line IL does not consume any surface area.

To return to the description of the invention, the injection line is preferentially produced using a doped semiconductive material. This is a P-type doping (notably, a P+ doping) of the material of the substrate in the examples represented in the figures in which the FET transistor is of the N type (P-type floating body). It will be understood that the invention is not limited to an N FET transistor, but also extends to the case of a P FET transistor (N-type floating body).

By using the techniques conventionally used in CMOS technology to produce such a doping of the substrate in order to produce the injection line IL, the latter does not need to be metallized so that metal wiring can be avoided.

Figures 4a-4b, 5a-5b, 6a-6b and 7a-7b show the equivalent circuit diagram of Figure 2a in order to compare the different programming, read and hold operations for a conventional memory cell of the type of that

illustrated in Figure 1 (Figures 4a, 5a, 6a and 7a) and for a memory cell according to the invention (Figures 4b, 5b, 6b and 7b).

In these various figures:

- Figures 4a and 4b illustrate the WRITE 0 operation for programming the logic 0 state,
- Figures 5a and 5b illustrate the WRITE 1 operation for programming the logic 1 state,
- Figures 6a and 6b illustrate the READ operation for reading the logic state,
- Figures 7a and 7b illustrate the HOLD operation for holding the logic state.

The tables below illustrate examples of voltages that have to be applied to the various lines to control the cell and carry out these various operations.

	BL	WL	SL
WRITE 1	2.5 VDD	VDD	0 V
WRITE 0	- 0.25 VDD	VDD	0 V
READ	0.25 VDD	VDD	0 V
HOLD	0 V	0 V	0 V

Table 1 – Memory cell of Figure 1

	BL	WL	SL	IL
WRITE 1	0.75 VDD	VDD	0 V	0.75 VDD
WRITE 0	- 0.25 VDD	VDD	0 V	0 V
READ	0.25 VDD	0.5 VDD	0 V	0 V
HOLD	0 V	0 V	0 V	0 V

Table 2 – Memory cell according to the invention

It will first of all be observed that the voltage that has to be applied to the word line WL to carry out the read operation READ is, moreover, lowered to a fraction of the nominal power supply voltage VDD, for example to 0.5 VDD. This makes it possible to lower the overall consumption level of the cell. Furthermore, inasmuch as this voltage is situated between the two

threshold voltage levels ("0" and "1"), the read selection leads to the presence of a current for the lowest threshold voltage (in principle, "0" by convention), and the absence of current in the other case. The design of the detection amplifier is then reduced to a "simple" comparator that is much easier to design than if there are two currents of different amplitudes that must be compared to references, references that must be known and that must be trusted.

Moreover, as already described in the introduction, a voltage of around 2.5 times the nominal write voltage VDD must be applied to the drain of the conventional memory cell to carry out the WRITE 1 operation.

By using the injection of charge into the floating body by the injector, the invention makes it possible to lower the voltage needed to carry out this WRITE 1 operation. In particular, the voltage that has to be applied to the drain of a memory cell according to the invention is less than or equal to the nominal voltage VDD, for example equal to 0.75 VDD as indicated in Table 2 above.

The fact that all the programming operations are carried out with low voltages applied to all the power supply lines 1 offers a number of advantages.

First of all, the power consumption is reduced and the design of the peripheral circuits is simplified. In particular, the circuitry needed to generate high voltages (2.5 VDD for the conventional memory cell, notably for the WRITE 1 operation) is not necessary.

Moreover, by reducing the voltage, damage to the memory cell is avoided. Disturbance of the neighbouring cells is also avoided.

Thus, a disturbance potentially generated via the bit line BL in a write operation on a neighbouring cell corresponds to a voltage of 0.75 VDD (WRITE 1) or -0.25 VDD (WRITE 0) on the bit line BL in the example in question (with WL=SL=IL=0V). These relatively low voltages are not likely to generate significant disturbances.

A disturbance potentially generated via the word line WL in a WRITE 1 write operation on a neighbouring cell corresponds to respective voltages of VDD on the word line WL and of 0.75 VDD on the injection line IL (and with BL=SL=0V). An injection of charge (holes in the example described here) into the floating body via the bipolar transistor is then likely to occur.

In a WRITE 0 write operation on a neighbouring cell, WL is at VDD while BL=SL=IL=0 V. The bipolar transistor (PNP type in the example described here) is then OFF and all the holes are likely to be evacuated via at negative bit line.

In order to simply overcome these disturbance phenomena, a choice can be made to not remain passive by writing to the stressed cells given that they are located on the active word line WL (which is tantamount to carrying out valid WRITE operations on all the cells along WL by applying the appropriate voltages to all the corresponding bit lines). This conditions the partitioning of the memory (requires all the cells along the word line WL to belong to the same word) without, however, this posing any problem given that all the stressed cells can be used directly by the application. In practice, if the word is wider, the information bit rate is greater and ultimately the consumption is lower.

It will have been understood from the foregoing that the invention is not limited to a memory cell according to its first aspect, but also extends to a memory array comprising a plurality of memory cells according to the first aspect of the invention, and to a method of controlling such a memory cell.

CLAIMS

1. Memory cell produced on a substrate, comprising:

- a horizontal FET transistor having a source connected to a source line, a drain connected to a bit line and a floating body between the source and the drain,
- an injector that can be controlled to inject a charge into the floating body of the FET transistor, the injector consisting of a bipolar transistor having an emitter connected to an injection line, a base and a collector formed by the floating body of the FET transistor,

wherein the emitter of the bipolar transistor is arranged so that the emitter/source assembly forms a vertical stack, the source of the FET transistor serving as the base for the bipolar transistor, and wherein the injection line runs below the surface of the substrate.

2. Memory cell according to Claim 1, in which the emitter is integrated in the source.

3. Memory cell according to Claim 2, in which the emitter is arranged in a bottom region of the source.

4. Memory cell according to Claim 3, in which the source comprises a strongly doped central region and a lightly doped peripheral region surrounding the central region, and in which the emitter is arranged within the peripheral region of the source under the central region of the source.

5. Memory cell according to Claim 2, in which the emitter is arranged in a top region of the source.

6. Memory cell according to Claim 5, in which the source comprises a lightly doped top region and a strongly doped bottom region arranged below the top region, and in which the emitter is integrated in the top region.
7. Memory cell according to Claim 6, in which the bottom region of the source is arranged below a buried insulating layer and is linked to the top region of the source via a connecting passage extending through the insulating layer.
8. Memory cell according to Claim 1, in which the emitter is arranged below the source.
9. Memory cell according to Claim 8, in which the emitter is arranged below a buried insulating layer and is linked to the source via a connecting passage extending through the insulating layer.
10. Memory cell according to one of Claims 1 to 9, in which the FET transistor also comprises a gate electrode recessed in the floating body and insulated from the latter by a dielectric layer.
11. Memory cell according to one of Claims 1 to 10, in which the emitter composes a doped semiconductive material of conductivity opposite to that of the source.
12. Memory cell according to one of Claims 1 to 11, produced on a semiconductor-on-insulator substrate.
13. Memory cell according to one of Claims 1 to 11, in which the FET transistor is formed in a well produced in the top part of a bulk substrate.

14. Memory array comprising a plurality of memory cells according to any one of Claims 1 to 13.

15. Memory array according to claim 14, wherein the source line is coupled to the source of each memory cell along a column of the array and the injection line is parallel to the source line and coupled to the emitter of each memory cell along said column.

16. Method of controlling a memory cell according to any one of claims 1-13, wherein during a WRITE 1 operation for programming a logic 1 state, a nominal write voltage is applied to the gate of the FET transistor, a voltage less than or equal to the nominal write voltage is applied to the drain of the FET transistor and a positive voltage is applied to the emitter of the bipolar transistor.

17. Method according to Claim 16, in which, during a READ operation for reading the logic state of the cell, a fraction of the nominal write voltage is applied to the gate of the FET transistor.