AUXILIARY VIDEO DATA SLICER

Field of the Invention

The present invention relates to detection of information that may be present in a video signal during blanking or overscan intervals.

Background of the Invention

A video signal typically includes vertical display intervals, or fields, having a plurality of horizontal line intervals, e.g. 262.5 lines per field in NTSC video systems. The beginning of each vertical and horizontal interval is identified by respective vertical and horizontal sync pulses that are included in a composite video signal. During a portion of each vertical interval, information in the video signal may not be intended for display. For example, a vertical blanking interval spans approximately the first 20 horizontal line intervals in each field. In addition, several line intervals adjacent to the vertical blanking period, e.g. line 21, may be within an overscan region of a video display and will not be visible.

The lack of displayed image information during blanking and overscan intervals makes it possible to insert an auxiliary information component, e.g. teletext or closed caption data, into these intervals. Standards such as Federal Communications Commissions (FCC) Regulations define the format for each type of auxiliary information including the positioning of the information within a vertical interval. For example, the present closed captioning standard (see e.g. 47 CFR §§ 15.119 and 73.682) specifies that digital data corresponding to ASCII characters for closed captioning must be in line 21 of field 1.

The first step in extracting auxiliary video information is to locate the auxiliary information. Various approaches may be used depending on the type of information involved. For example,

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recognition of teletext data characteristics such as the framing code pattern is a method of locating teletext data. Closed caption information in line 21 may be located by counting video lines, e.g. counting horizontal sync pulses.

After the auxiliary video information is located, the information must be extracted. In the case of digital data, a "data slicer" may be used to convert the video signal into binary data. A data slicer typically operates by comparing the video signal level to a reference level known as the slicing level. For video levels that exceed the slicing level, the comparison produces a logic 1. Video levels that are less than the slicing level produce a logic 0. As an example, closed caption data in line 21 of the video signal may exhibit a signal amplitude range of 0 IRE to 50 IRE. For a signal range of 0 IRE to 50 IRE, a slicing level of 25 IRE would be appropriate.

A constant slicing level may not be adequate for all video signals. Video signal levels may vary depending on the source of the video signal. Utilizing a constant slicing level with varying video signal levels may bias the extracted data undesirably toward logic 0 or logic 1 resulting in erroneous data extraction. For example, if the video signal range is 0 IRE to 20 IRE rather than 0 IRE to 50 IRE, a slicing level of 10 IRE rather than 25 IRE is desirable. If 25 IRE were used as a slicing level for a signal range of 0 IRE to 20 IRE, a logic 1 would never be extracted because the signal never exceeds the slicing level. Thus, it is desirable to adapt the slicing level to the amplitude of the input video signal.

Another possible problem with a constant slicing level is that the switching threshold level of components used in a data slicer may vary as a function of temperature, supply voltage, or manufacturer. As an example, a CMOS inverter may be constructed using PMOS and NMOS field effect transistors (FET). Matching the current conducting characteristics of these devices makes it possible to design the switching threshold to be

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approximately midway between the power supply extremes of the inverter. The current conducting characteristics of the devices in the inverter may, however, vary as a result of temperature and supply voltage changes or different integrated circuit fabrication techniques causing the switching threshold to change. If the amplitude of an auxiliary video data signals is low, e.g. 50 IRE (approximately 350 mV for a 1 V peak-to-peak video signal), changes of component switching thresholds with respect to a fixed slicing level might significantly decrease the accuracy of data extraction. It may be desirable, therefore, to adapt the slicing level to compensate for component variations.

The format of an auxiliary information component such as closed caption data includes provisions to facilitate an adaptive slicing level function. For example, a closed caption signal in line 21 of field 1 begins after the "back porch" interval with a 7 cycle burst of a sinusoidal reference signal designated the "run-in clock" (RIC). The closed caption data standard establishes that the amplitude of the RIC signal is identical to the amplitude of the data signal that occurs during the latter half of the line 21 interval. Thus, the average of the RIC signal amplitude is an appropriate slicing level for the subsequent data signal.

Auxiliary data such as closed-caption data may not exist in all video signals. For example, switching between different video sources may result in switching from one signal having closed caption data to another source that does not. If no auxiliary video data exists, there will be no RIC signal to serve as the basis for modifying the slicing level. Attempting to adjust the slicing level when a RIC signal is not present may produce an incorrect slicing level.

Current video signal processing approaches typically involve digital signal processing functions implemented in digital integrated circuits (IC). It may be desirable to include a data slicer function in a digital signal processing IC. Analog approaches to data slicing (see e.g. U.S. Patent No. 4,115,811 (Goff) and U.S.

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Patent No. 4,358,790 (Summers)) typically involve analog functions such as analog signal comparators that may be difficult to implement in a digital IC's. However, certain digital data slicers (see e.g. U.S. Patent No. 4,656,513 (Langenkamp) and U.S. Patent No. 4,858,007 (Schweer et al.)) may require complex digital circuitry that may undesirably require an excessive percentage of the available chip area in a complex digital signal processing IC.

Summary of the Invention

In accordance with the principles of the present invention, a data slicer for extracting auxiliary video information from a video signal comprises a device responsive to the video signal for producing an output signal having one of two values. The output signal has a first value when the video signal exceeds a threshold level and has a second level when the video signal is less than the threshold level. A DC signal component at the video signal input of the output signal producing device may be modified to decrease the difference between the magnitude of the DC component and the threshold level. Modification of the DC component occurs during a predetermined interval in response to periodic variations in a reference signal that is included in the auxiliary video information signal. The predetermined interval has a duration that is substantially equal to a predetermined integral number of cycles of the reference signal.

Brief Description of the Drawing

Figure 1 shows an example of an auxiliary video data waveform.

Figure 2 shows, partially in block diagram form and partially in schematic form, an embodiment of the invention.

Figures 3 and 4 show signal waveforms useful for understanding the operation of the embodiment in Figures 2.

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Detailed Description of the Drawing

The operation of the exemplary embodiment of the invention shown in Figure 2 will be explained in the context of closed caption data that complies with the FCC standard (see e.g. 47 CFR §§ 15.119 and 73.682) closed caption signal depicted in Figure 1. As discussed further below, the invention may also be applicable to the extraction of other forms of auxiliary video data such as teletext.

In Figure 2, a composite video signal VIDEO is input to data slicer 210. Data slicer 210 converts auxiliary video data, e.g. closed caption data, included in signal VIDEO into a digital data stream identified in Figure 2 as signal DSOUT. Logic 0 and logic 1 levels in signal DSOUT represent levels of signal VIDEO that are less than and exceed, respectively, the slicing level of data slicer 210.

Data slicer 210 includes input coupling capacitor 211 for coupling video signal VIDEO to the input of buffer amplifier 213 at node A in Figure 2. Signal DSOUT is produced at the output of buffer amplifier 213. A signal VA at node A includes an AC component VAAC from video signal VIDEO and a DC component VADC. If signal VA exceeds a switching threshold voltage VT of buffer amplifier 213, a logic 1 value is generated on signal DSOUT. Values of signal VA below switching threshold voltage VT cause buffer amplifier 213 to generate a logic 0 on signal DSOUT. Thus, the slicing level with respect to signal VA is at switching threshold voltage VT. However, the slicing level of interest for purposes of accurately converting auxiliary video data (represented by AC component VAAC) into logic values is the slicing level with respect to AC component VAAC. As described below, the slicing level with respect to AC component VAAC may be controlled by varying DC component VADC.

The slicing level of data slicer 210 with respect to AC component VAAC is determined by the relationship between DC

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component VADC and switching threshold voltage VT. The most reliable slicing of AC component VAAC into digital logic 1 and logic 0 values occurs when the average value of the peak-to-peak amplitude of signal VAAC is at voltage VADC and voltage VADC equals switching threshold voltage VT (see e.g. Figure 3(A)). Under this condition, signal VAAC extends equally above and below switching threshold voltage VT and undesirable biasing of the slicing operation in favor of a particular logic state is prevented.

The average value of signal VAAC may not equal switching threshold voltage VT as desired. For example, switching threshold voltage VT may vary as discussed above. If voltage VADC is less than switching threshold voltage VT' (Figure 3(B)), the average value of signal VAAC is offset below switching threshold voltage VT by an amount equal to VT minus VADC. Similarly, values of voltage VADC above voltage VT produce an offset of signal VAAC above voltage VT. Under either offset condition, the mid-point of the peak-to-peak range of signal VAAC is not at switching threshold voltage VT and inaccurate data slicing of signal VAAC may result. As described below, voltage VADC is controlled to cause the average of the peak-to-peak range of signal VAAC to be at switching threshold voltage VT.

In the exemplary embodiment shown in Figure 2, voltage VADC is controlled via a feedback path comprising tristate inverting buffer 215 and resistor 212. The feedback path is coupled between data slicer output DSOUT and the input of buffer 213. Voltage VADC is modified when the feedback path is conducting (tristate inverting buffer 215 enabled). A control circuit comprising control microprocessor 200, NAND gate 241, inverter 242, and counter 220 controls the operation of the described functions.

It may be desirable to initialize voltage VADC at certain times, e.g. following turn on of the system. Initialization to a voltage such as the expected switching threshold voltage of

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buffer 213 may decrease the time required to complete the adjustment of voltage VADC. Various approaches to initialization are possible. For illustrative purposes, the embodiment shown in Figure 2 includes initialization circuit 230. When initialization is desired control microprocessor 200 enables initialization circuit 230 by forcing signal INIT to a logic 1. Signal INIT at logic 1 causes PMOS transistor 231 to conduct, thereby forcing node A to approximately voltage VINIT. The value of VINIT may be, for example, the expected value of switching threshold voltage VT. The initialization circuitry is then disabled (signal INIT forced to logic 0).

Voltage VADC may be modified via low impedance paths through either initialization circuit 230 or the feedback path comprising resistor 212 and tristate inverting buffer 215. After voltage VADC is established the DC level may be retained substantially unchanged at node A for an extended period of time if buffer 213 has a high input impedance (e.g. a CMOS inverter) and if the low impedance paths coupled to node A are disabled. Leakage current effects, e.g. through disabled initialization circuit 230, may be ignored if voltage VADC is adjusted periodically in the manner described below.

When adjustment of voltage VADC is to occur, e.g. following initialization or periodically, control µP 200 enables the feedback loop by forcing signal RICGATE to a logic 0. For reasons explained below, the adjustment of voltage VADC is timed to occur when the RIC signal is active on signal VIDEO. At this time, the RIC signal also appears at node A as signal VAAC. Microprocessor 200 evaluates synchronization signal SYNC and line indicator signal LINE to determine when auxiliary video data and a RIC signal should be present on signal VIDEO. Signal RICGATE is forced to logic 0 to enable tristate inverting buffer 215 during the RIC interval. As explained below, adjustment of voltage VADC should occur during a substantially integral number of cycles of the RIC signal. The RICGATE signal is established by µP 200 to

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span a substantially integral number of RIC cycles to provide the desired adjustment interval.

When the feedback loop is enabled, oscillations may appear on signal DSOUT. The frequency of the oscillations is determined by the delay around the feedback loop. For example, a waveform having a period equal to double the loop delay will experience positive feedback (360 degree phase shift) around the inverting feedback loop, thereby introducing the potential for oscillations. Oscillations on signal DSOUT during the RIC interval do not adversely affect auxiliary video data capture circuitry coupled to signal DSOUT. Auxiliary video data occurs during the data interval of the auxiliary video signal when the feedback loop is disabled. Thus, the oscillations will not exist on signal DSOUT when data capture is in progress.

Any oscillations that may exist will have a negligible effect on the described approach to controlling voltage VADC. As discussed below, a waveform symmetrical with respect to switching threshold voltage VT is intentionally established at node A when the slicing level is adjusted. An oscillation waveform will be substantially symmetrical at node A and will not, therefore, adversely affect slicing level adjustment that occurs in response to a symmetrical waveform.

When tristate inverting buffer 215 is enabled, voltages at node A that are above the threshold of buffer 213 will produce logic levels of 1 and 0 at the outputs of buffer 213 and tristate inverting buffer 215, respectively. Assuming the voltage represented by logic 0 at the output of tristate inverting buffer 215 is less than the voltage at node A, the low impedance path to ground represented by the logic 0 at the output of tristate inverting buffer 215 will act to discharge capacitor 211 and decrease the voltage at node A. If the voltage at node A is below the threshold of buffer 213, logic levels of 0 and 1 will be produced at the outputs of buffer 213 and tristate inverting buffer 215, respectively. Assuming the logic 1 voltage at the

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output of tristate inverting buffer 215 is greater than the voltage at node A, capacitor 211 will charge via resistor 212 and the voltage at node A will increase. Thus, the voltage at node A will tend toward the switching threshold level of buffer 213 when the feedback loop is enabled.

If the signal at node A has an AC component VAAC (e.g. in response to signal VIDEO) when the feedback loop is enabled, the variations of signal VAAC may affect voltage VADC. If signal VAAC is symmetrical about signal VADC during the feedback interval, voltage VADC will change during the feedback interval in a manner that will cause voltage VADC to be substantially equal to switching threshold voltage VT of buffer 213. In Figure 3(B), for example, signal VAAC is symmetrical about voltage VADC during the interval shown. However, signal VAAC is not symmetrical about switching threshold voltage VT. As Figure 3(B) shows, signal VAAC is less than switching threshold voltage VT for a greater period of time than it is above switching threshold voltage VT. As a result, the above-described operation of the feedback loop will act to increase voltage VADC for a greater interval than the interval when voltage VADC is being decreased. The net effect will be an increase in voltage VADC. If voltage VADC is greater than voltage VT rather than less than voltage VT as in Figure 3(B), the net effect will be a decrease in voltage VADC. In either case, the operation of the feedback loop acts to decrease the magnitude of the difference between voltages VADC and VT.

If signal VAAC is symmetrical about voltage VADC during the feedback interval, the net change in voltage VADC will continue (assuming the feedback loop is enabled for a sufficient interval) until voltage VADC substantially equals voltage VT. Signal VAAC is then symmetrical about voltages VADC and VT (see e.g. Figure 3(A). Thus, activating the feedback loop during an interval encompassing a symmetrical waveform of sufficient duration will cause voltage VADC to be at both the switching

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threshold voltage of buffer 213 and the midpoint of the signal range. Therefore, data slicing will occur at the mid-point of the range of the symmetrical signal. If the symmetrical signal is a RIC signal, data slicing will also occur at the mid-point of the range of the data signal that follows the RIC signal because the amplitude of the RIC signal is equal to the amplitude of the data signal.

In the present exemplary embodiment, signal VAAC is made symmetrical with respect to switching voltage VT during the feedback interval by timing the feedback interval to span a substantially integral number of cycles of the RIC signal. This condition is depicted in Figure 3 where 5 cycles of a RIC waveform occur while feedback is enabled. For a RIC signal in a closed caption signal, approximately five cycles of the 503 kHz RIC signal will occur during 10 μs. Thus, enabling the feedback loop by setting signal RICGATE to logic 0 for 10 μs when the RIC signal is active will provide the desired symmetrical reference waveform at node A in Figure 2. The RICGATE signal period may be timed by μP 200 to coincide with the RIC signal based on synchronizing signals SYNC and LINE and the timing specified in the FCC specification for closed caption signals (see e.g. 47 CFR §§ 15.119 and 73.682).

The interval required to adjust voltage VADC to equal voltage VT may exceed the duration of an integral number of cycles of the RIC signal within one line 21 interval. The described exemplary adaptive slicing level system includes charging and discharging capacitor 211 via resistor 212. The time constants associated with the charging and discharging operation determine how rapidly the voltage at node A will change. A relatively long time constant in comparison to the RIC interval (e.g. capacitor and resistor values of 1 μF and 10 kΩ, respectively) combined with an initial voltage at node A that differs significantly from the desired value will prevent the voltage at node A from reaching the desired value during one RIC signal interval. It may be necessary, therefore, to activate the feedback network during more than one

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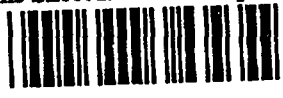
occurrence of the RIC signal. One approach to this problem is to close the feedback loop and adjust the slicing level during every RIC interval. This approach simplifies the control circuitry and insures that any leakage current effects at node A will be corrected by the repetitive adjustment of the slicing level. If leakage current effects are not significant, slicing level adjustment could be enabled for a predetermined number of RIC intervals sufficient to overcome the time constants of the circuit and then disabled. Any leakage effects could be overcome by periodic readjustment of the slicing level.

If signal VIDEO is certain to include auxiliary video data having the desired reference or RIC signal, the slicing level may be adapted as described above. If, however, the presence of auxiliary video data is uncertain, it may be desirable to include a feature to verify that the RIC signal is present during the feedback enabling interval. If the feedback loop is enabled and no symmetrical reference is present, an inaccurate slicing level may be generated.

Counter 220 is included in the exemplary embodiment shown in Figure 2 for the purpose of verifying the presence of the RIC signal. Counter 220 is cleared when signal RESET at the output of inverter 242 is at logic 1 in response to signal RICCNT being at logic 0. Counting is enabled when signals RICCNT and RICWND are at logic 1 because signal RICCNT at logic 1 deactivates (forces to logic 0) signal RESET and signal RICWND at logic 1 enables pulses on signal DSOUT to clock counter 220 via AND gate 250. Signals RICCNT and RICWND are also logically combined in NAND gate 241 to generate signal RICGATE for controlling enabling of the feedback loop.

When enabled, counter 220 counts pulses occurring on signal DSOUT. For the above-described case of a 10 μs feedback interval, five cycles of signal RIC should occur during the feedback interval. As a result, five pulses corresponding to the five peaks of the RIC signal should occur on signal DSOUT. If the RIC signal is

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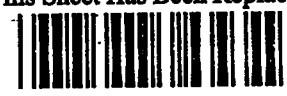


present as expected, count value CNTVAL should be equal to five after the end of the counting interval. Count value CNTVAL is evaluated by μP 200. If count value CNTVAL is not five as expected, μP 200 may produce a control signal (not shown in Figure 2) indicating to the video signal processing system that auxiliary video data was not present as expected. The system may respond by, for example, ceasing auxiliary video data processing, or by delaying processing until another video source (e.g. a different program or channel) that may contain auxiliary video data is selected, or by repeating the test on the present signal after a delay.

The described control arrangement including signals RICCNT, RICWND, and RICGATE prevents counter 220 from counting while the feedback loop is enabled. The above-described oscillations that are produced on signal DSOUT when the feedback loop is enabled would cause count value CNTVAL to be an inaccurate indication of the presence of the RIC signal. More specifically, the counter would count the peaks of the oscillation waveform rather than the peaks of the RIC waveform.

Enabling of the feedback loop and enabling of the counter are synchronized to avoid inaccurate count values as follows. Signal RICWND defines the duration of the feedback (or counting) interval. Signal RICCNT indicates whether feedback or counting will occur. The feedback loop is enabled (signal RICGATE at logic 0) and the counter is disabled when signal RICWND is at logic 1 and signal RICCNT is at logic 0 (signal RESET at logic 1). Counting is enabled and the feedback loop is disabled when signal RICWND is at logic 1 and signal RICCNT is at logic 1. A possible sequence of operation of the system might include initializing the slicing level, activating the feedback loop (counter disabled) to adapt the slicing level (initially assume the RIC signal is present), enabling the counter (disabling the feedback) during one window interval, and evaluating the count to determine if the RIC signal is present.

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An example of the operation of signals RICWND and RICCNT is shown in Figure 4. Two separate waveforms for signal DSOUT are shown in Figure 4. The upper DSOUT waveform depicts the DSOUT signal when signal RICCNT is at logic 0. In this case, the feedback loop is enabled to adjust the slicing level during the interval when RICWND is at logic 1. Oscillations may exist on signal DSOUT when the feedback loop is enabled causing signal DSOUT to be undefined as shown in the upper DSOUT waveform. In the lower DSOUT waveform, signal RICCNT is at logic 1 which disables the feedback loop. As a result, signal DSOUT pulses in response to the RIC signal during the interval when signal RICWND is at logic 1. Thus, accurate counting of the pulses on signal DSOUT is possible during the interval established by the pulse on signal RICWND if signal RICCNT is at logic 1.

Although the lower DSOUT waveform in Figure 4 indicates that signal RICCNT is at a fixed level during the line 21 interval, an alternative approach (not shown in Figure 4) would be to produce a pulse to logic 1 on signal RICCNT when counting is to be enabled. For example, the desired synchronization of the counter and feedback loop would be provided if a pulse on signal RICCNT is timed such that the pulse on signal RICWND occurs during the period of the RICCNT pulse.

Although the invention has been described in the context of closed caption data, the invention may also be applicable to other forms of auxiliary video data, e.g. teletext. In the case of other forms of data, the system may require certain modifications. For example, the teletext standard permits teletext data to appear on a number of video lines, e.g. lines 17 to 20. Thus, for a teletext system, signal LINE shown in Figure 2 may have to be generated by means other than the above-described line counter.

The operation of the disclosed system may be modified in other ways to accommodate alternative auxiliary data formats. As an example, if the format of the reference signal (RIC

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signal in the described embodiment) changes, the disclosed hardware (or software of μP 200) can easily be changed to operate correctly with various data formats. Modifications of this type may include adapting the system for reference signals having characteristics (e.g. amplitude, waveform, frequency) that differ from the described exemplary RIC signal. In particular, the duration of the feedback interval may easily be changed to span an integral number of cycles for RIC signals of other frequencies. In addition, the feedback interval may span an integral number of cycles other than five as described above.

Other modifications of the invention may also be evident to one skilled in the art. For example, functions shown as separate hardware blocks in Figure 2, e.g. counter 220, may be incorporated into the operations performed by μP 200.

These and other modifications are intended to be within the scope of the invention as defined by the following claims.

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CLAIMS:

1. In a system for processing a video signal (VIDEO), said video signal including an auxiliary information signal component occurring during at least one of a plurality of periodic horizontal line intervals of said video signal, said auxiliary information signal component having a data signal component and a reference signal component (RIC) varying periodically at a predetermined frequency, apparatus comprising:

means (213) having an input coupled to said video signal for producing an output signal (DSOUT) having one of first and second values, said output signal having said first value when said video signal exceeds a predetermined threshold level (VT) and said output signal having said second value when said video signal is less than said predetermined threshold level; and

means (212,215,230) for modifying the value of a DC signal component (VADC) at said input of said output signal producing means in response to said periodic variations of said reference signal component occurring during a predetermined interval defined by a control signal (RICWND) such that the magnitude of the difference between the value of said predetermined threshold level and the value of said DC signal component is decreased, said predetermined interval spanning a predetermined substantially integral number of cycles of said periodic variation of said reference component; and

means (200,220,250) for generating said control signal in response to a synchronizing signal (LINE) indicative of the occurrence of said horizontal line intervals containing said auxiliary information.

2. The apparatus of Claim 1, further comprising said output signal producing means (213) comprises an amplifier.

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3. The apparatus of Claim 1, further comprising said DC signal component modifying means comprises feedback means (212,215) responsive to said control signal (RICWND) for coupling said output signal (DSOUT) to said input of said output signal producing means (213) during said predetermined interval.

4. The apparatus of Claim 1, further comprising said control signal generating means (200,220,250) comprises a microprocessor (200).

5. The apparatus of Claim 1, further comprising said control signal generating means comprises means (200,220) responsive to said video signal for verifying that said auxiliary information signal component is present in said video signal.

6. The apparatus of Claim 5, further comprising said verifying means comprises:

means (220) for counting amplitude variations in said video signal during a counting interval defined by said control signal to occur when said reference signal component (RIC) is expected to occur and to have a duration equal to said predetermined substantially integral number of said periodic variations of said reference signal component; and

means (200) for evaluating said count to determine if said predetermined substantially integral number of said periodic variations of said reference signal component occurred during said counting interval.

7. The apparatus of Claim 6, further comprising said counting interval is an interval other than said predetermined interval when said DC signal component modifying means is operative.

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