

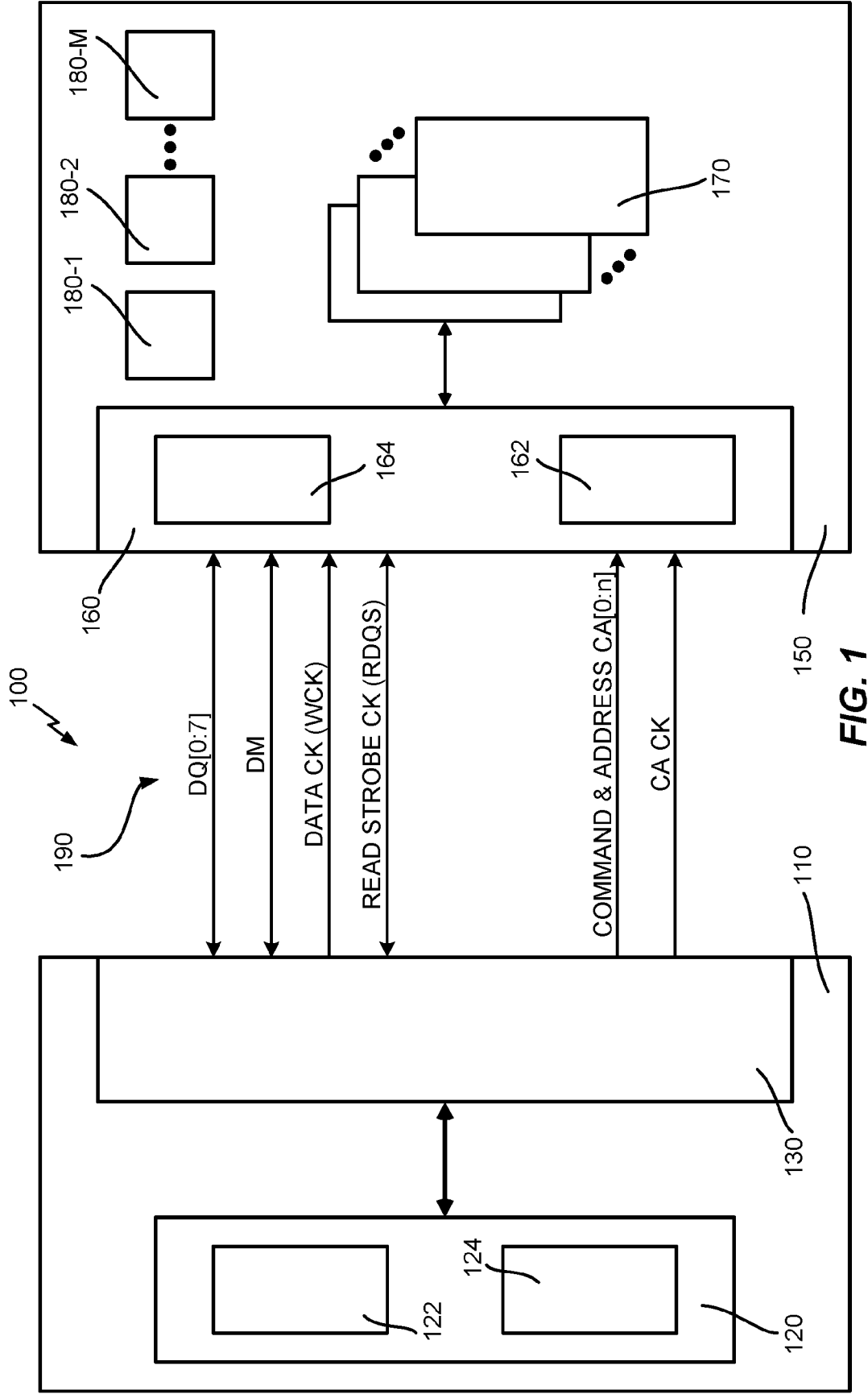


FIG. 1

MRxx definition (OP: Operand)

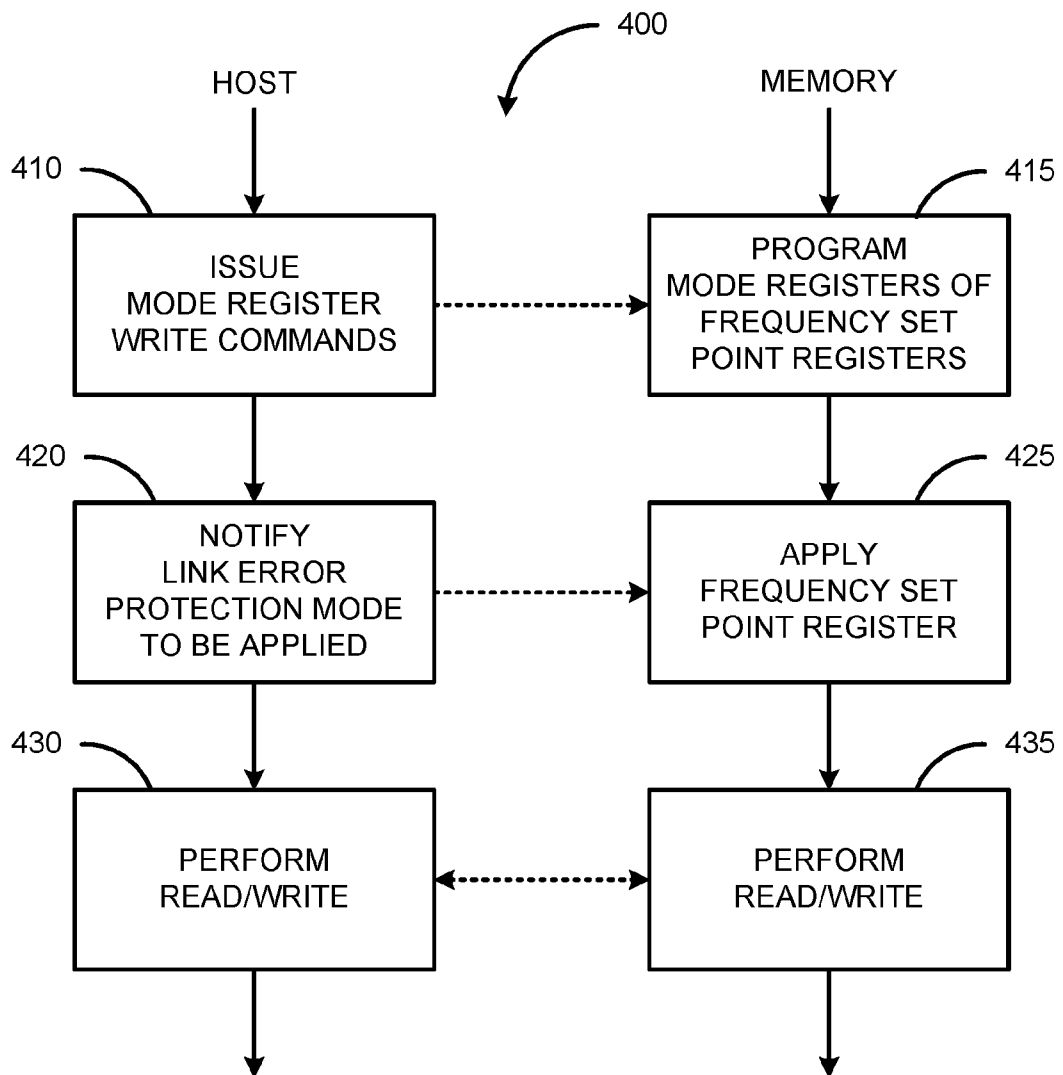
OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Reserved for Future Use				RECC		WECC	

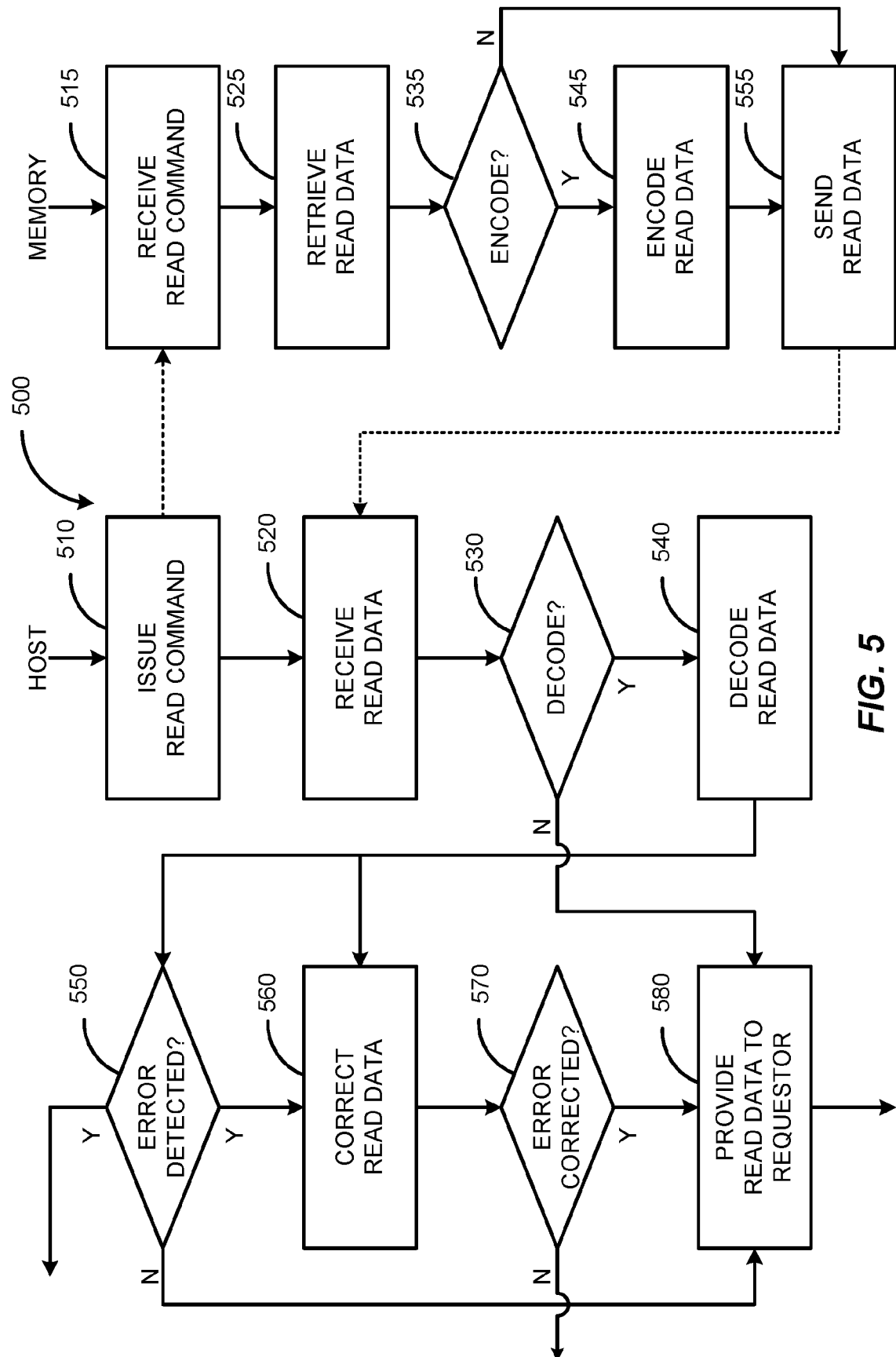
Function	Register Type	Operand	Operation
WECC	Write only	OP[1:0]	00: Write link ECC disable 01: Write link ECC correction enable 10: Write link ECC detection enable 11: Write link ECC correction & detection enable
RECC	Write only	OP[3:2]	00: Read link ECC disable 01: Read link ECC correction enable 10: Read link ECC detection enable 11: Read link ECC correction & detection enable

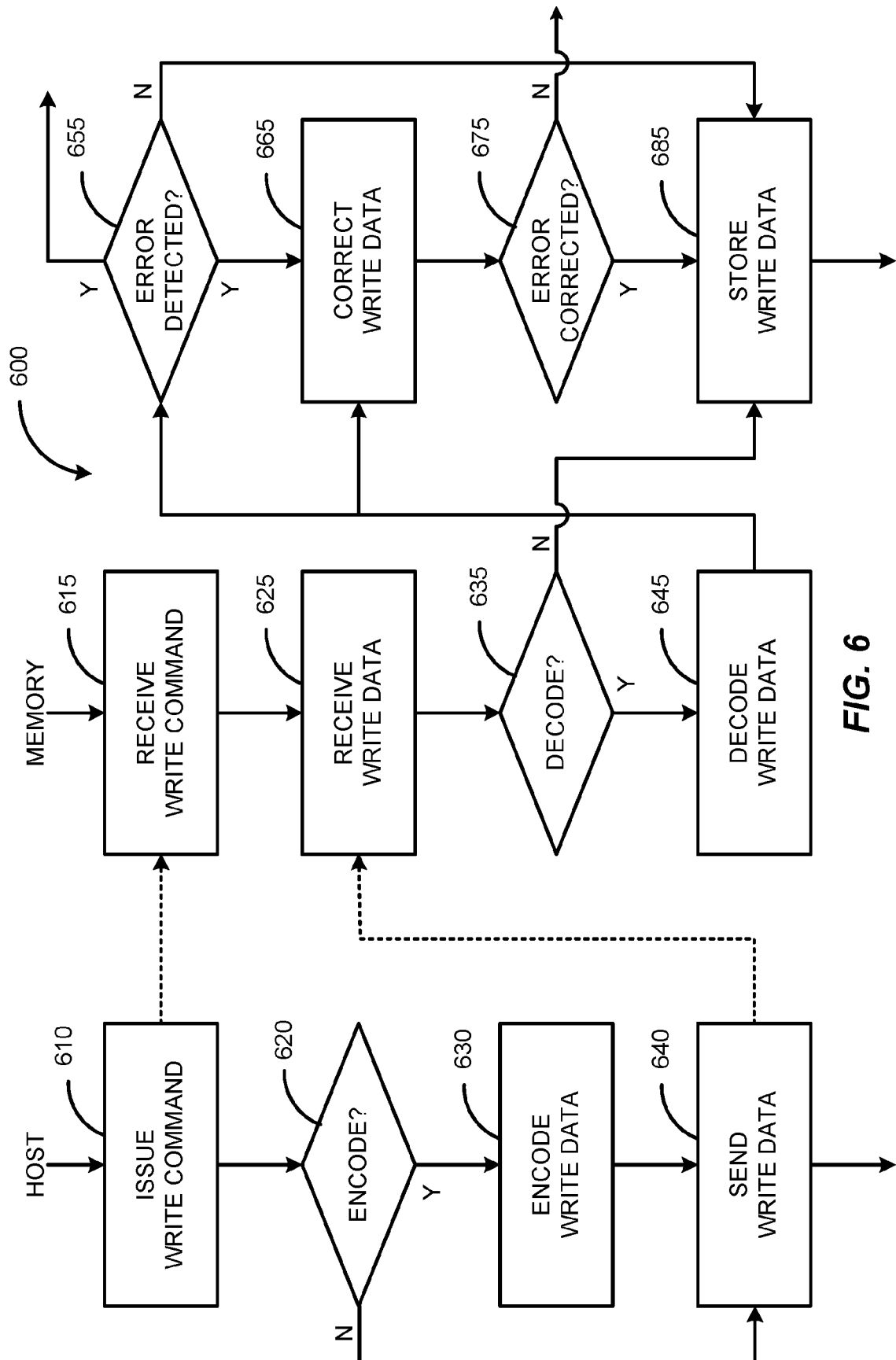
FIG. 2

FSP	OP[7:0]
MRxx FSP[0] (low speed)	XXXX0000
MRxx FSP[1] (middle speed)	XXXX0101
MRxx FSP[2] (high speed)	XXXX1101

FIG. 3

**FIG. 4**





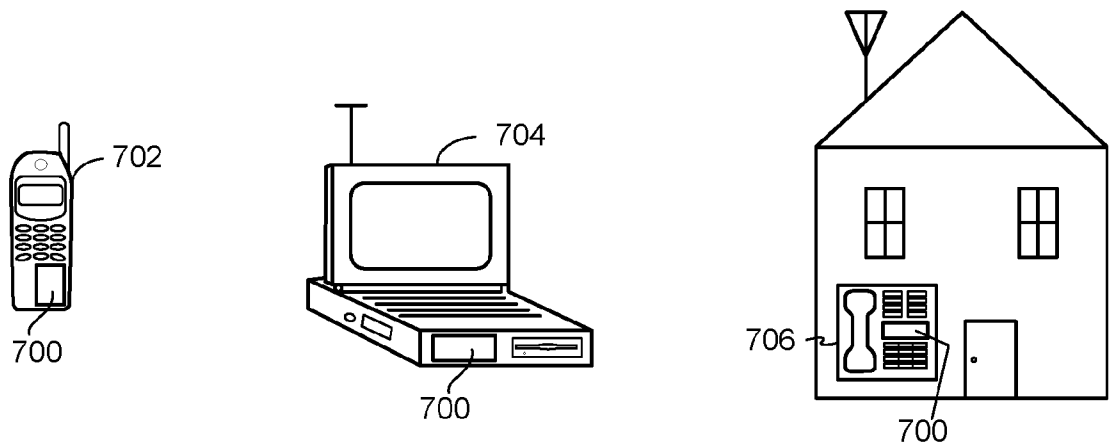


FIG. 7