

FIG. 1

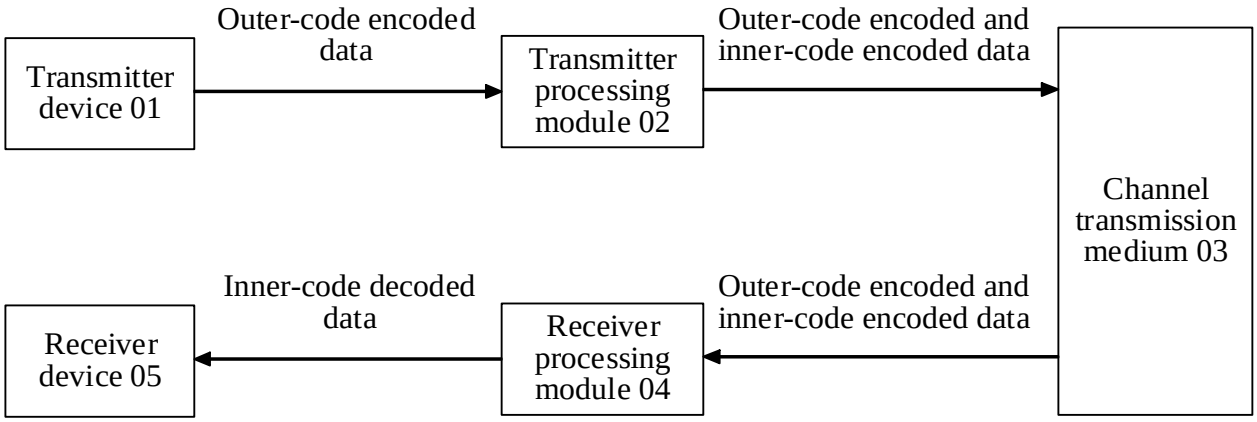


FIG. 2

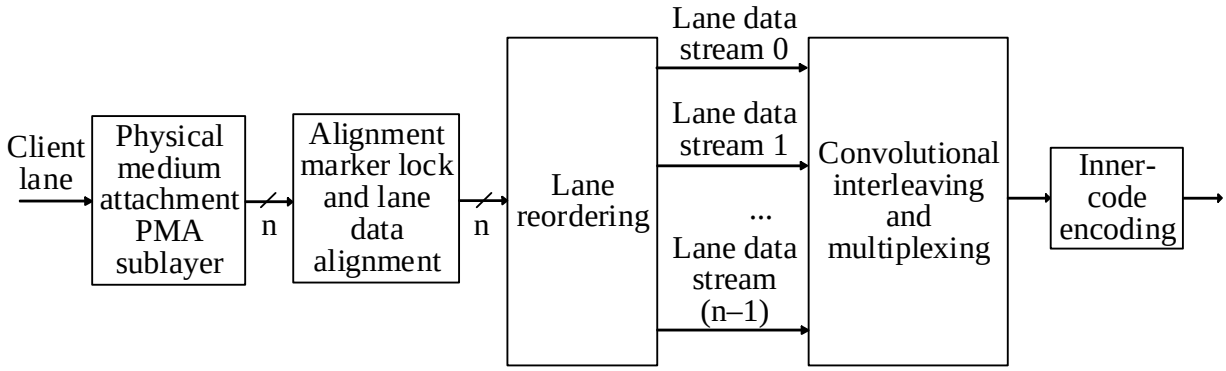


FIG. 3(a)

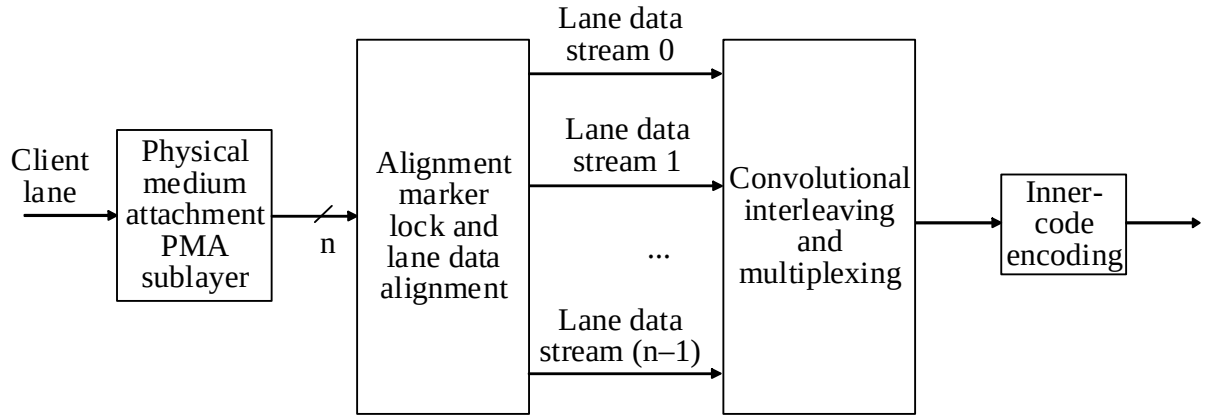


FIG. 3(b)

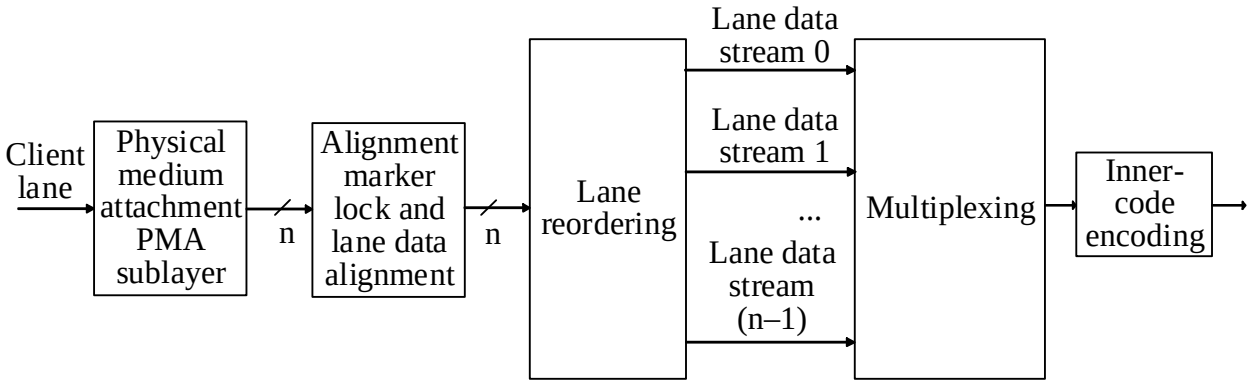


FIG. 3(c)

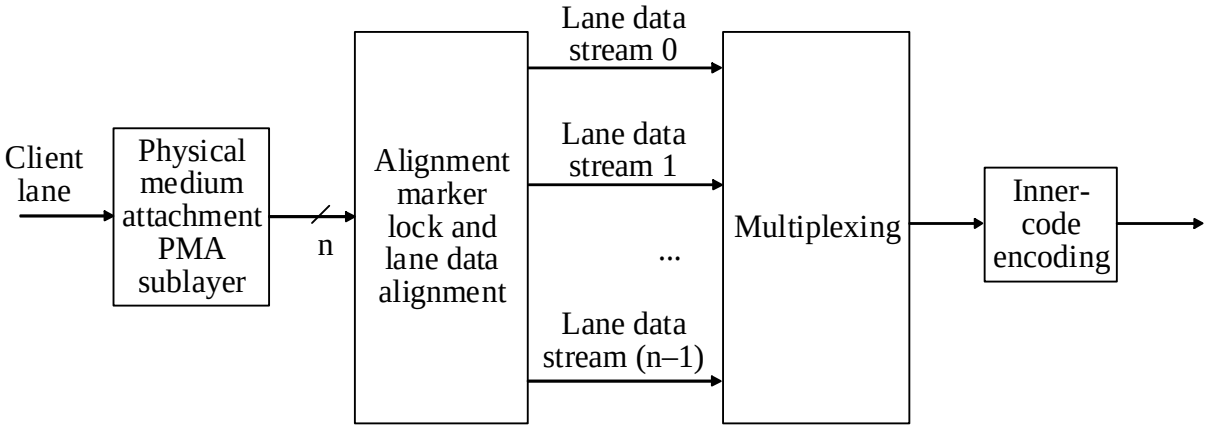


FIG. 3(d)

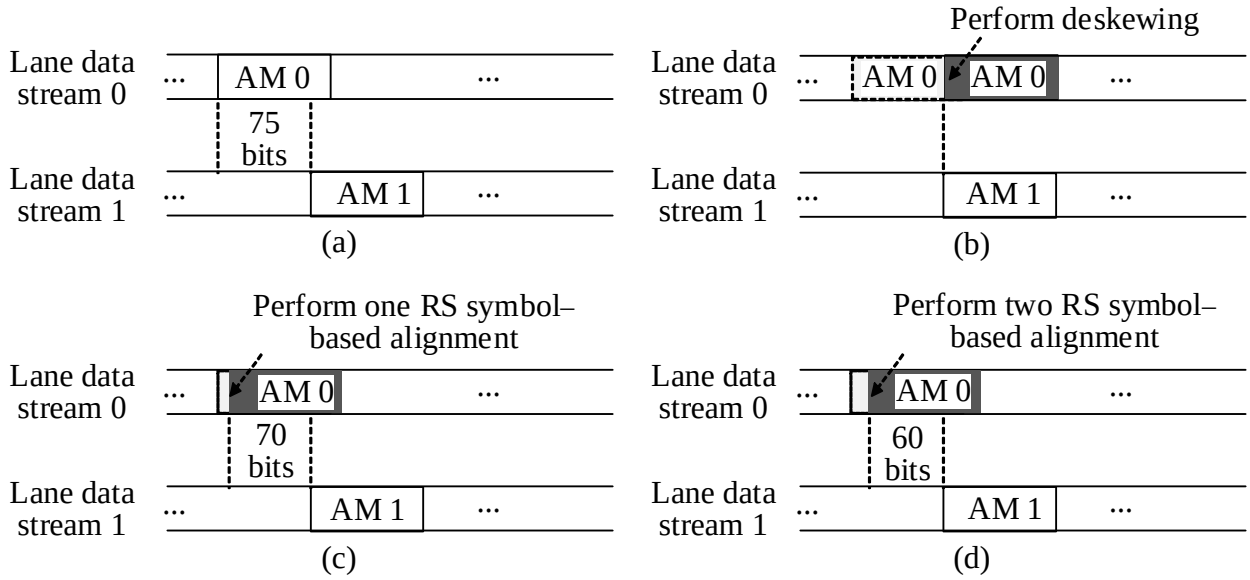

Lane data stream 0
Lane data stream 1
AM 0
AM 1
75 bits
(a)
Perform deskewing
AM 0
AM 0
AM 1
(b)
Perform one RS symbol–based alignment
70 bits
(c)
Perform two RS symbol–based alignment
60 bits
(d)

FIG. 3(e)

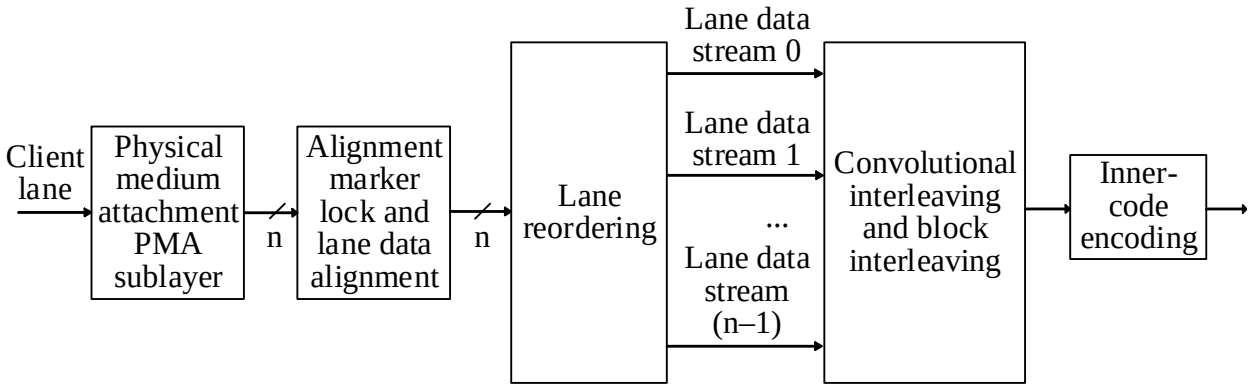

Client lane
Physical medium attachment PMA sublayer
n
Alignment marker lock and lane data alignment
n
Lane reordering
Lane data stream 0
Lane data stream 1
...
Lane data stream (n–1)
Convolutional interleaving and block interleaving
Inner-code encoding

FIG. 3(f)

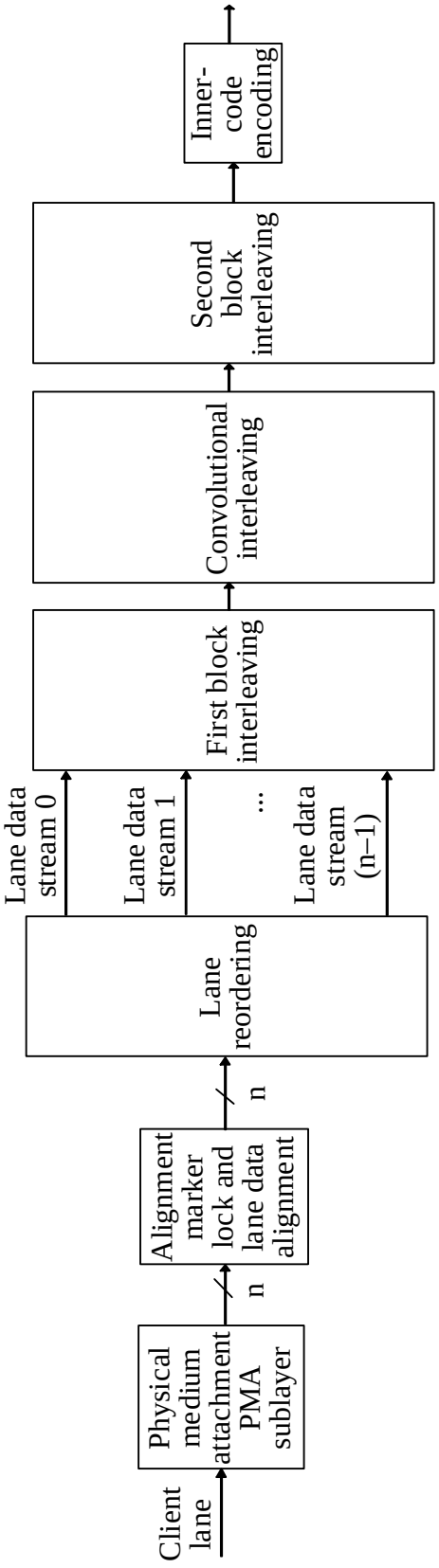

Client lane
Physical medium attachment PMA sublayer
n
Alignment marker lock and lane data alignment
n
Lane reordering
Lane data stream 0
Lane data stream 1
...
Lane data stream (n–1)
First block interleaving
Convolutional interleaving
Second block interleaving
Inner-code encoding

FIG. 3(g)

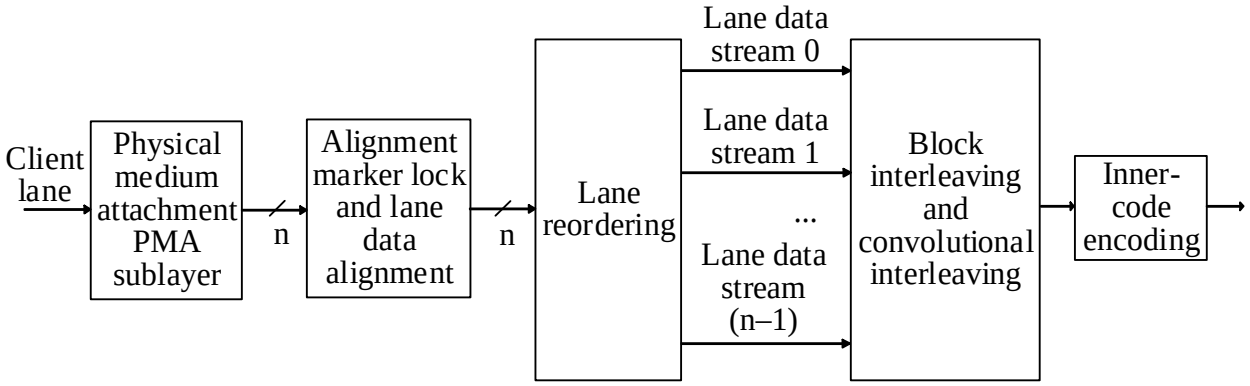


FIG. 3(h)

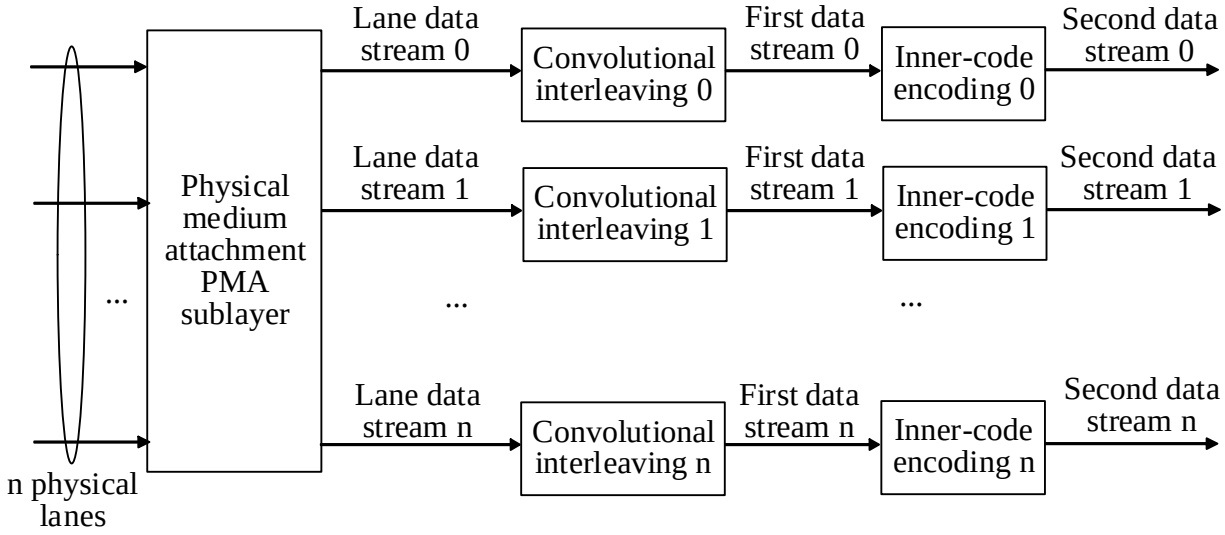


FIG. 3(i)

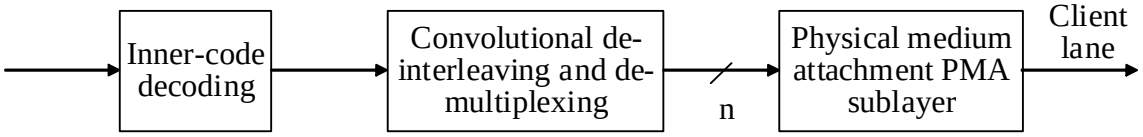


FIG. 4(a)

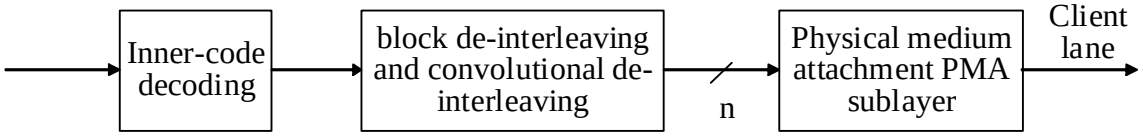


FIG. 4(b)

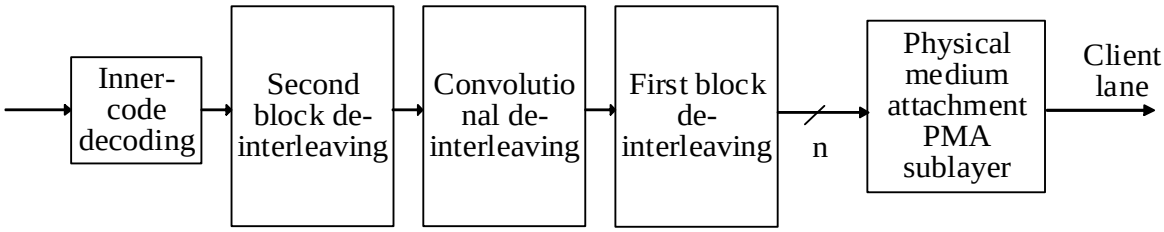

Inner-code decoding
Second block de-interleaving
Convolutional de-interleaving
First block de-interleaving
n
Physical medium attachment PMA sublayer
Client lane

FIG. 4(c)

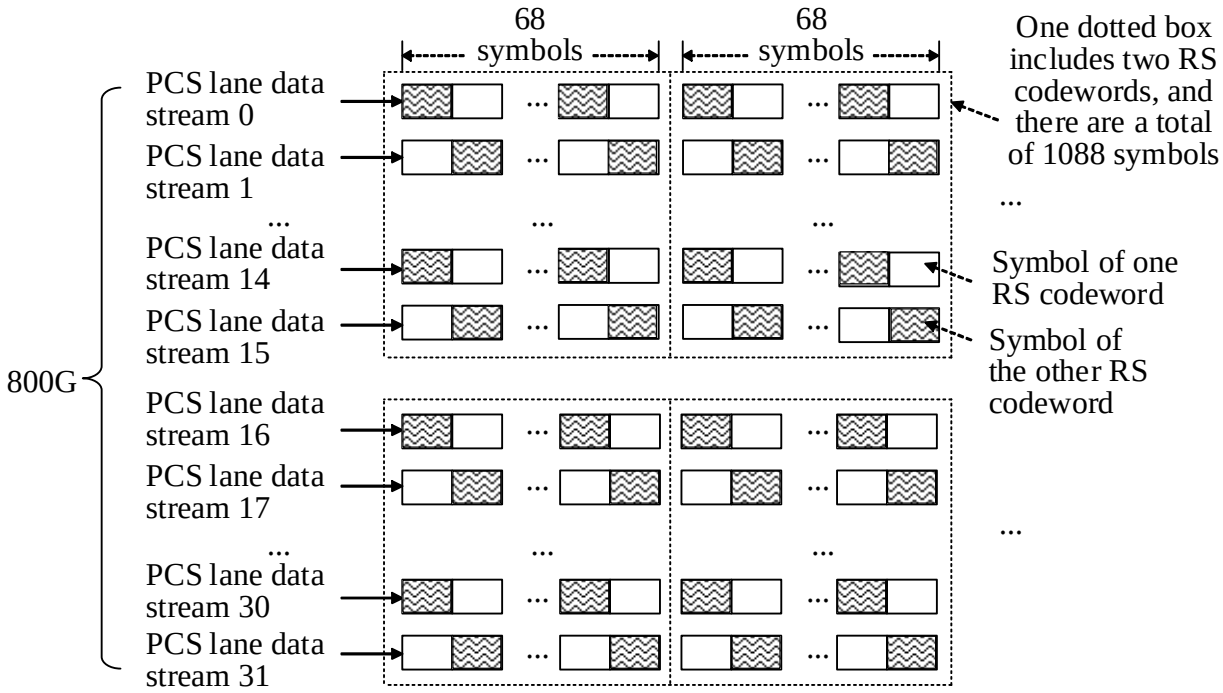

68 symbols
68 symbols
One dotted box includes two RS codewords, and there are a total of 1088 symbols
PCS lane data stream 0
PCS lane data stream 1
PCS lane data stream 14
PCS lane data stream 15
PCS lane data stream 16
PCS lane data stream 17
PCS lane data stream 30
PCS lane data stream 31
800G
Symbol of one RS codeword
Symbol of the other RS codeword

FIG. 5

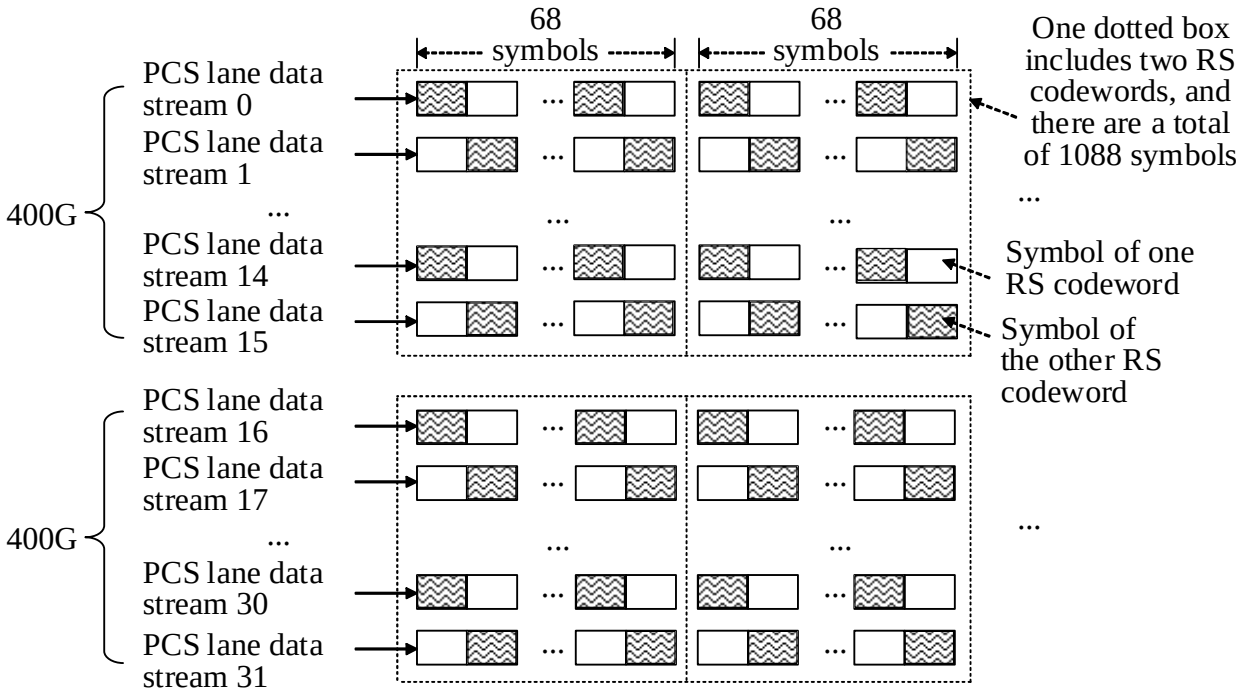

68 symbols
68 symbols
One dotted box includes two RS codewords, and there are a total of 1088 symbols
400G
PCS lane data stream 0
PCS lane data stream 1
PCS lane data stream 14
PCS lane data stream 15
Symbol of one RS codeword
Symbol of the other RS codeword
400G
PCS lane data stream 16
PCS lane data stream 17
PCS lane data stream 30
PCS lane data stream 31

FIG. 6

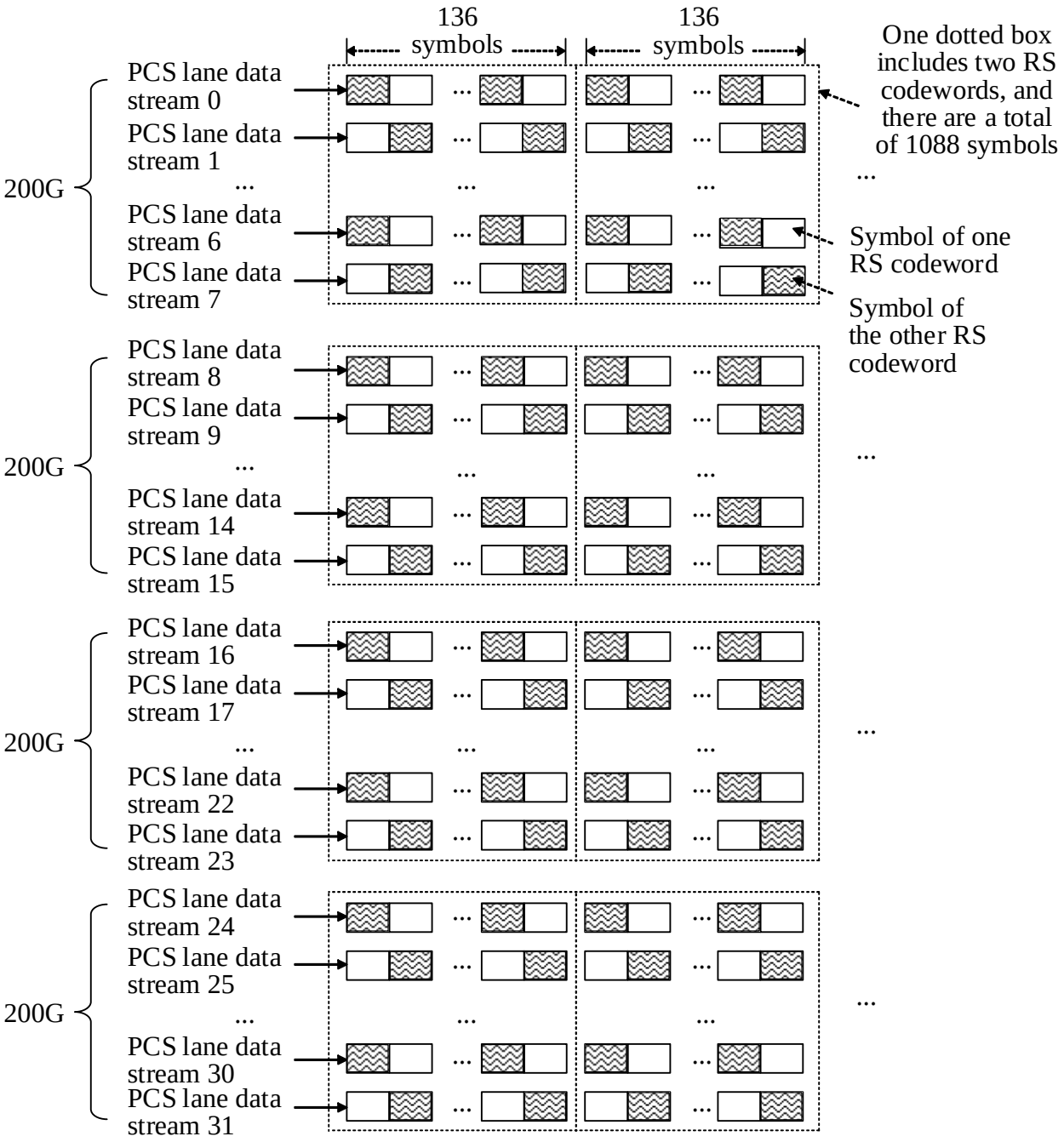

136 symbols
136 symbols
One dotted box includes two RS codewords, and there are a total of 1088 symbols
Symbol of one RS codeword
Symbol of the other RS codeword
200G
PCS lane data stream 0
PCS lane data stream 1
PCS lane data stream 6
PCS lane data stream 7
PCS lane data stream 8
PCS lane data stream 9
PCS lane data stream 14
PCS lane data stream 15
PCS lane data stream 16
PCS lane data stream 17
PCS lane data stream 22
PCS lane data stream 23
PCS lane data stream 24
PCS lane data stream 25
PCS lane data stream 30
PCS lane data stream 31

FIG. 7

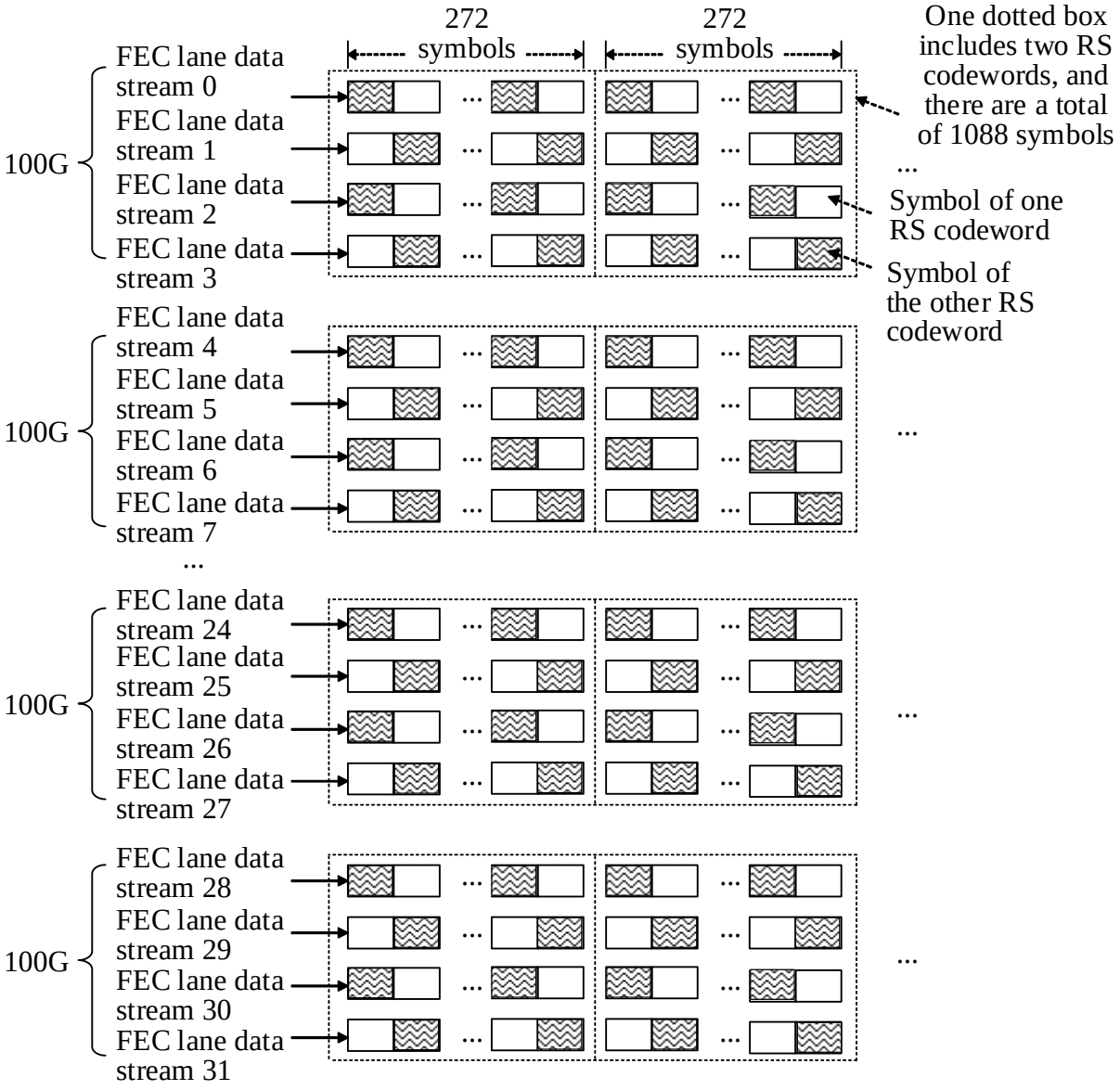

272 symbols
272 symbols
One dotted box includes two RS codewords, and there are a total of 1088 symbols
Symbol of one RS codeword
Symbol of the other RS codeword
100G
FEC lane data stream 0
FEC lane data stream 1
FEC lane data stream 2
FEC lane data stream 3
FEC lane data stream 4
FEC lane data stream 5
FEC lane data stream 6
FEC lane data stream 7
FEC lane data stream 24
FEC lane data stream 25
FEC lane data stream 26
FEC lane data stream 27
FEC lane data stream 28
FEC lane data stream 29
FEC lane data stream 30
FEC lane data stream 31

FIG. 8

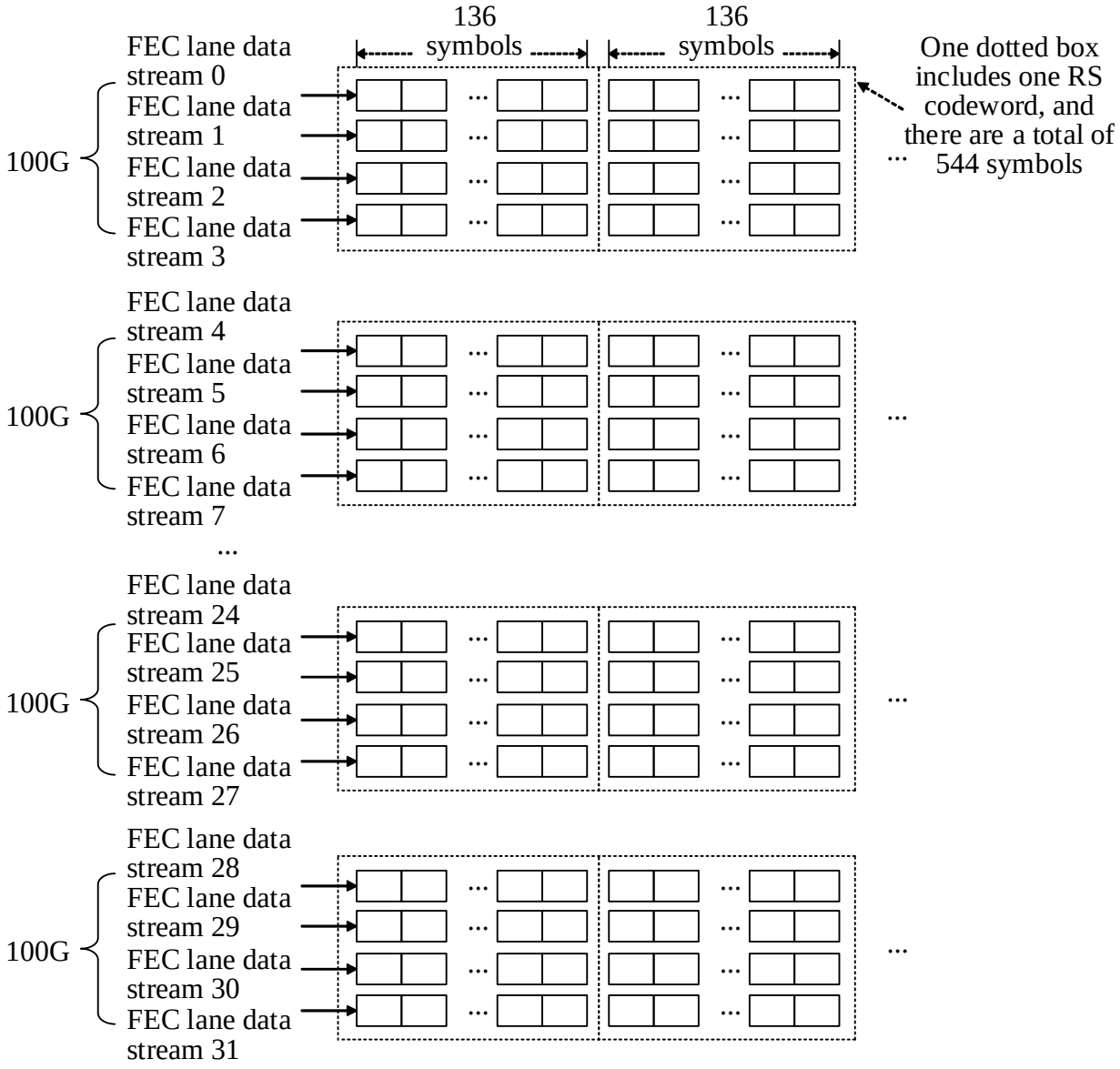

136 symbols
136 symbols
One dotted box includes one RS codeword, and there are a total of 544 symbols
100G
FEC lane data stream 0
FEC lane data stream 1
FEC lane data stream 2
FEC lane data stream 3
FEC lane data stream 4
FEC lane data stream 5
FEC lane data stream 6
FEC lane data stream 7
FEC lane data stream 24
FEC lane data stream 25
FEC lane data stream 26
FEC lane data stream 27
FEC lane data stream 28
FEC lane data stream 29
FEC lane data stream 30
FEC lane data stream 31

FIG. 9

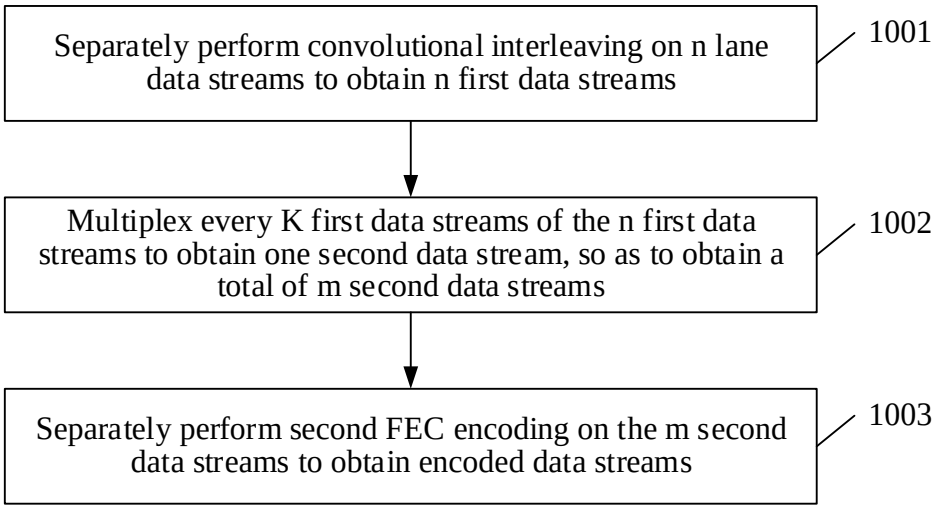

Separately perform convolutional interleaving on n lane data streams to obtain n first data streams
1001
Multiplex every K first data streams of the n first data streams to obtain one second data stream, so as to obtain a total of m second data streams
1002
Separately perform second FEC encoding on the m second data streams to obtain encoded data streams
1003

FIG. 10

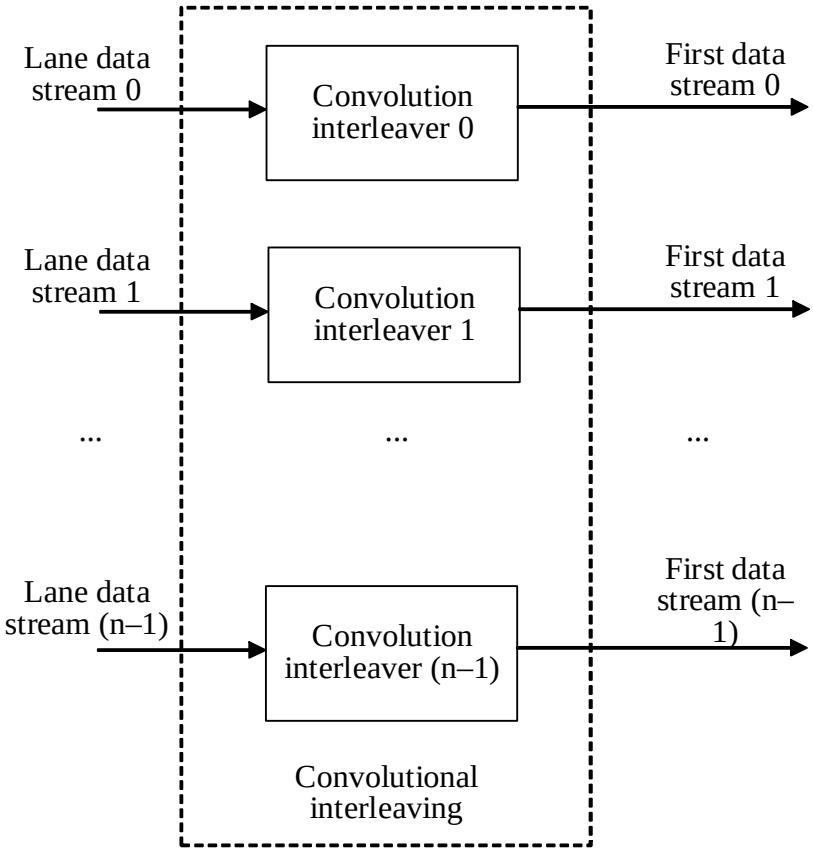

Lane data stream 0
Convolution interleaver 0
First data stream 0
Lane data stream 1
Convolution interleaver 1
First data stream 1
...
...
...
Lane data stream (n–1)
Convolution interleaver (n–1)
First data stream (n–1)
Convolutional interleaving

FIG. 11

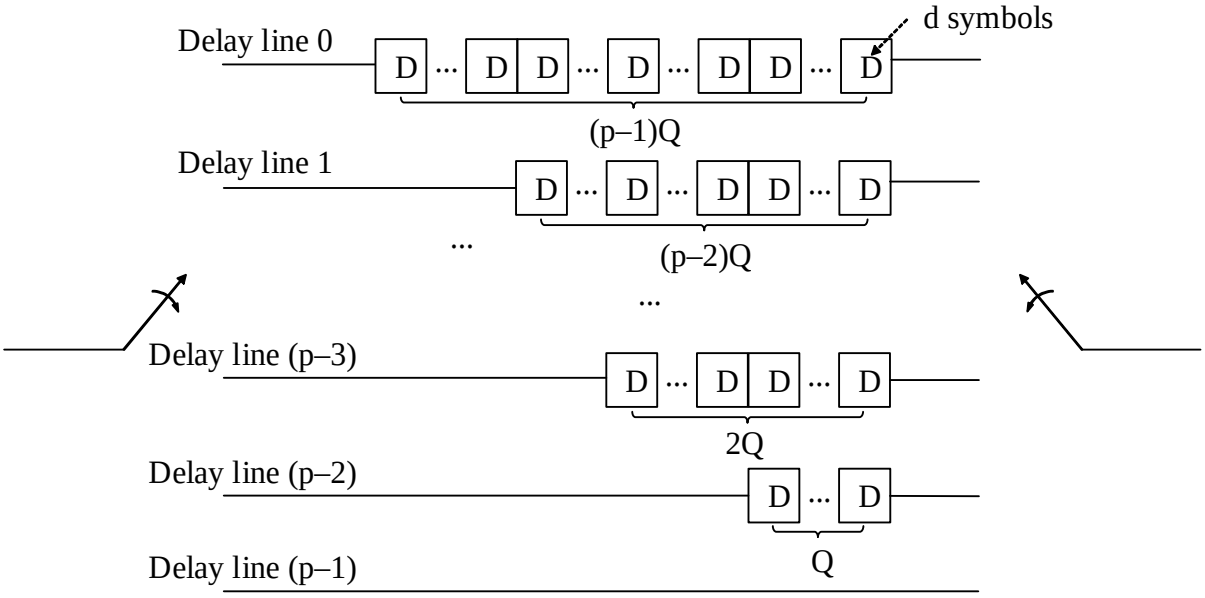


FIG. 12(a)

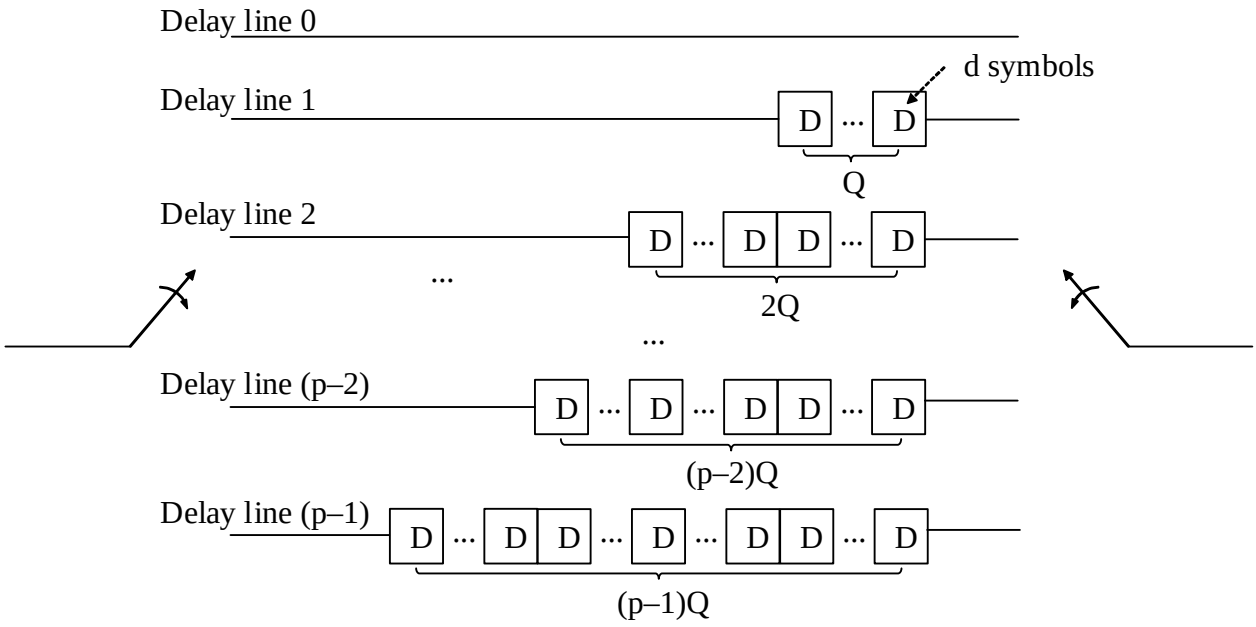


FIG. 12(b)

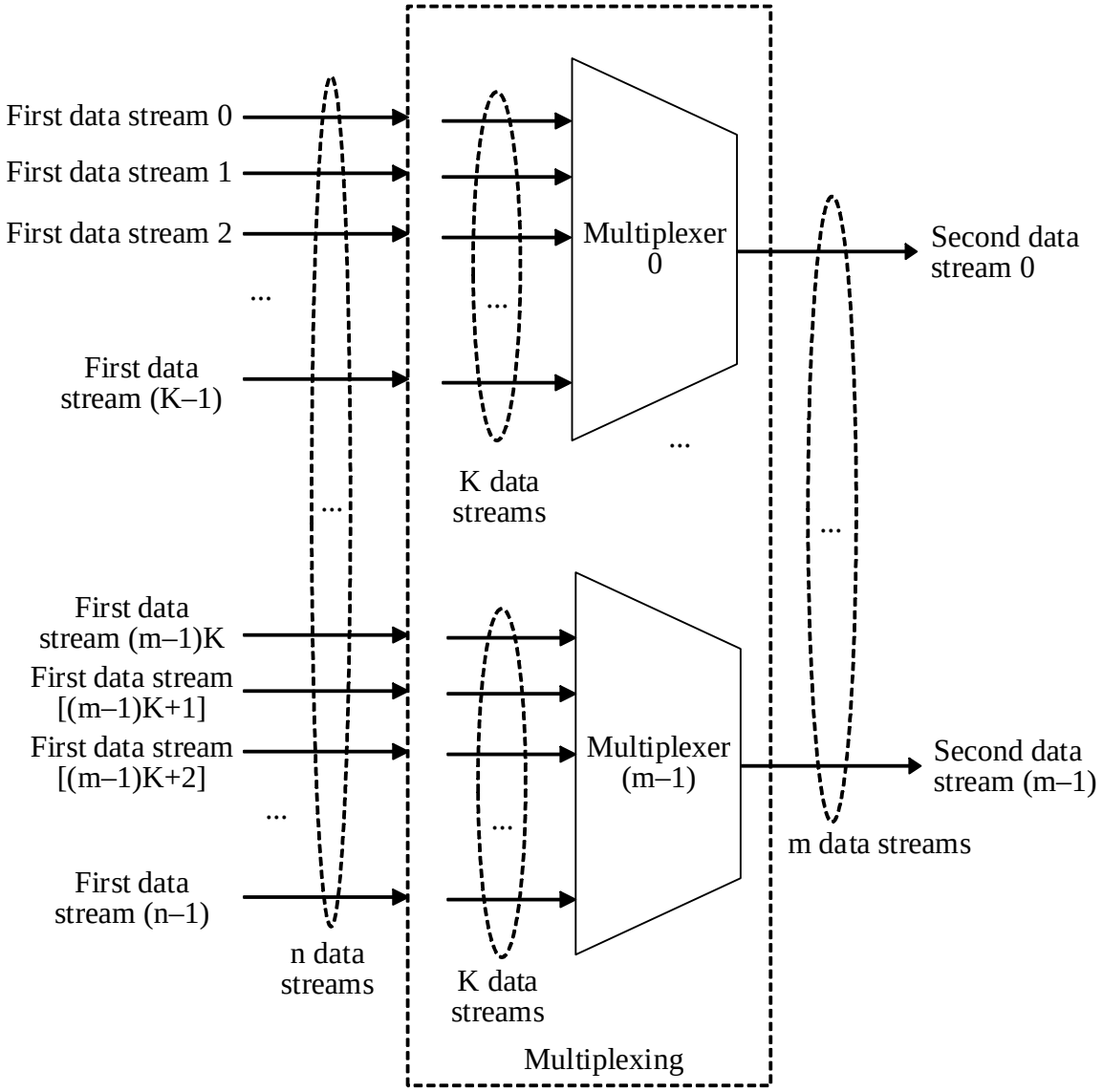

First data stream 0
First data stream 1
First data stream 2
...
First data stream (K–1)
...
n data streams
K data streams
Multiplexer 0
...
Second data stream 0
First data stream (m–1)K
First data stream [(m–1)K+1]
First data stream [(m–1)K+2]
...
First data stream (n–1)
...
K data streams
Multiplexer (m–1)
Second data stream (m–1)
...
m data streams
Multiplexing

FIG. 13

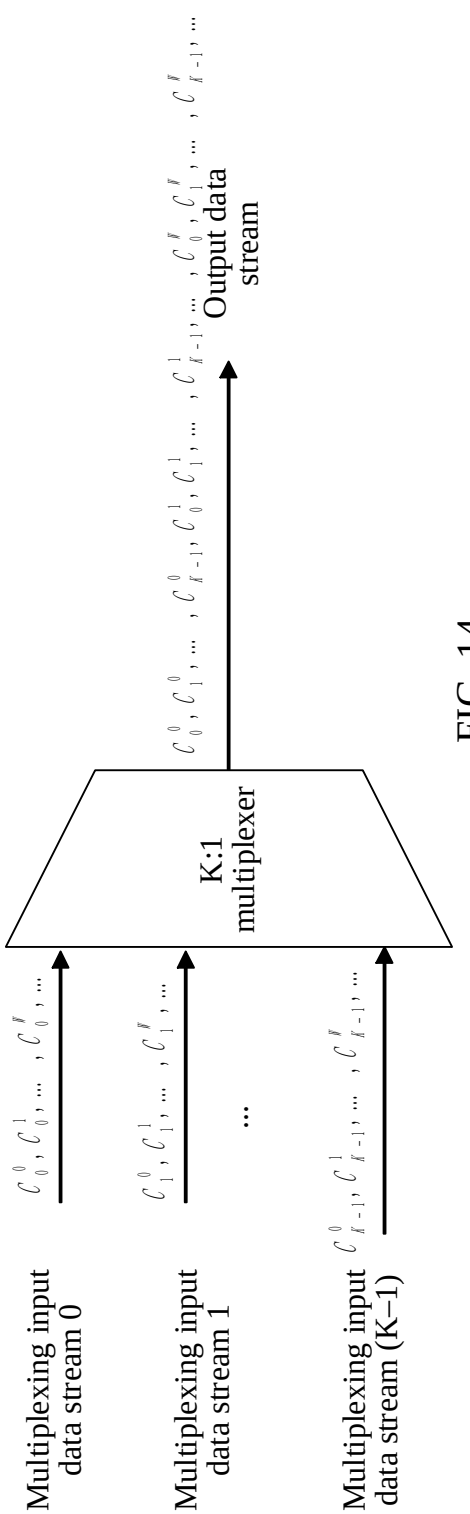

Multiplexing input data stream 0
Multiplexing input data stream 1
Multiplexing input data stream (K–1)
...
K:1 multiplexer
Output data stream

FIG. 14

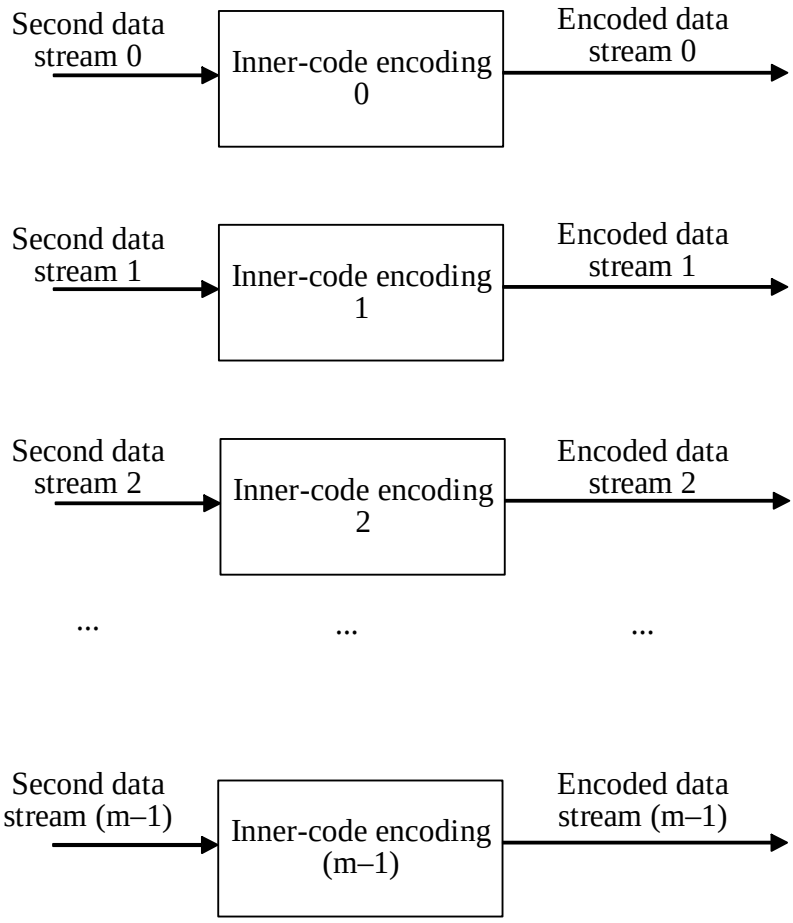


FIG. 15

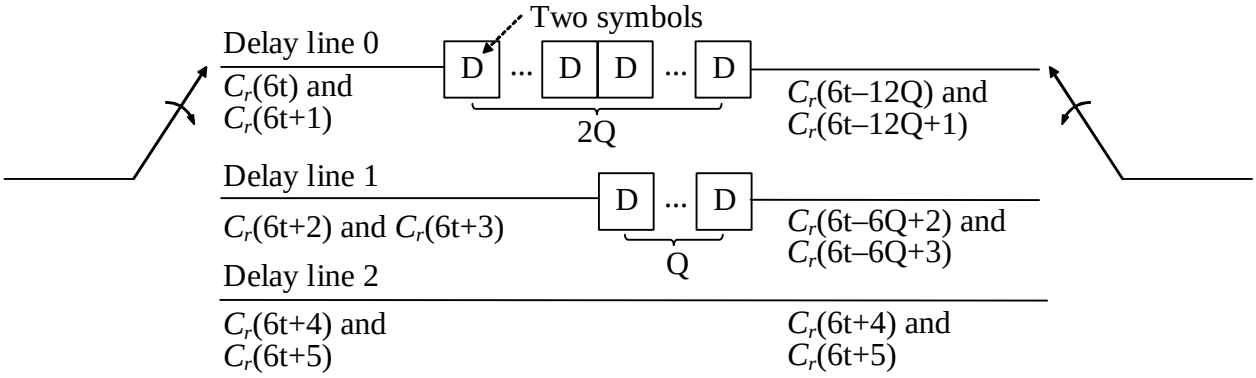


FIG. 16(a)

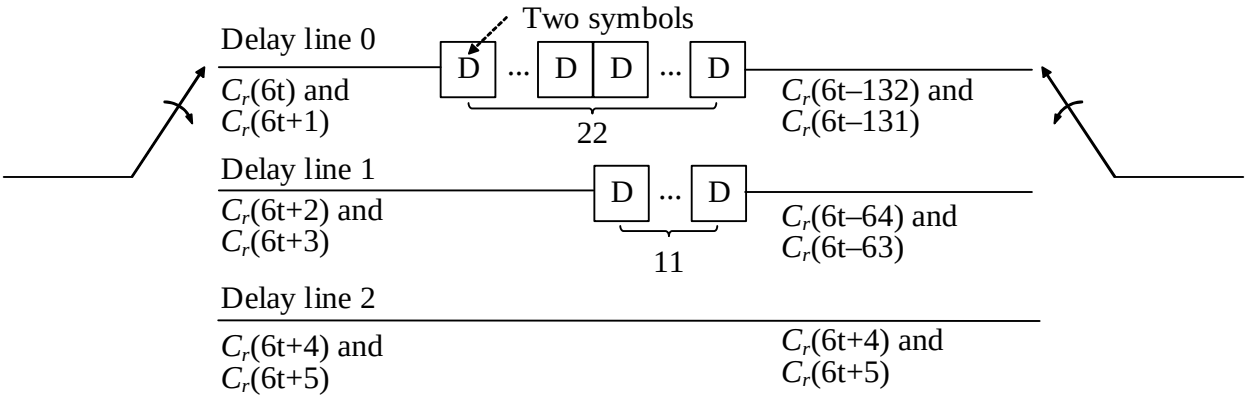


FIG. 16(b)

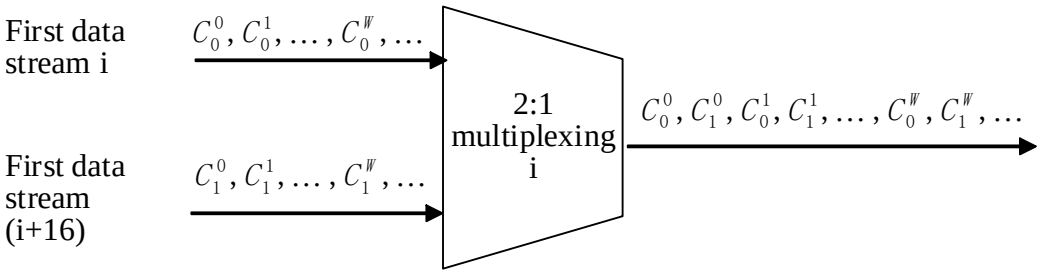


FIG. 17(a)

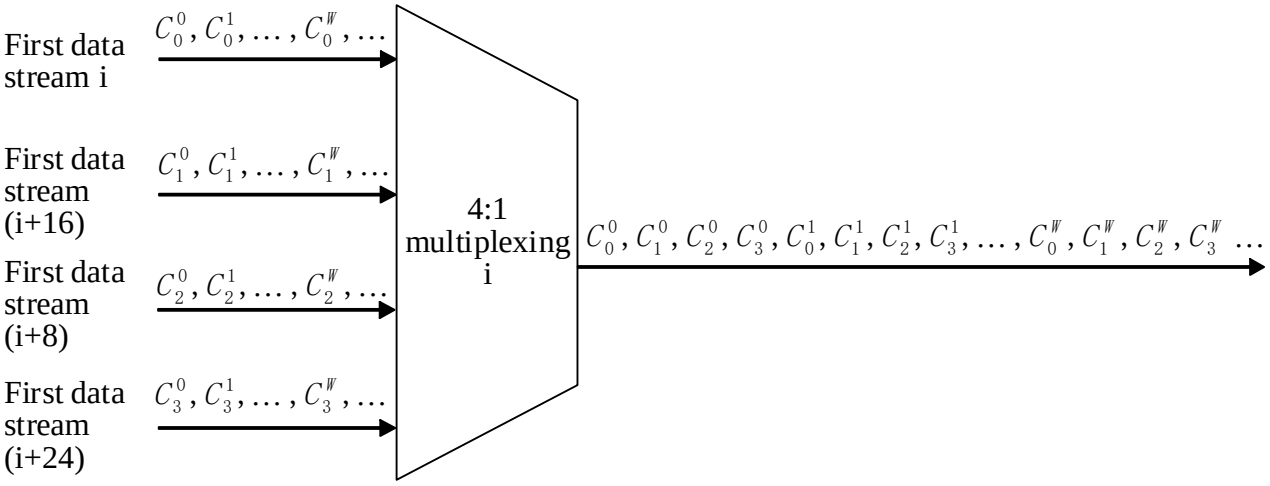


FIG. 17(b)

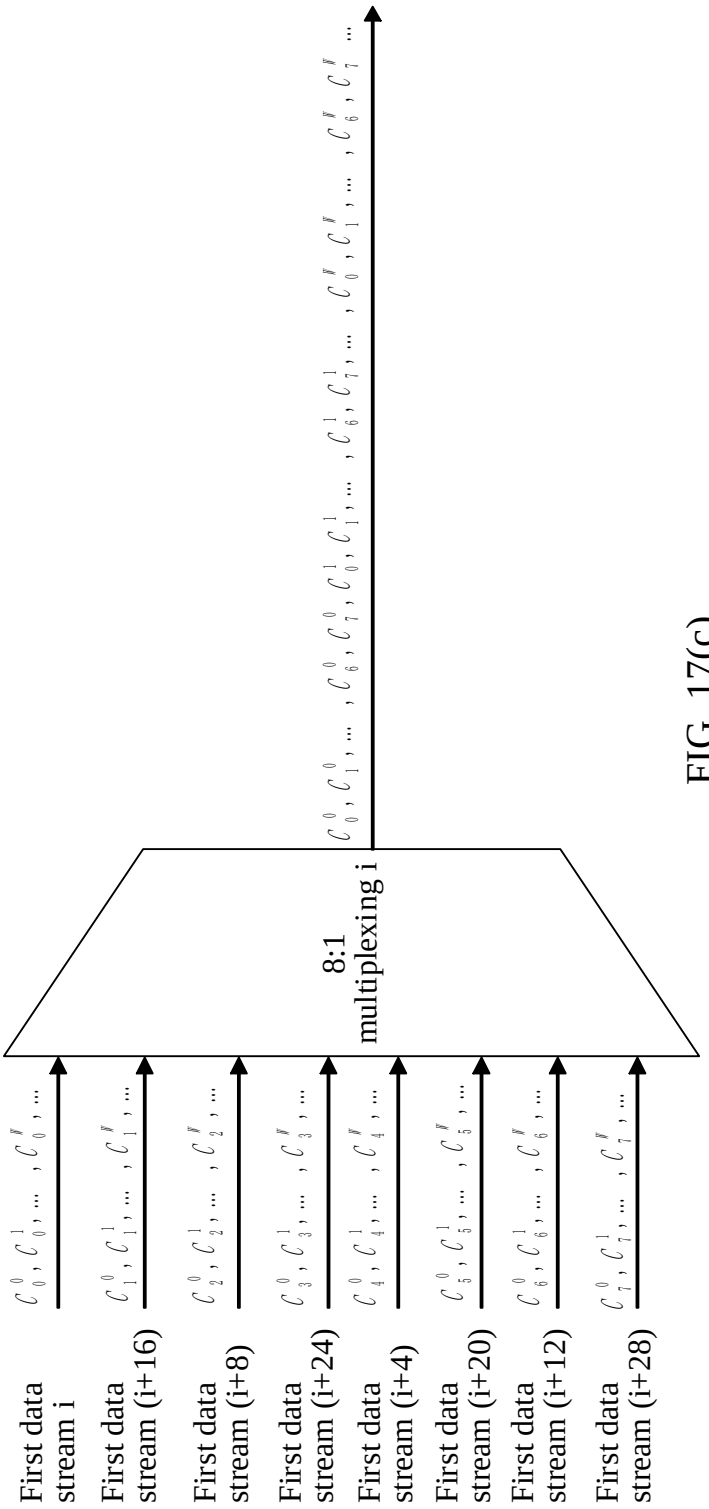

First data stream i
First data stream (i+16)
First data stream (i+8)
First data stream (i+24)
First data stream (i+4)
First data stream (i+20)
First data stream (i+12)
First data stream (i+28)
8:1 multiplexing i

FIG. 17(c)

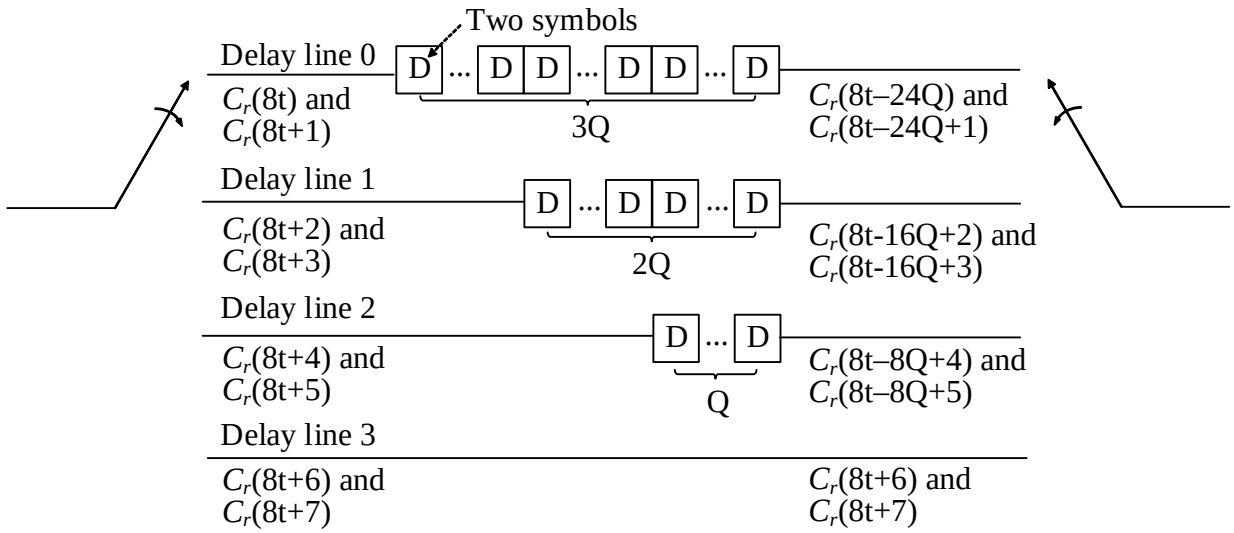


FIG. 18(a)

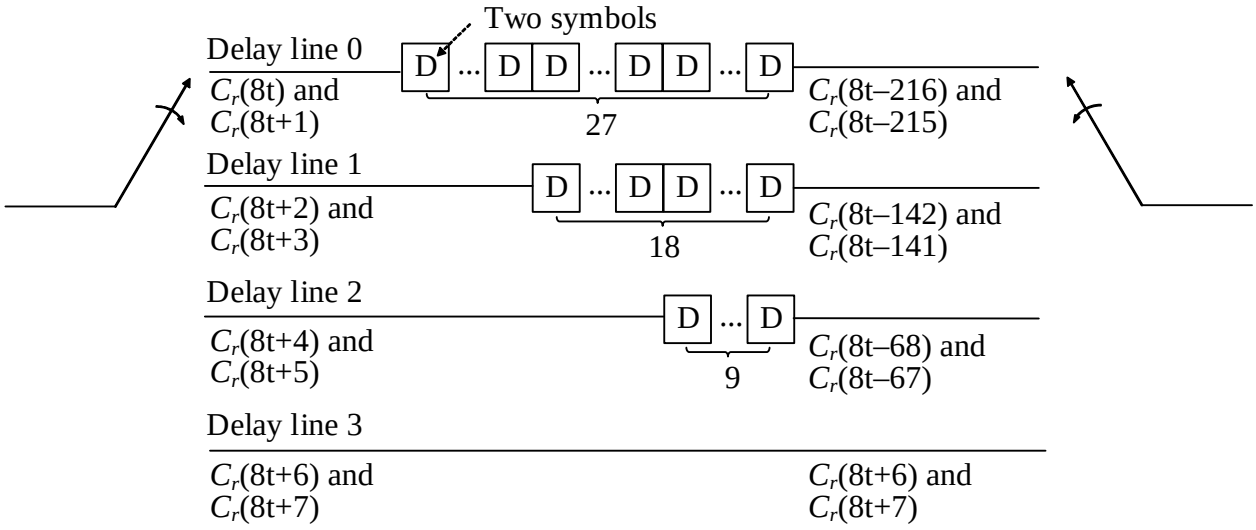


FIG. 18(b)

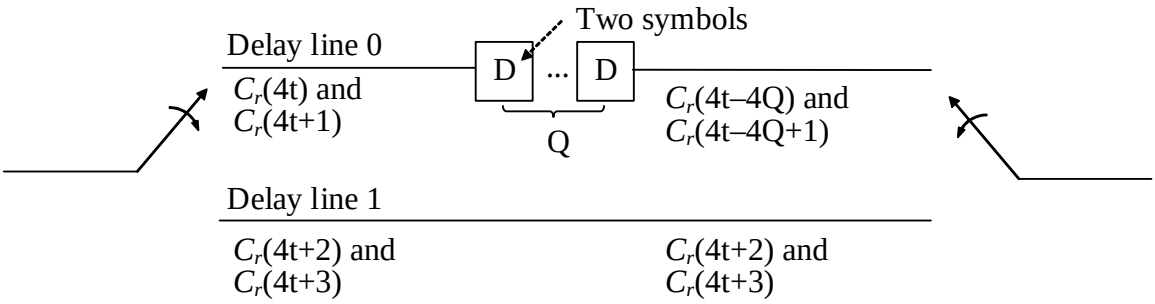


FIG. 19(a)

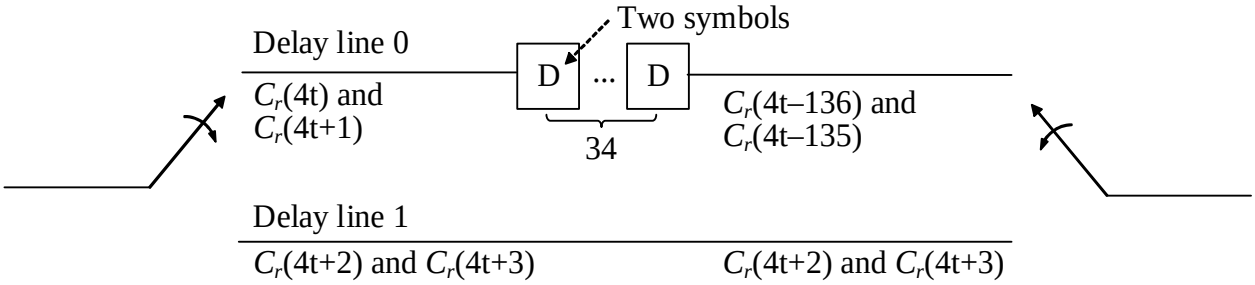


FIG. 19(b)

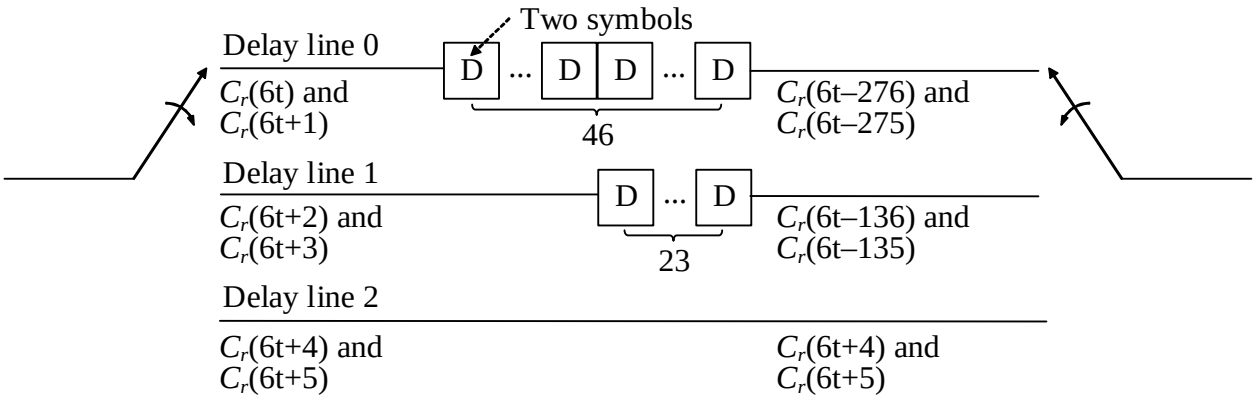


FIG. 20

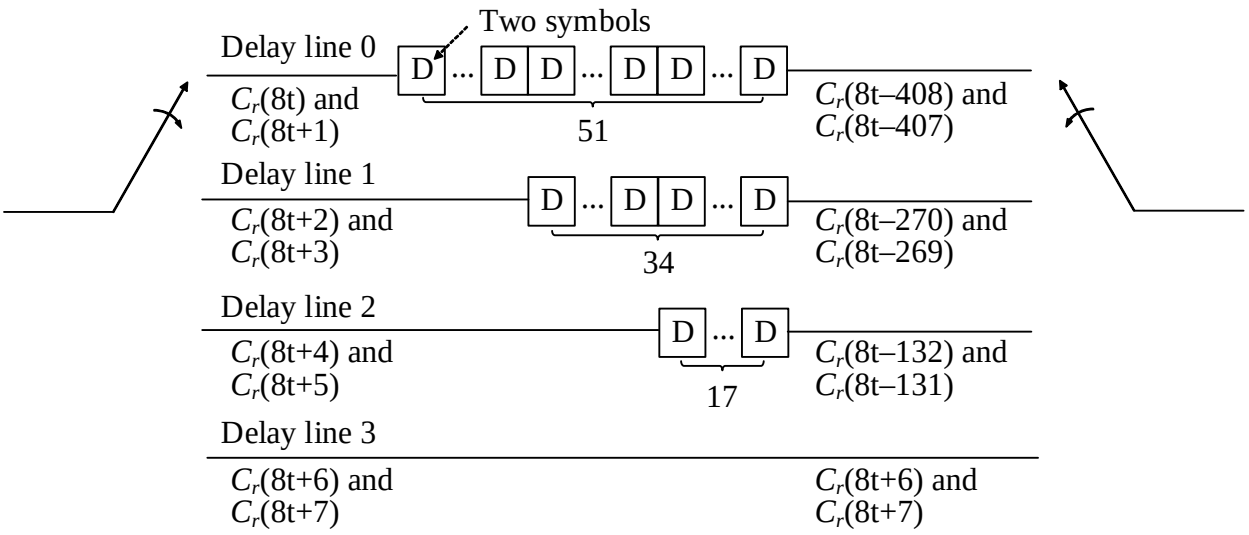

Two symbols
Delay line 0
D ... D D ... D D ... D
51
C_r(8t) and
C_r(8t+1)
C_r(8t–408) and
C_r(8t–407)
Delay line 1
D ... D D ... D
34
C_r(8t+2) and
C_r(8t+3)
C_r(8t–270) and
C_r(8t–269)
Delay line 2
D ... D
17
C_r(8t+4) and
C_r(8t+5)
C_r(8t–132) and
C_r(8t–131)
Delay line 3
C_r(8t+6) and
C_r(8t+7)
C_r(8t+6) and
C_r(8t+7)

FIG. 21

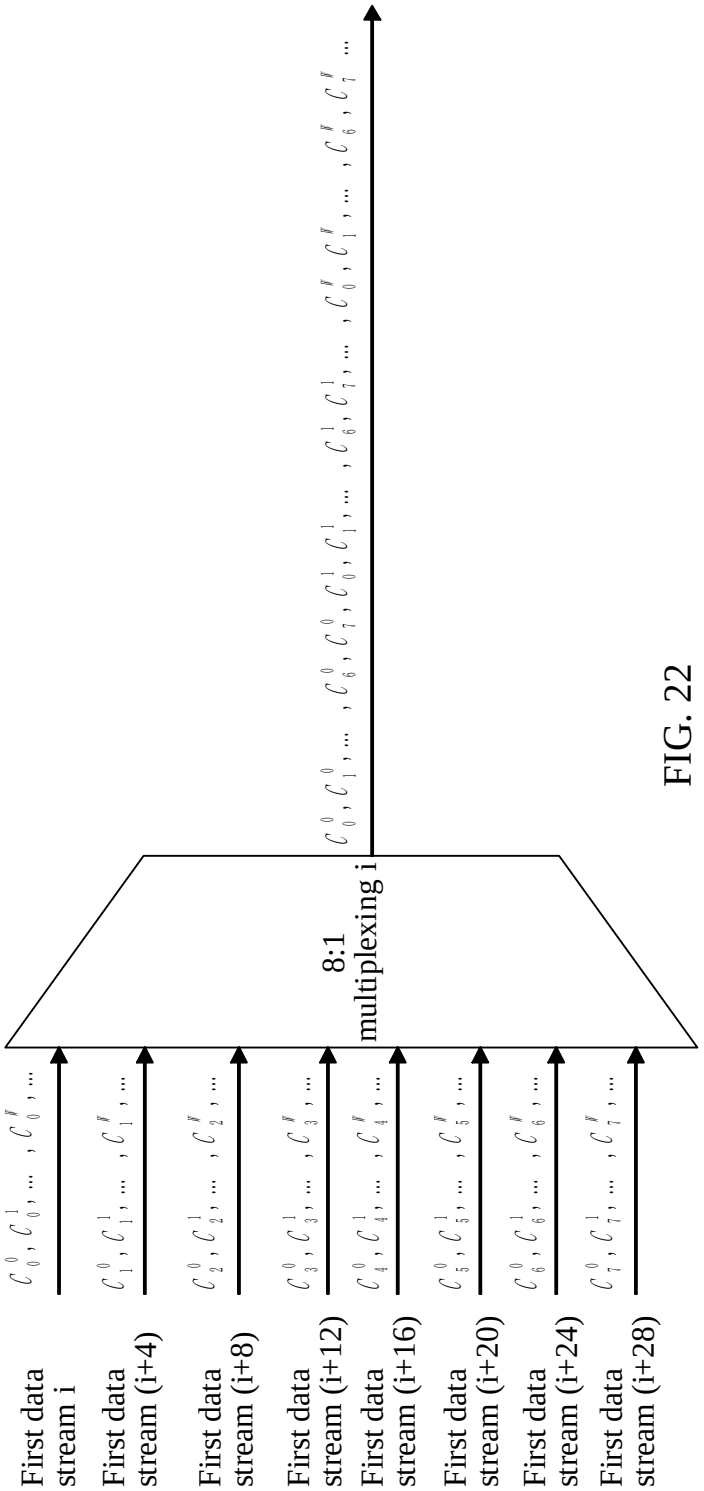

First data stream i
First data stream (i+4)
First data stream (i+8)
First data stream (i+12)
First data stream (i+16)
First data stream (i+20)
First data stream (i+24)
First data stream (i+28)
8:1 multiplexing i

FIG. 22

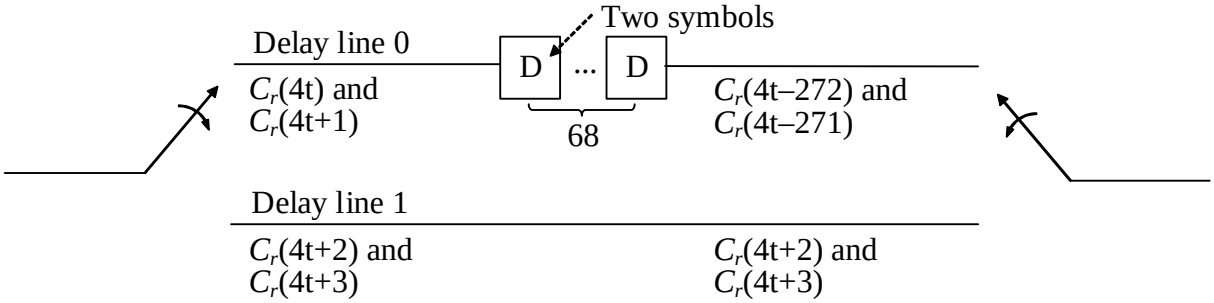


FIG. 23

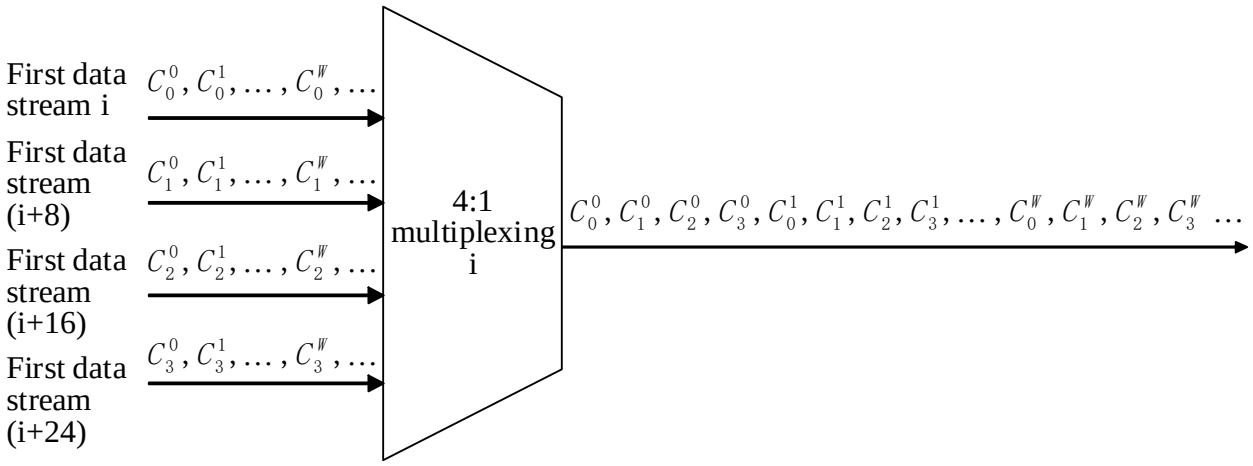


FIG. 24

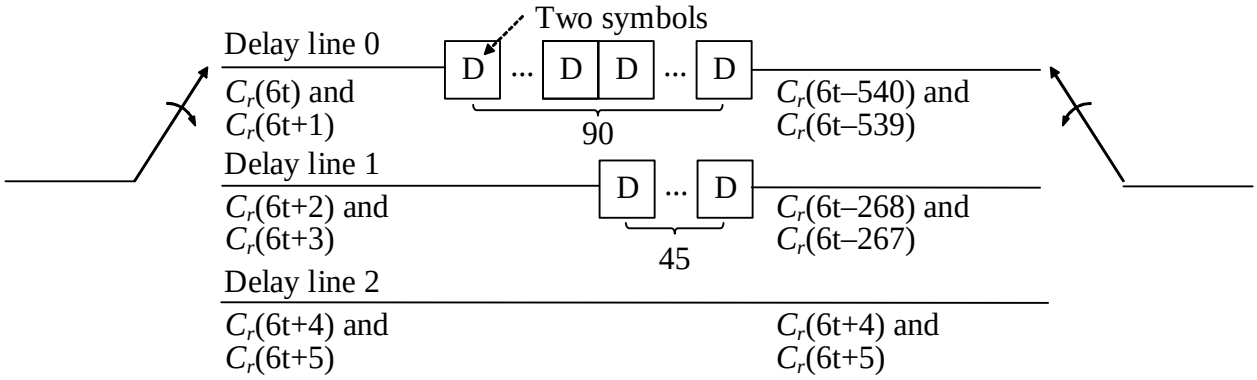


FIG. 25

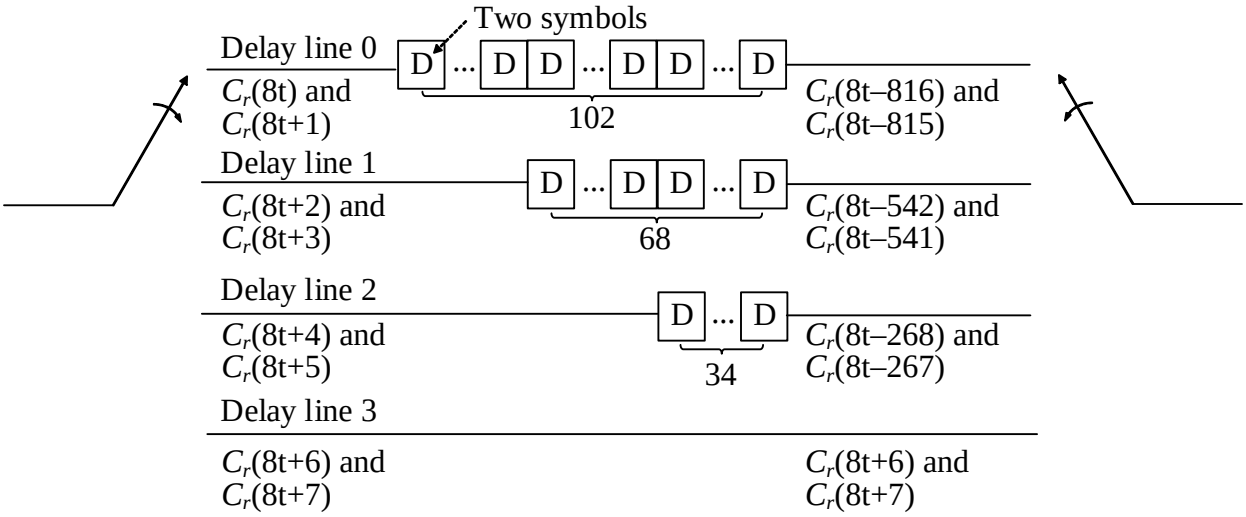


FIG. 26

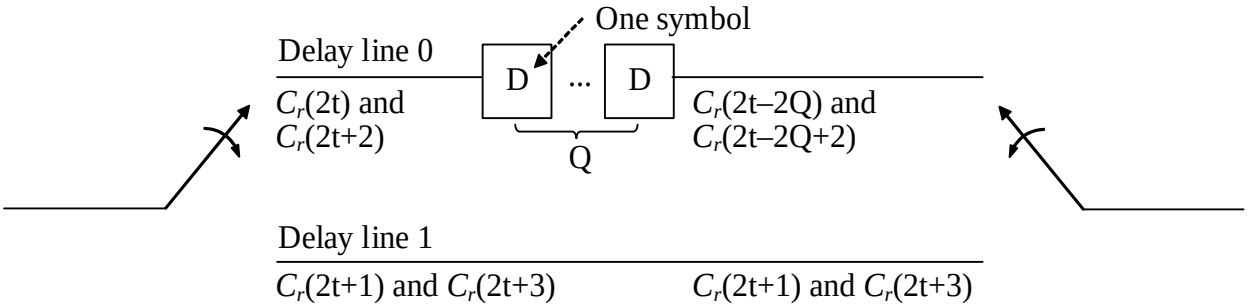


FIG. 27(a)

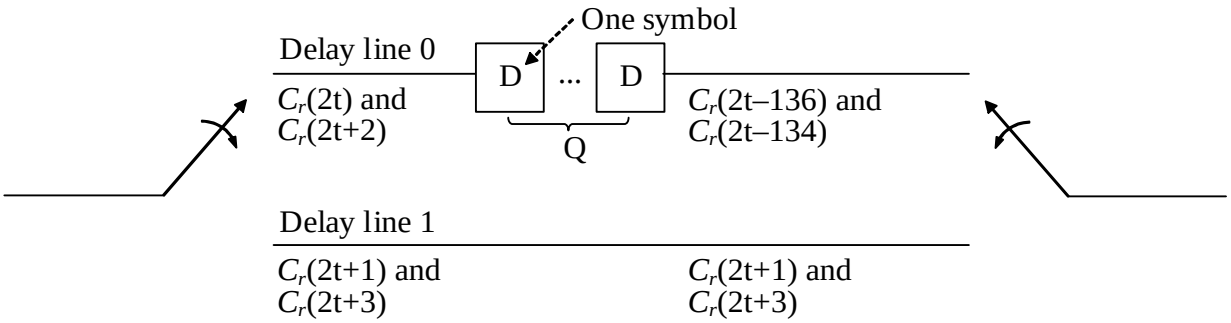


FIG. 27(b)

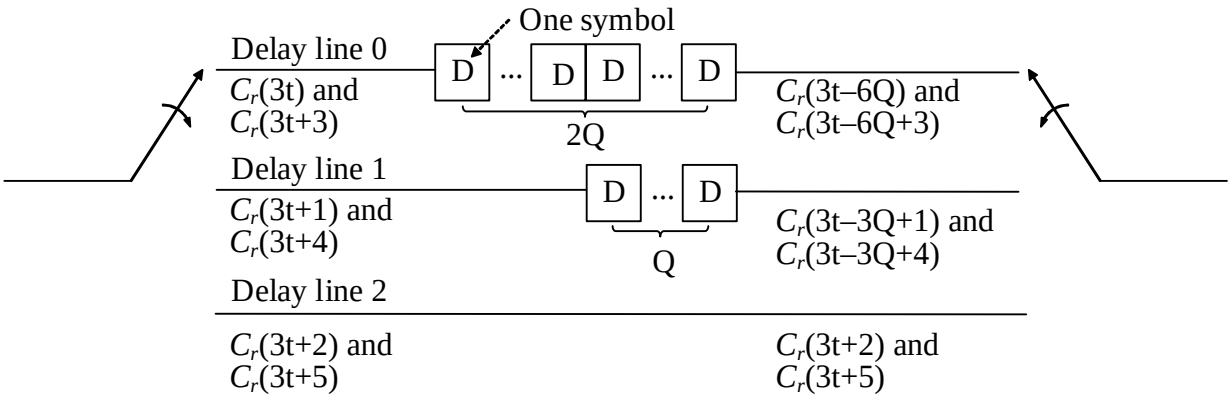


FIG. 28(a)

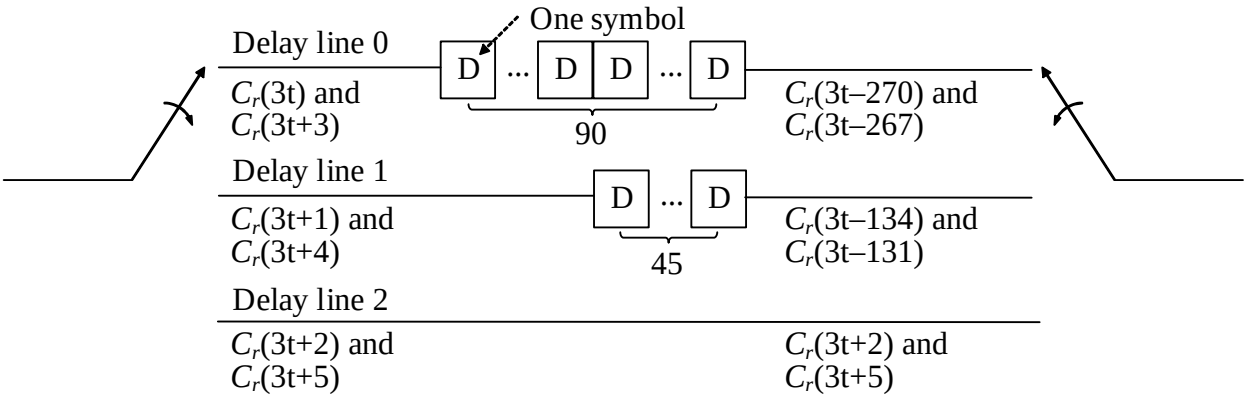


FIG. 28(b)

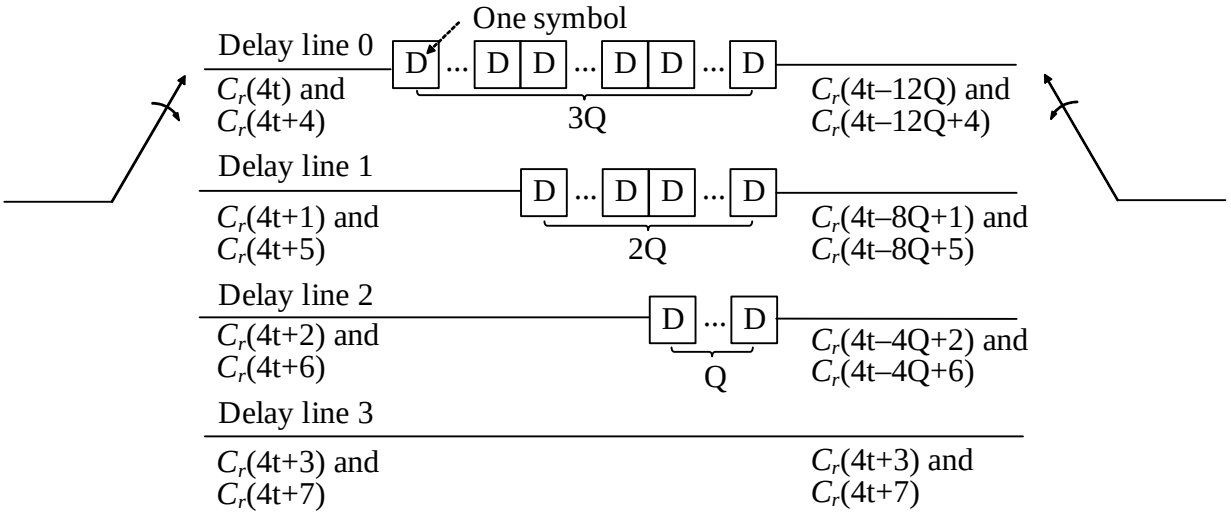


FIG. 29(a)

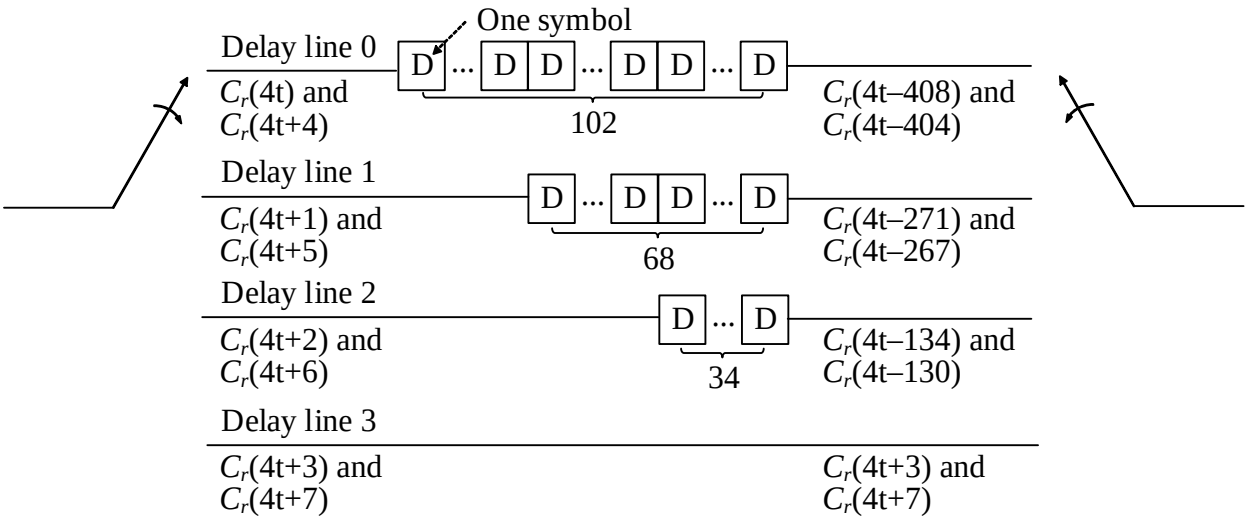


FIG. 29(b)

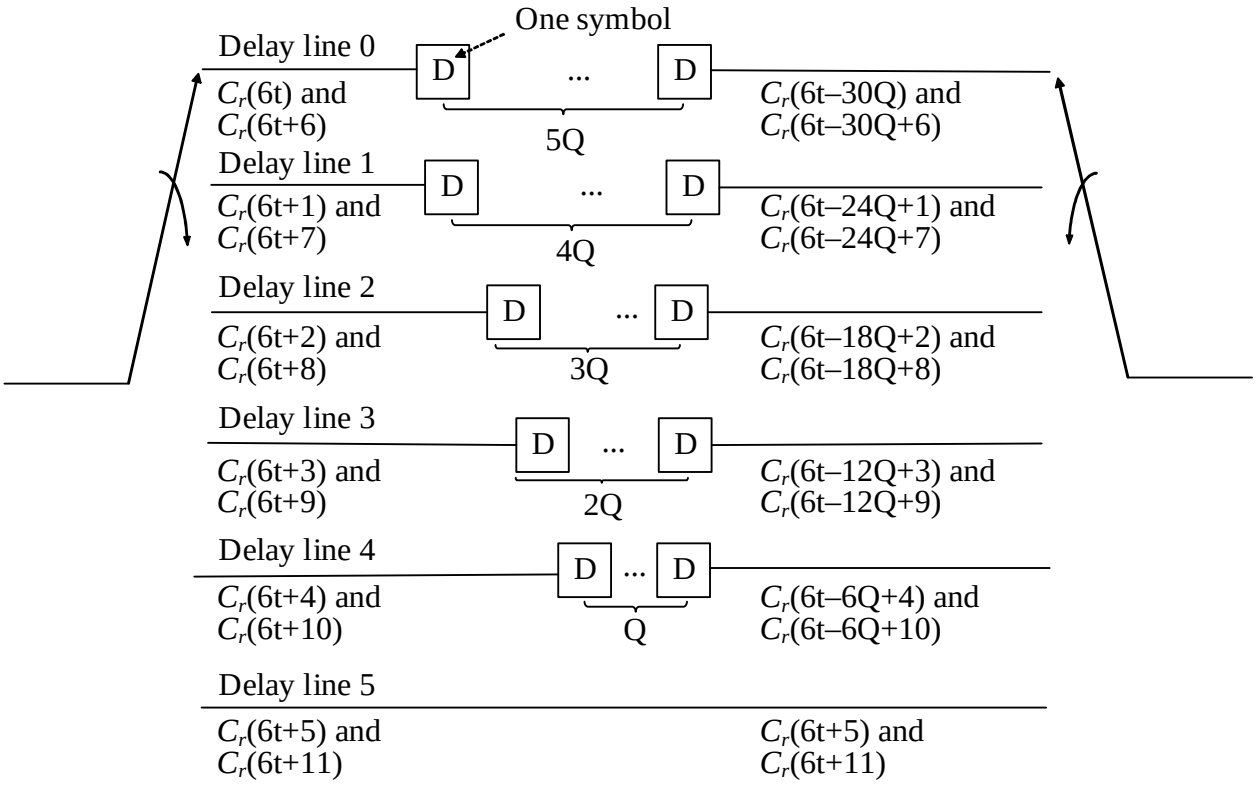


FIG. 30(a)

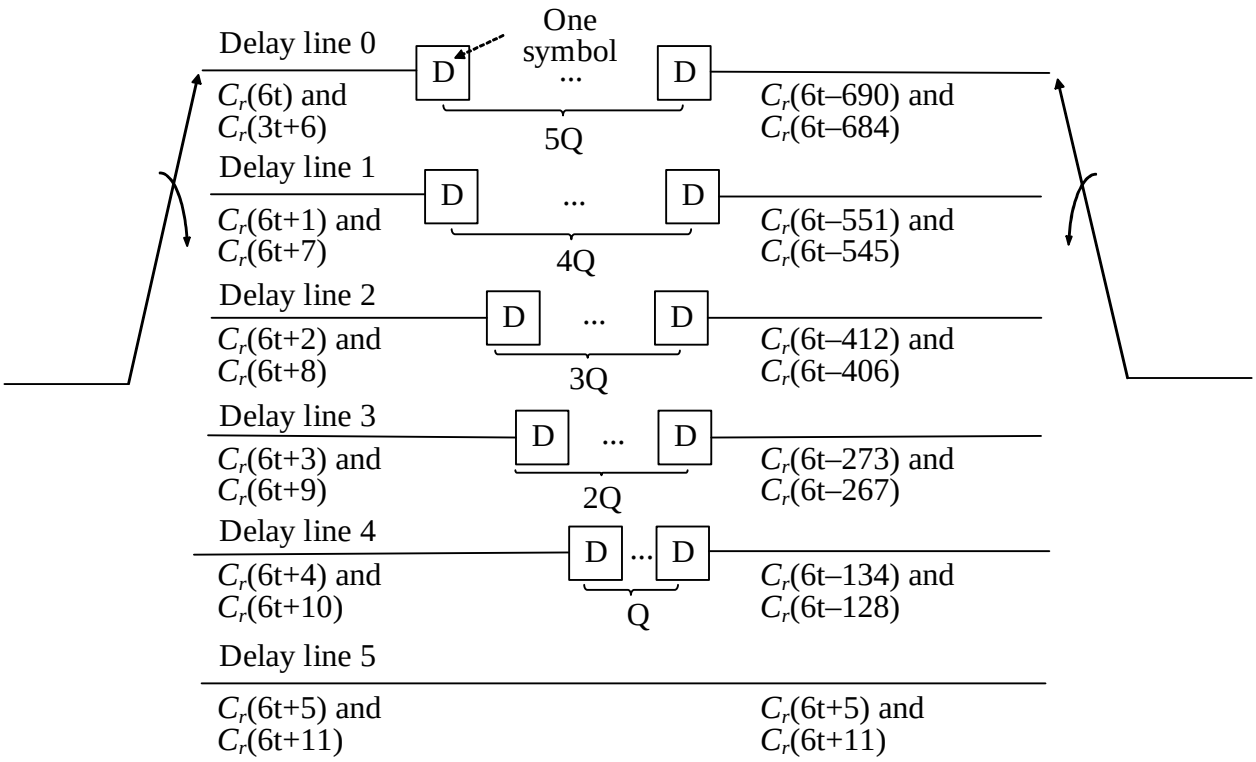

Delay line 0
One symbol
D
...
D
C_r(6t) and C_r(3t+6)
5Q
C_r(6t–690) and C_r(6t–684)
Delay line 1
D
...
D
C_r(6t+1) and C_r(6t+7)
4Q
C_r(6t–551) and C_r(6t–545)
Delay line 2
D
...
D
C_r(6t+2) and C_r(6t+8)
3Q
C_r(6t–412) and C_r(6t–406)
Delay line 3
D
...
D
C_r(6t+3) and C_r(6t+9)
2Q
C_r(6t–273) and C_r(6t–267)
Delay line 4
D
...
D
C_r(6t+4) and C_r(6t+10)
Q
C_r(6t–134) and C_r(6t–128)
Delay line 5
C_r(6t+5) and C_r(6t+11)
C_r(6t+5) and C_r(6t+11)

FIG. 30(b)

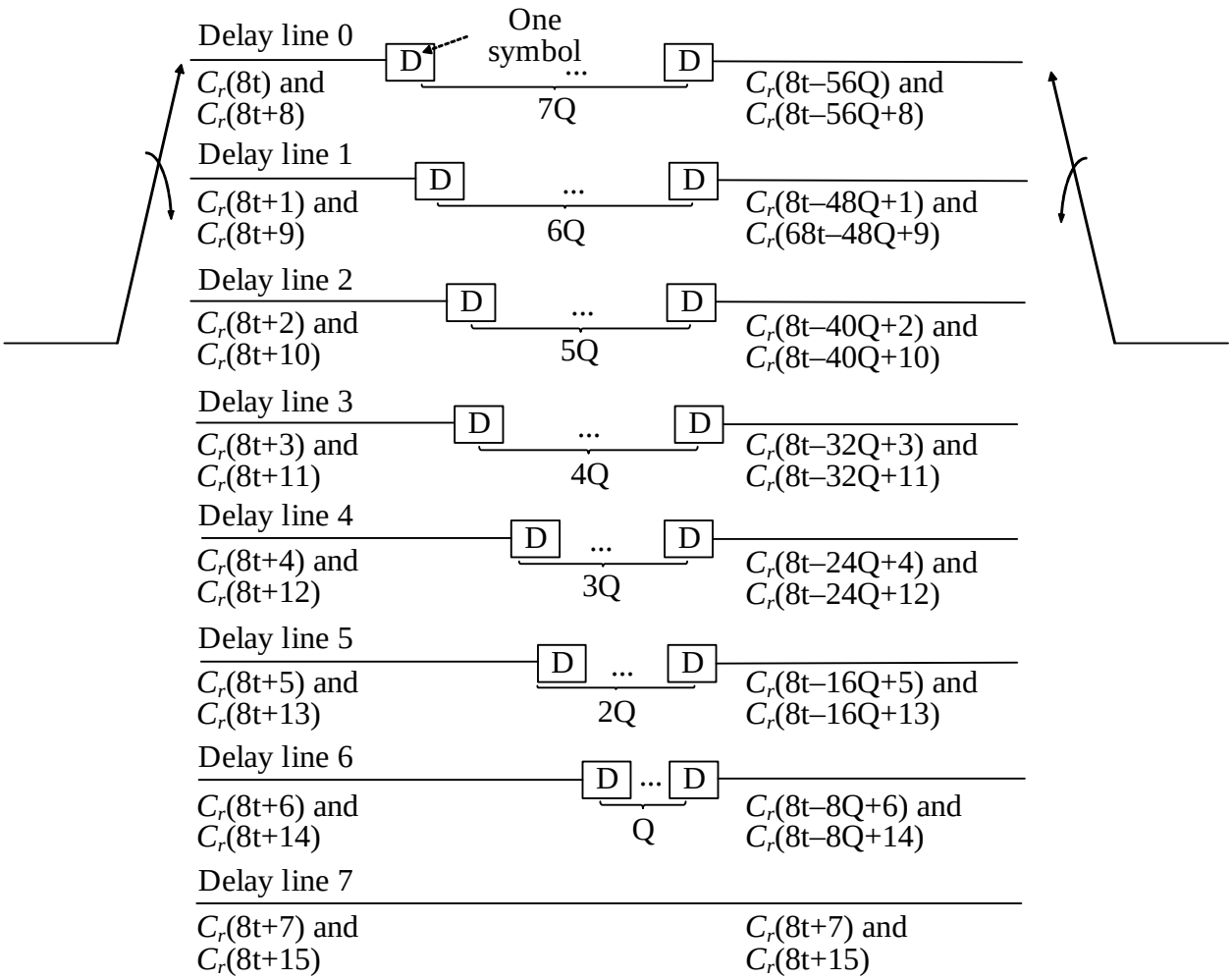

Delay line 0
One symbol
D
...
D
7Q
C_r(8t) and C_r(8t+8)
C_r(8t–56Q) and C_r(8t–56Q+8)
Delay line 1
6Q
C_r(8t+1) and C_r(8t+9)
C_r(8t–48Q+1) and C_r(68t–48Q+9)
Delay line 2
5Q
C_r(8t+2) and C_r(8t+10)
C_r(8t–40Q+2) and C_r(8t–40Q+10)
Delay line 3
4Q
C_r(8t+3) and C_r(8t+11)
C_r(8t–32Q+3) and C_r(8t–32Q+11)
Delay line 4
3Q
C_r(8t+4) and C_r(8t+12)
C_r(8t–24Q+4) and C_r(8t–24Q+12)
Delay line 5
2Q
C_r(8t+5) and C_r(8t+13)
C_r(8t–16Q+5) and C_r(8t–16Q+13)
Delay line 6
Q
C_r(8t+6) and C_r(8t+14)
C_r(8t–8Q+6) and C_r(8t–8Q+14)
Delay line 7
C_r(8t+7) and C_r(8t+15)
C_r(8t+7) and C_r(8t+15)

FIG. 31(a)

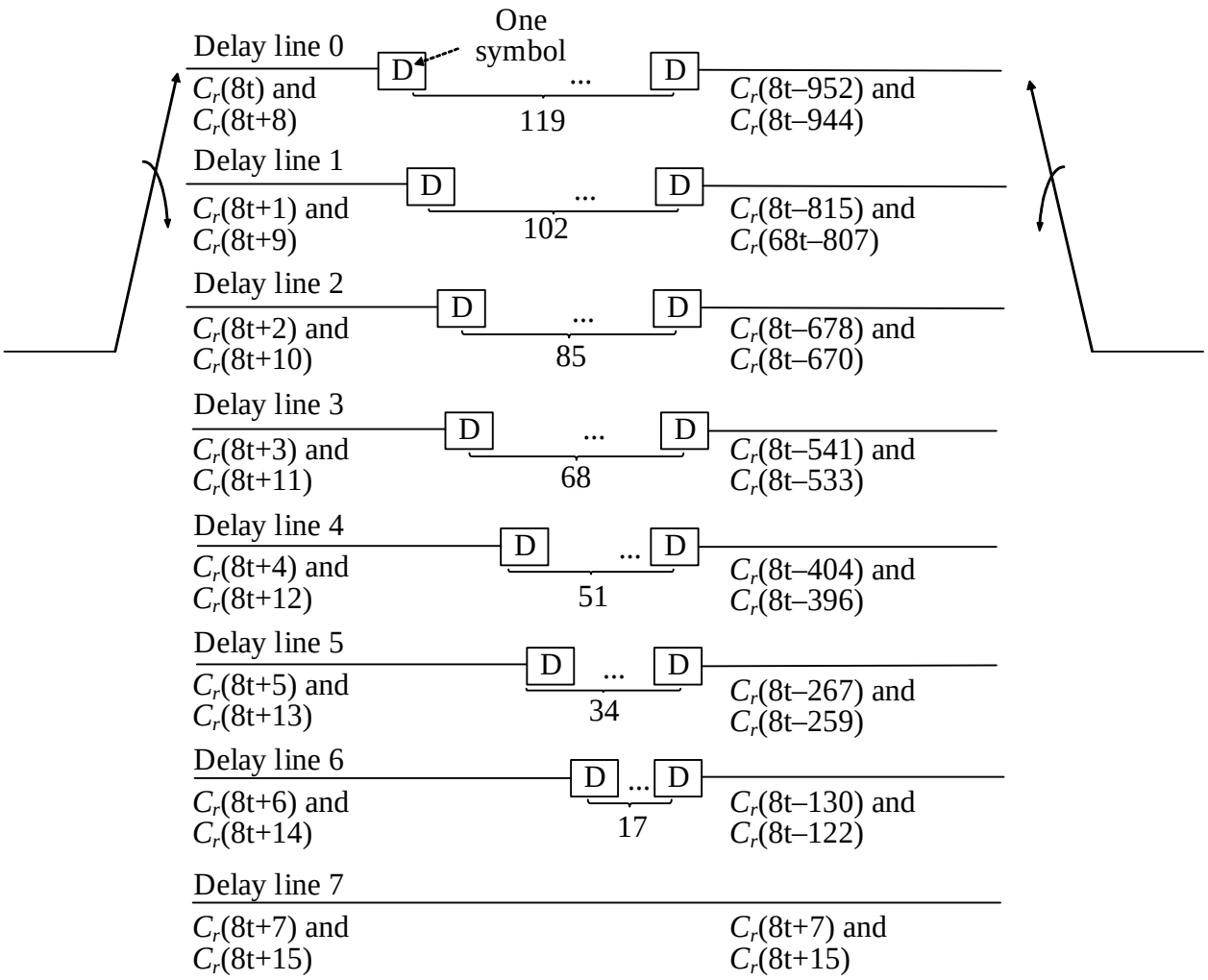

Delay line 0
One symbol
D
...
D
119
C_r(8t) and C_r(8t+8)
C_r(8t–952) and C_r(8t–944)
Delay line 1
D
...
D
102
C_r(8t+1) and C_r(8t+9)
C_r(8t–815) and C_r(68t–807)
Delay line 2
D
...
D
85
C_r(8t+2) and C_r(8t+10)
C_r(8t–678) and C_r(8t–670)
Delay line 3
D
...
D
68
C_r(8t+3) and C_r(8t+11)
C_r(8t–541) and C_r(8t–533)
Delay line 4
D
...
D
51
C_r(8t+4) and C_r(8t+12)
C_r(8t–404) and C_r(8t–396)
Delay line 5
D
...
D
34
C_r(8t+5) and C_r(8t+13)
C_r(8t–267) and C_r(8t–259)
Delay line 6
D
...
D
17
C_r(8t+6) and C_r(8t+14)
C_r(8t–130) and C_r(8t–122)
Delay line 7
C_r(8t+7) and C_r(8t+15)
C_r(8t+7) and C_r(8t+15)

FIG. 31(b)

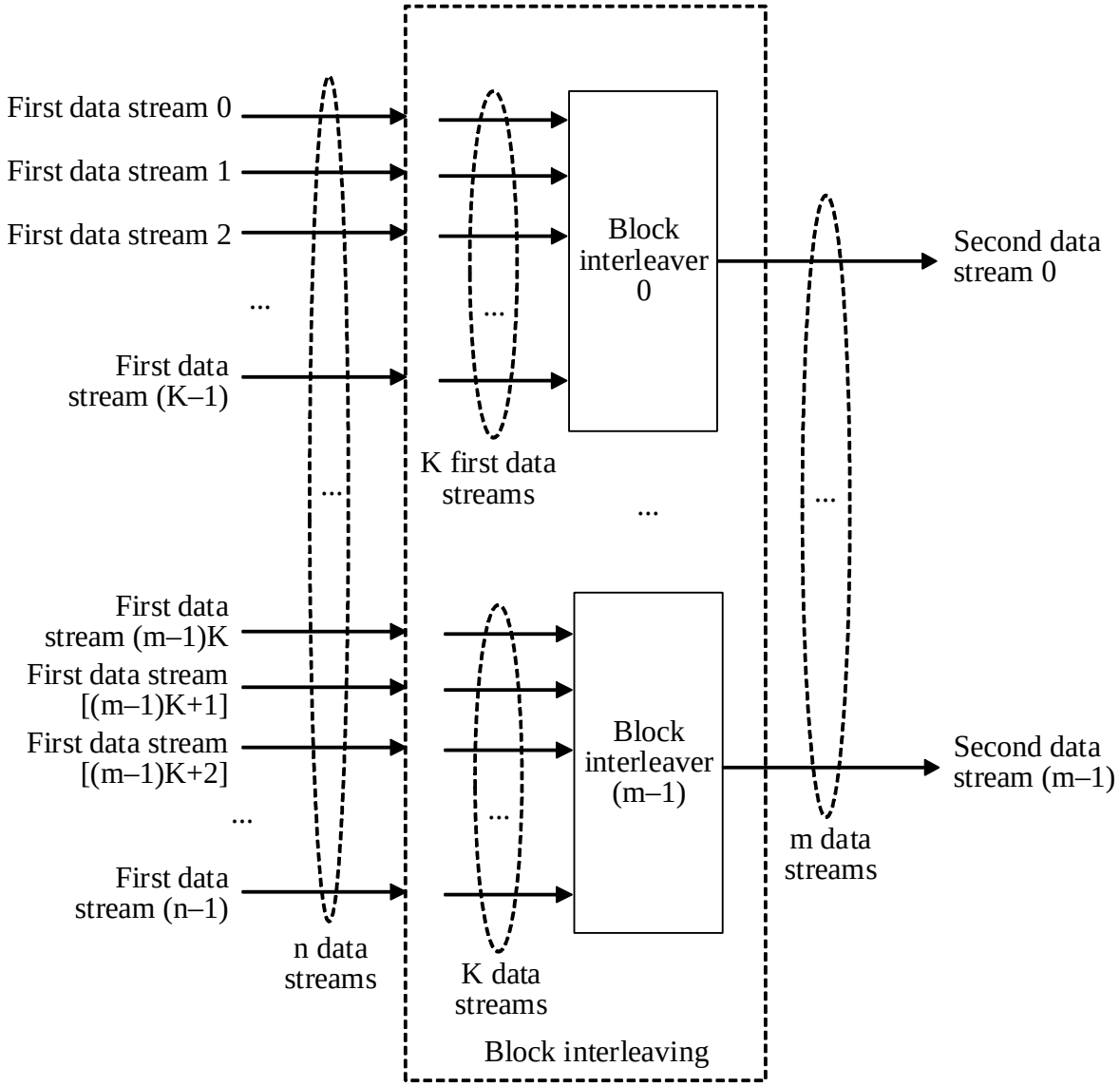

First data stream 0
First data stream 1
First data stream 2
...
First data stream (K–1)
...
n data streams
K first data streams
...
Block interleaver 0
Second data stream 0
...
First data stream (m–1)K
First data stream [(m–1)K+1]
First data stream [(m–1)K+2]
...
First data stream (n–1)
...
K data streams
Block interleaver (m–1)
Second data stream (m–1)
...
m data streams
Block interleaving

FIG. 32(a)

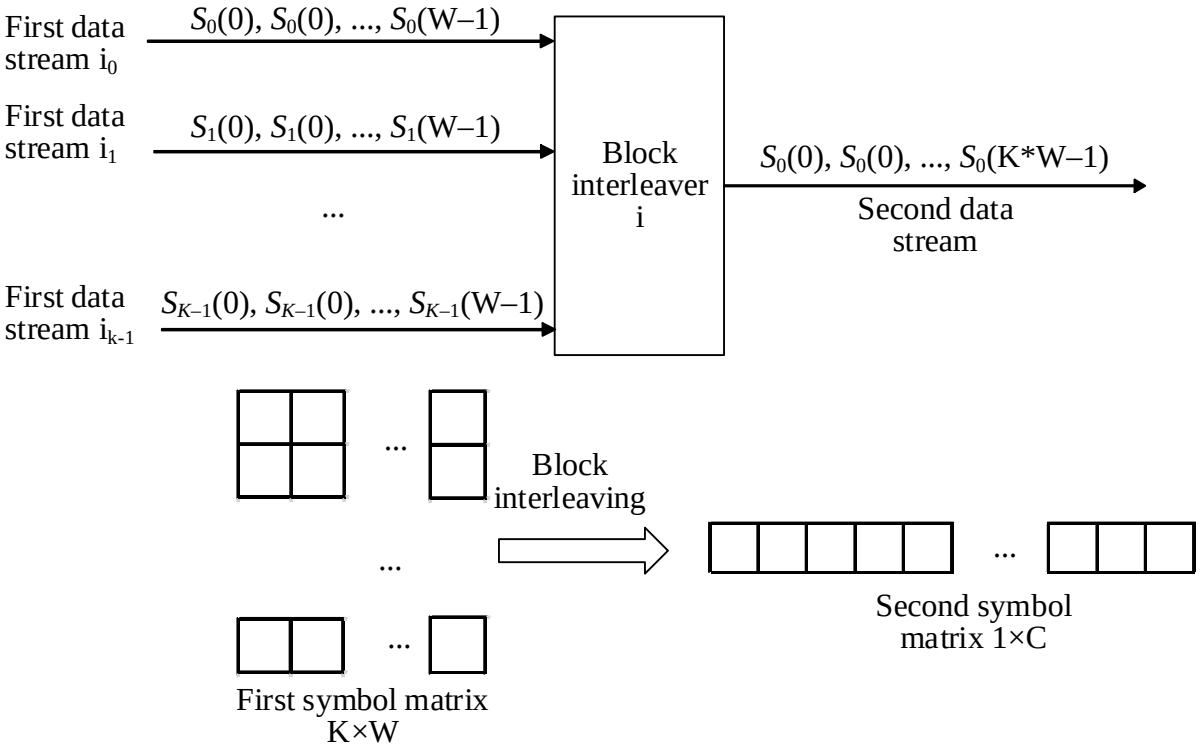


FIG. 32(b)

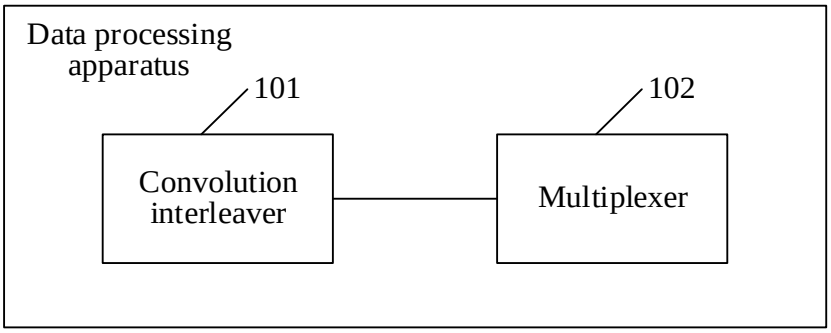


FIG. 33

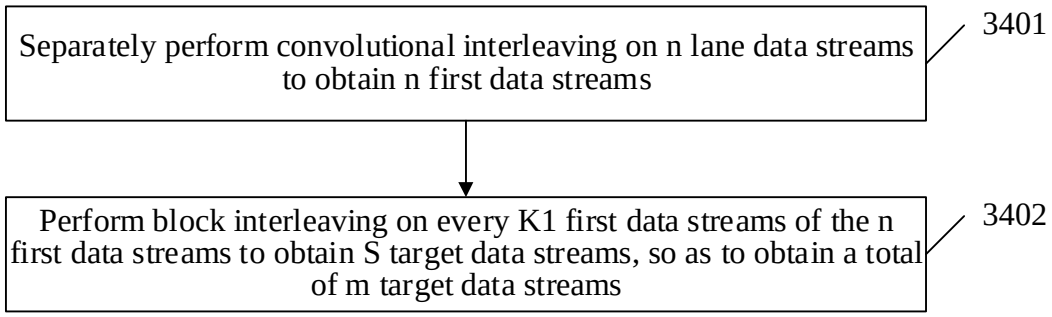


FIG. 34

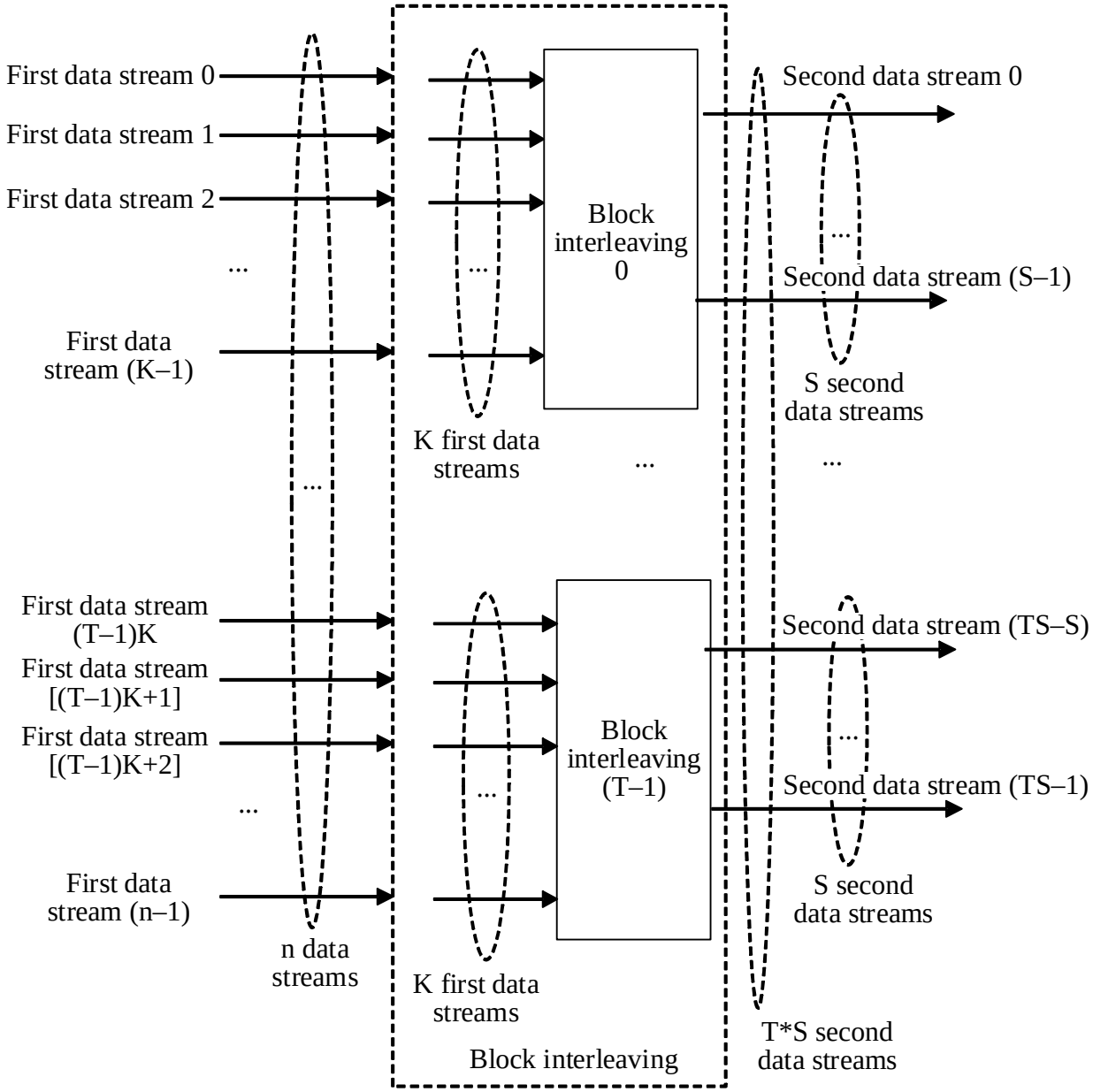

First data stream 0
First data stream 1
First data stream 2
...
First data stream (K–1)
...
First data stream (T–1)K
First data stream [(T–1)K+1]
First data stream [(T–1)K+2]
...
First data stream (n–1)
n data streams
K first data streams
Block interleaving 0
...
K first data streams
Block interleaving (T–1)
Block interleaving
Second data stream 0
...
Second data stream (S–1)
S second data streams
...
Second data stream (TS–S)
...
Second data stream (TS–1)
S second data streams
T*S second data streams

FIG. 35

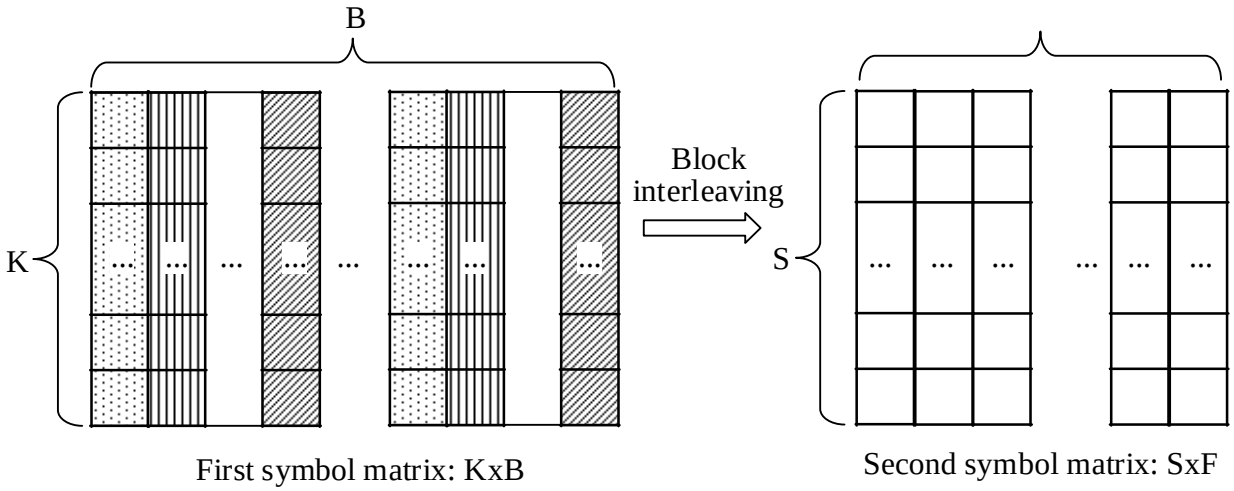

B
K
Block
interleaving
S
First symbol matrix: KxB
Second symbol matrix: SxF

FIG. 36

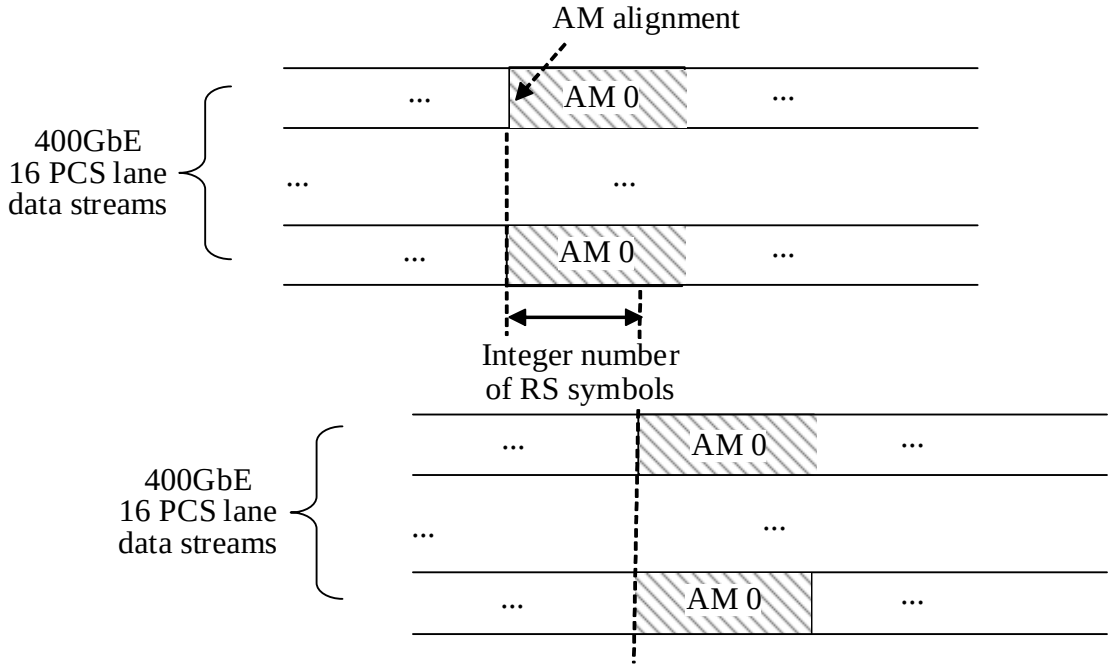

AM alignment
AM 0
400GbE
16 PCS lane
data streams
Integer number
of RS symbols
AM 0
400GbE
16 PCS lane
data streams
AM 0

FIG. 37

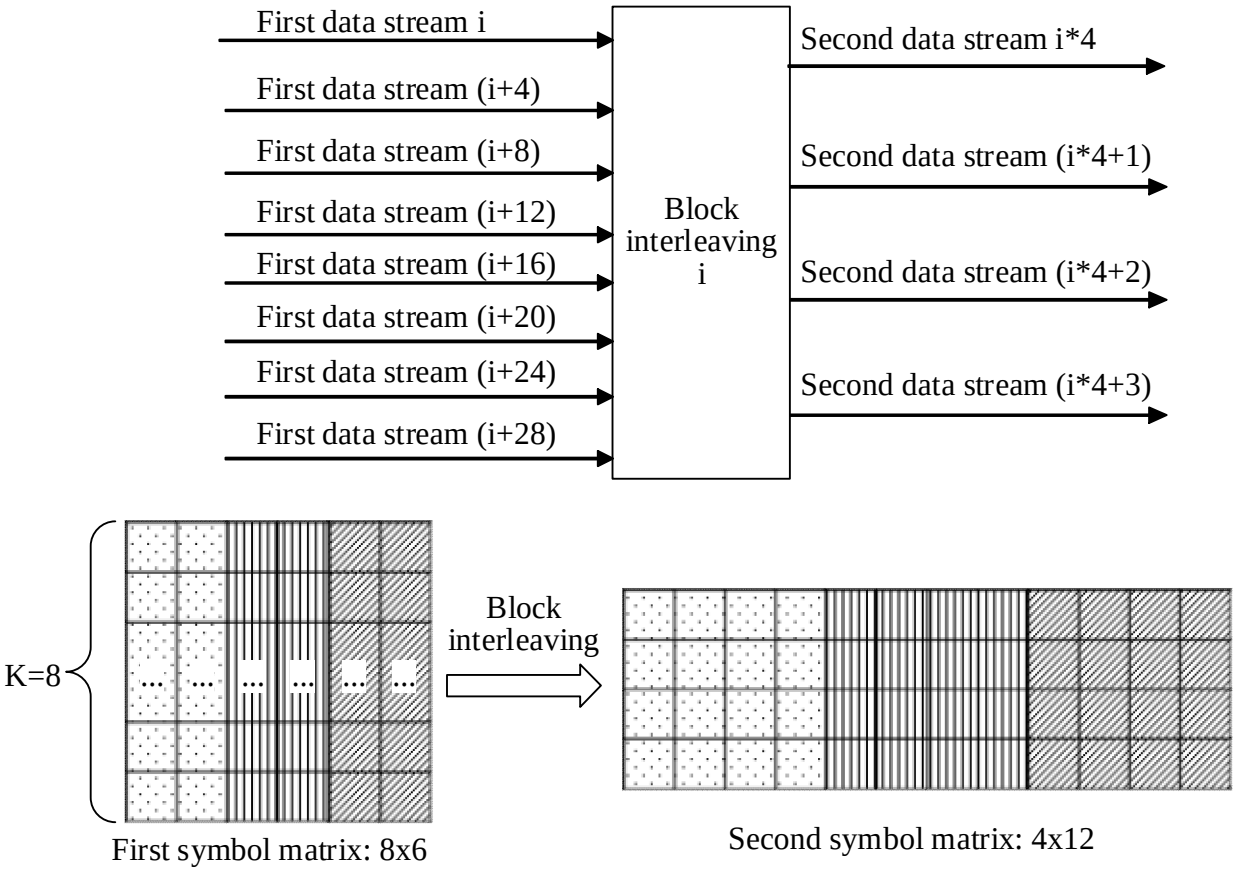

First data stream i
First data stream (i+4)
First data stream (i+8)
First data stream (i+12)
First data stream (i+16)
First data stream (i+20)
First data stream (i+24)
First data stream (i+28)
Block interleaving i
Second data stream i*4
Second data stream (i*4+1)
Second data stream (i*4+2)
Second data stream (i*4+3)
K=8
Block interleaving
First symbol matrix: 8x6
Second symbol matrix: 4x12

FIG. 38

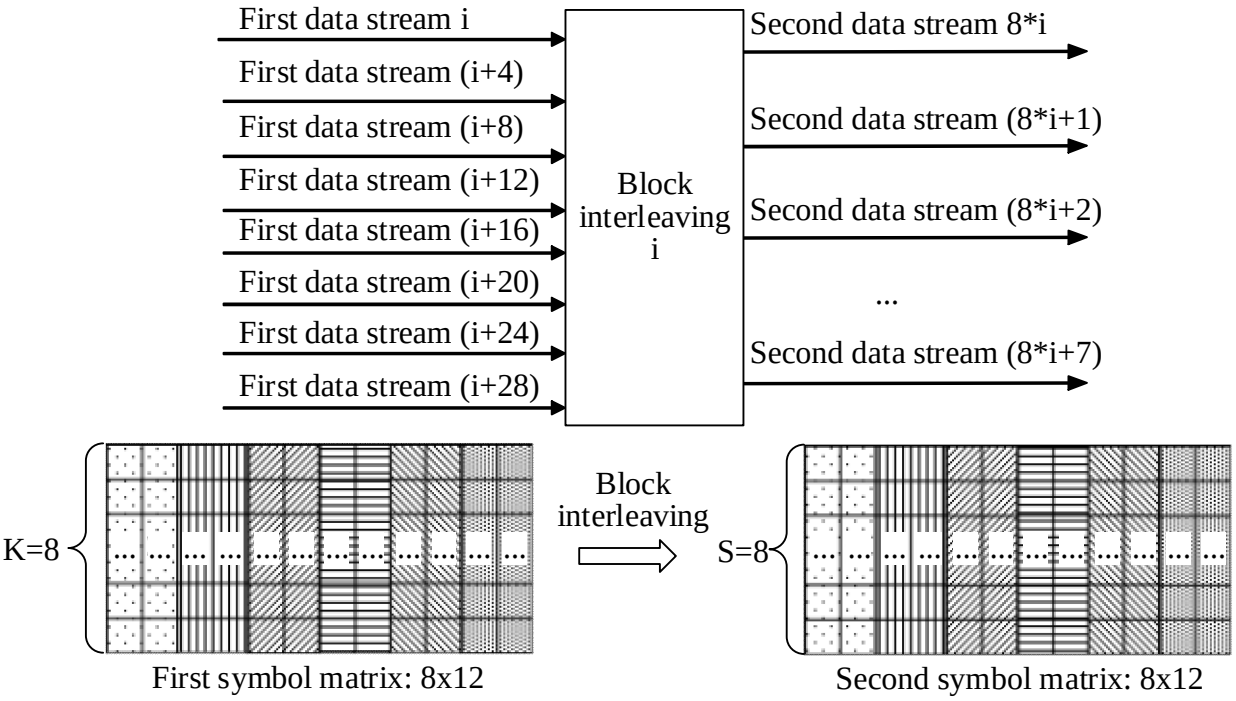

First data stream i
First data stream (i+4)
First data stream (i+8)
First data stream (i+12)
First data stream (i+16)
First data stream (i+20)
First data stream (i+24)
First data stream (i+28)
Block interleaving i
Second data stream 8*i
Second data stream (8*i+1)
Second data stream (8*i+2)
...
Second data stream (8*i+7)
K=8
Block interleaving
S=8
First symbol matrix: 8x12
Second symbol matrix: 8x12

FIG. 39

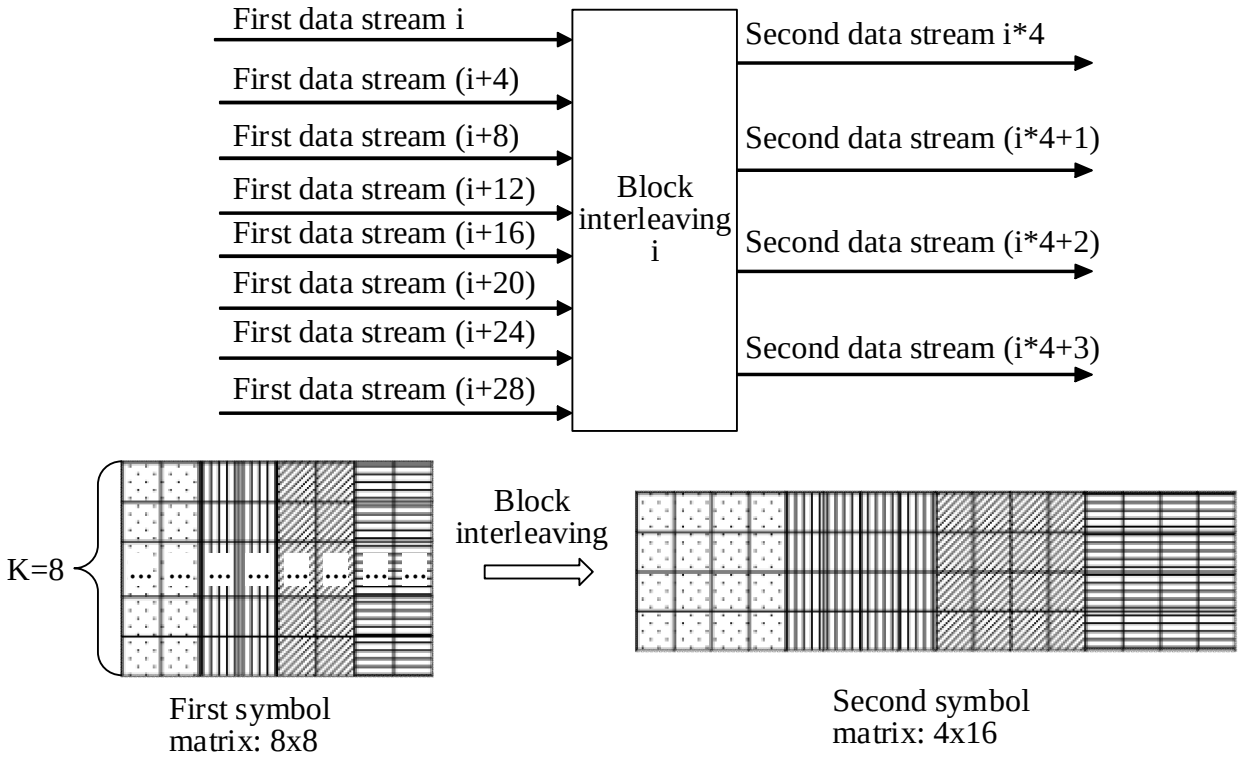

First data stream i
First data stream (i+4)
First data stream (i+8)
First data stream (i+12)
First data stream (i+16)
First data stream (i+20)
First data stream (i+24)
First data stream (i+28)
Block interleaving i
Second data stream i*4
Second data stream (i*4+1)
Second data stream (i*4+2)
Second data stream (i*4+3)
K=8
Block interleaving
First symbol matrix: 8x8
Second symbol matrix: 4x16

FIG. 40

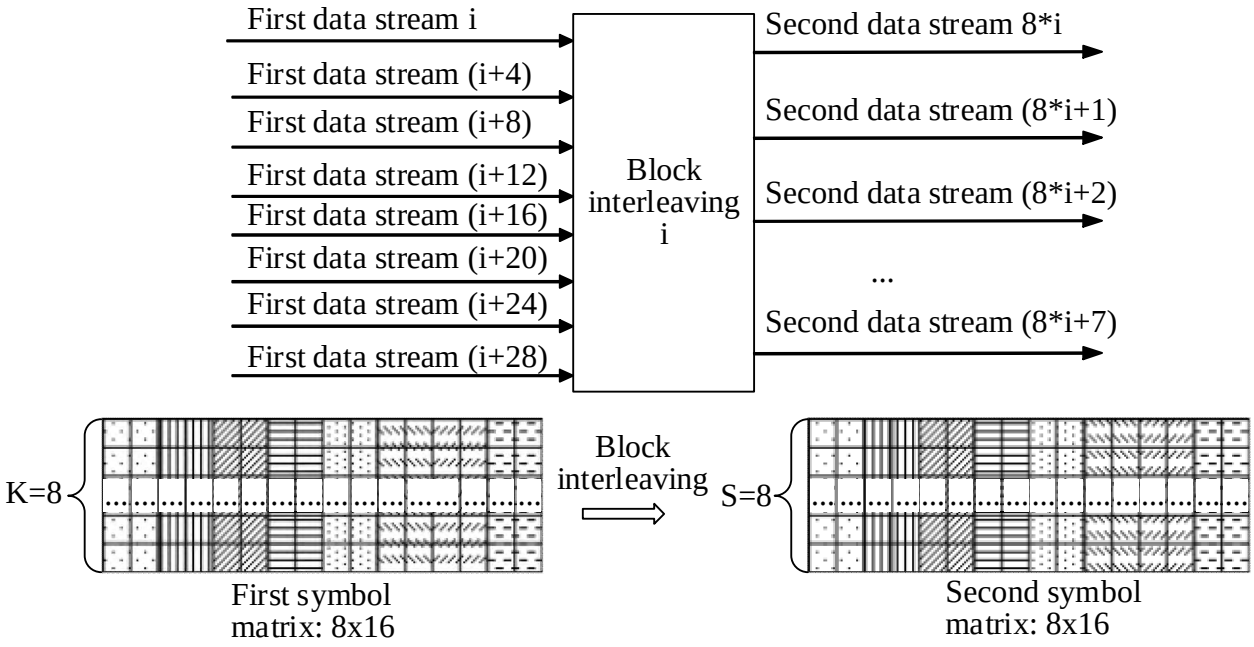

First data stream i
First data stream (i+4)
First data stream (i+8)
First data stream (i+12)
First data stream (i+16)
First data stream (i+20)
First data stream (i+24)
First data stream (i+28)
Block interleaving i
Second data stream 8*i
Second data stream (8*i+1)
Second data stream (8*i+2)
...
Second data stream (8*i+7)
K=8
Block interleaving
S=8
First symbol matrix: 8x16
Second symbol matrix: 8x16

FIG. 41

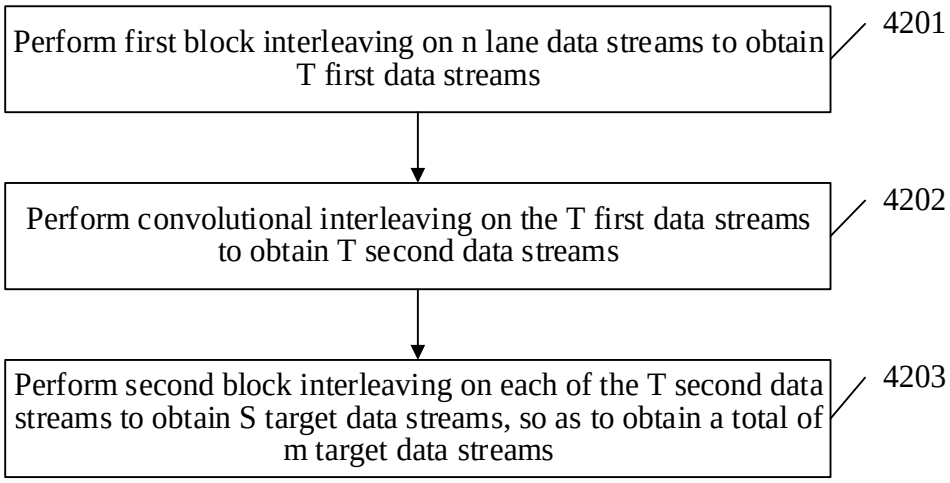

Perform first block interleaving on n lane data streams to obtain T first data streams
4201
Perform convolutional interleaving on the T first data streams to obtain T second data streams
4202
Perform second block interleaving on each of the T second data streams to obtain S target data streams, so as to obtain a total of m target data streams
4203

FIG. 42

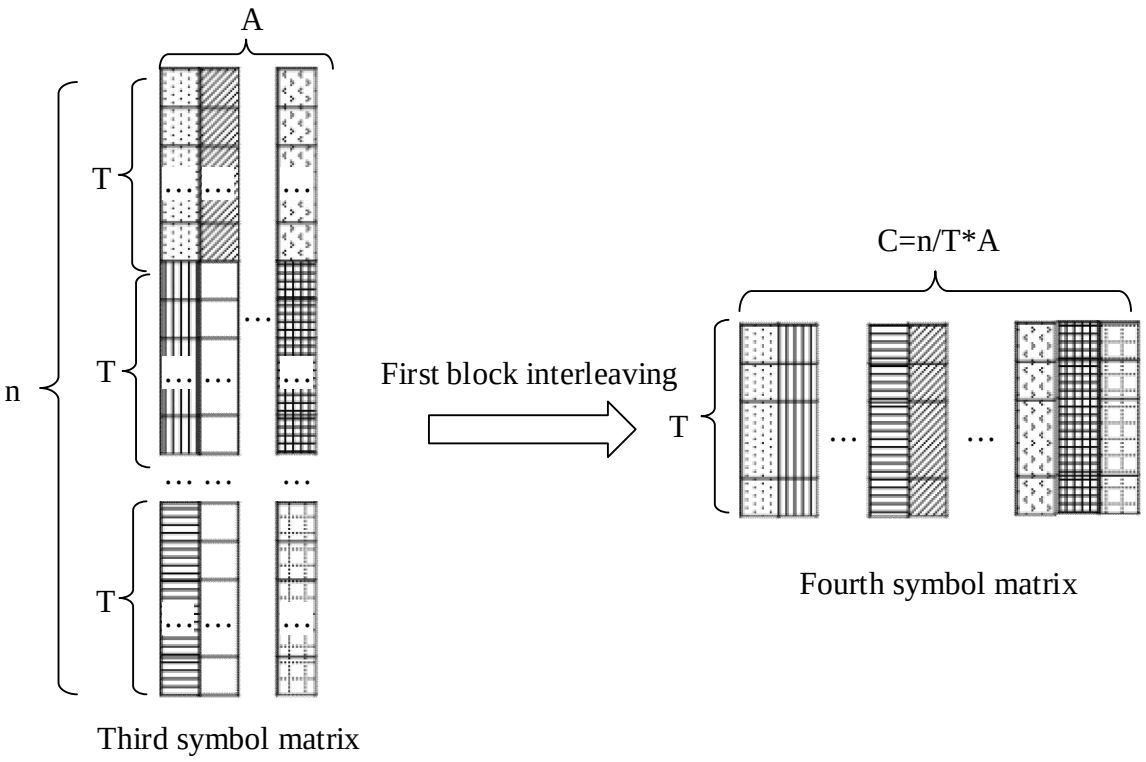

A
T
T
T
n
Third symbol matrix
First block interleaving
C=n/T*A
T
Fourth symbol matrix

FIG. 43

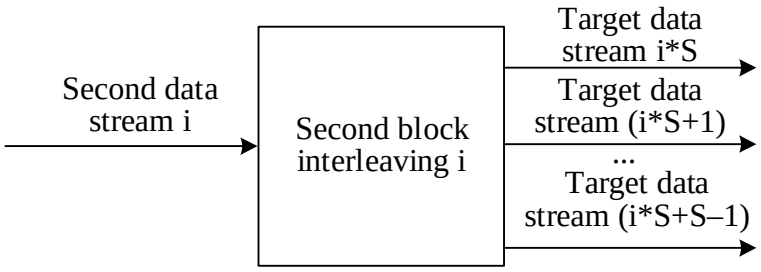


FIG. 44(a)

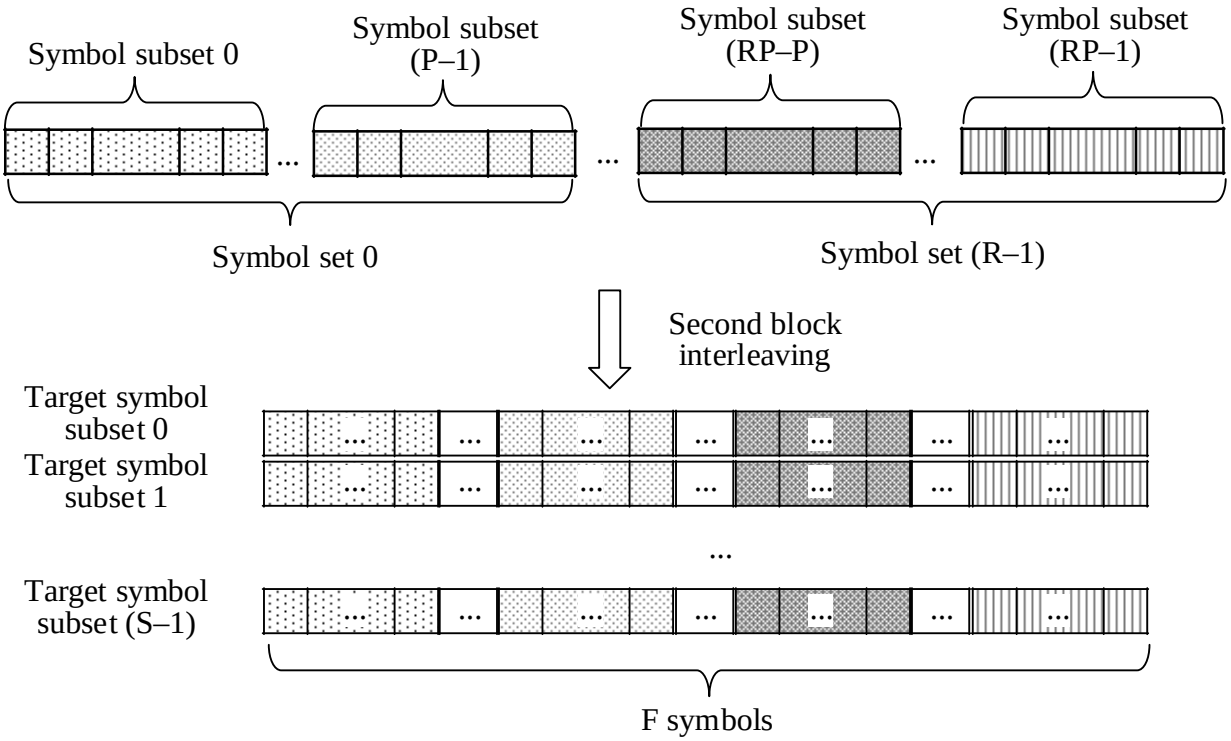


FIG. 44(b)

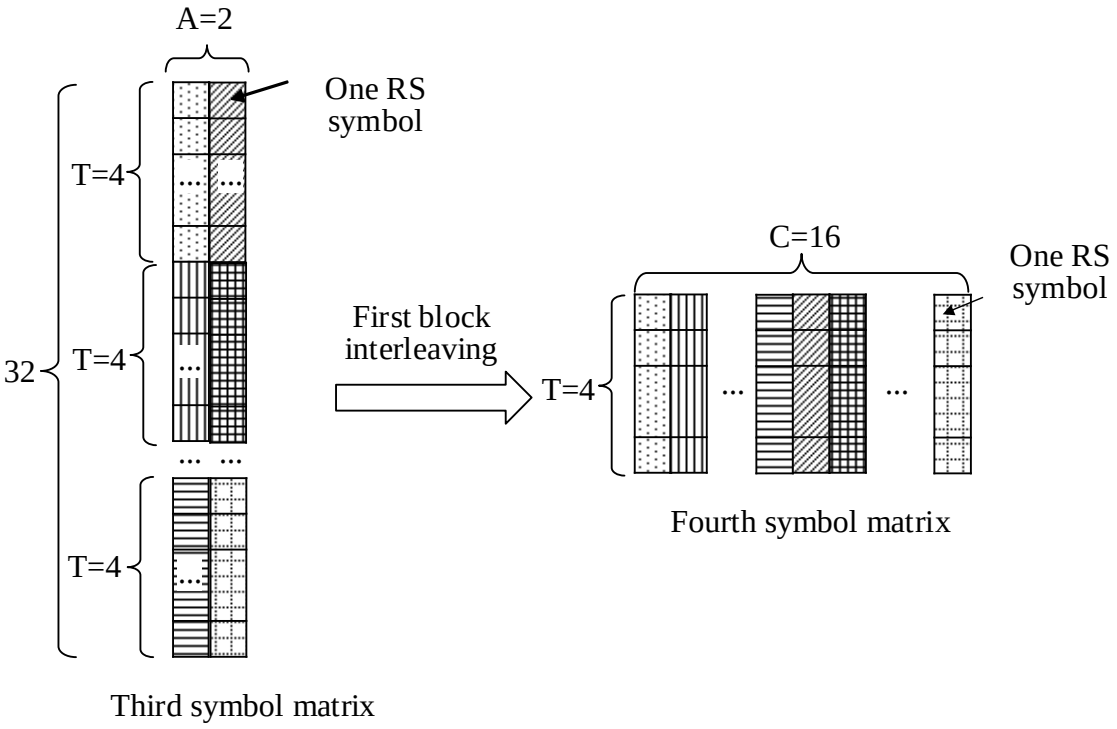


FIG. 45(a)

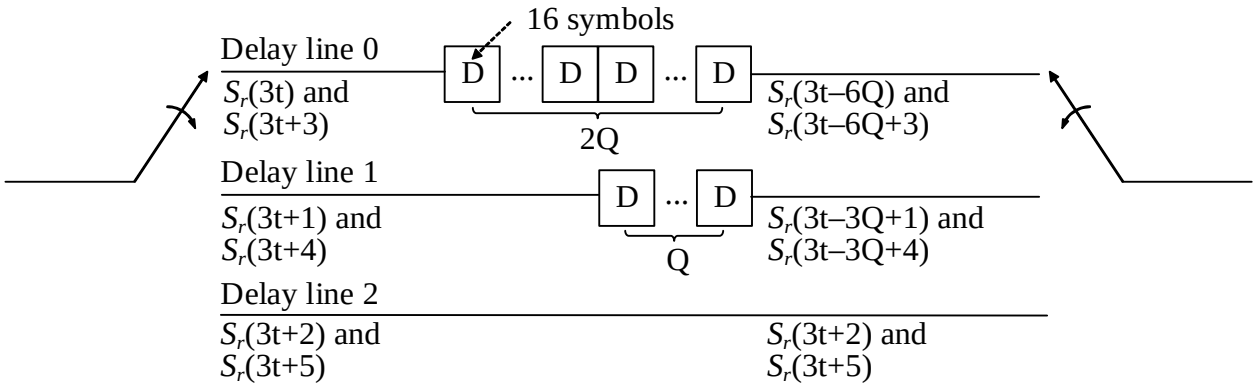


FIG. 45(b)

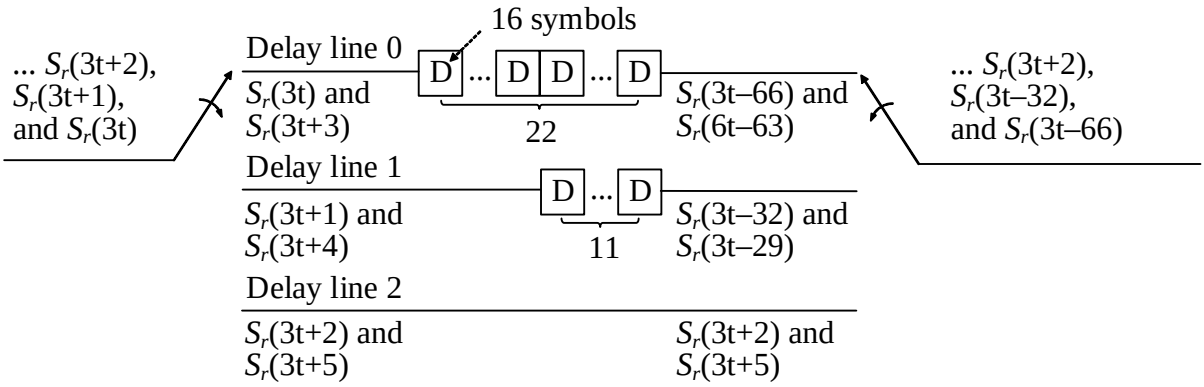


FIG. 45(c)

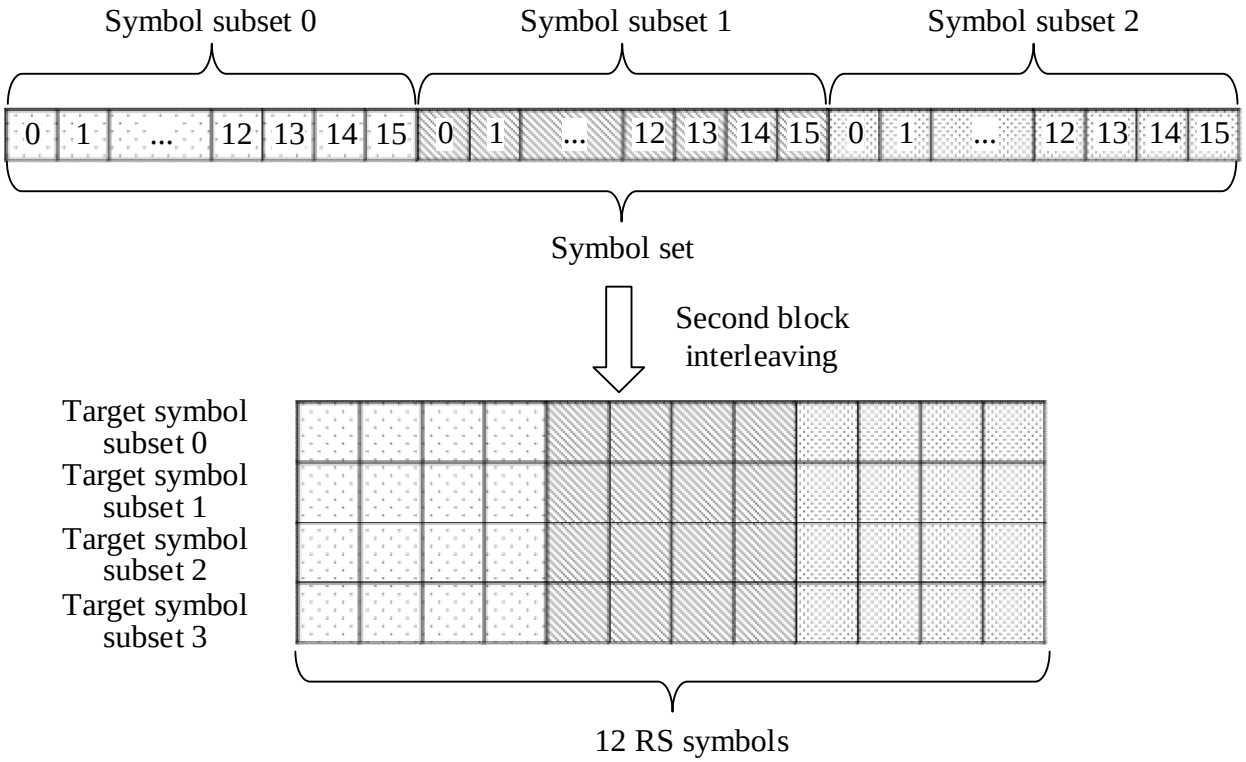


FIG. 45(d)

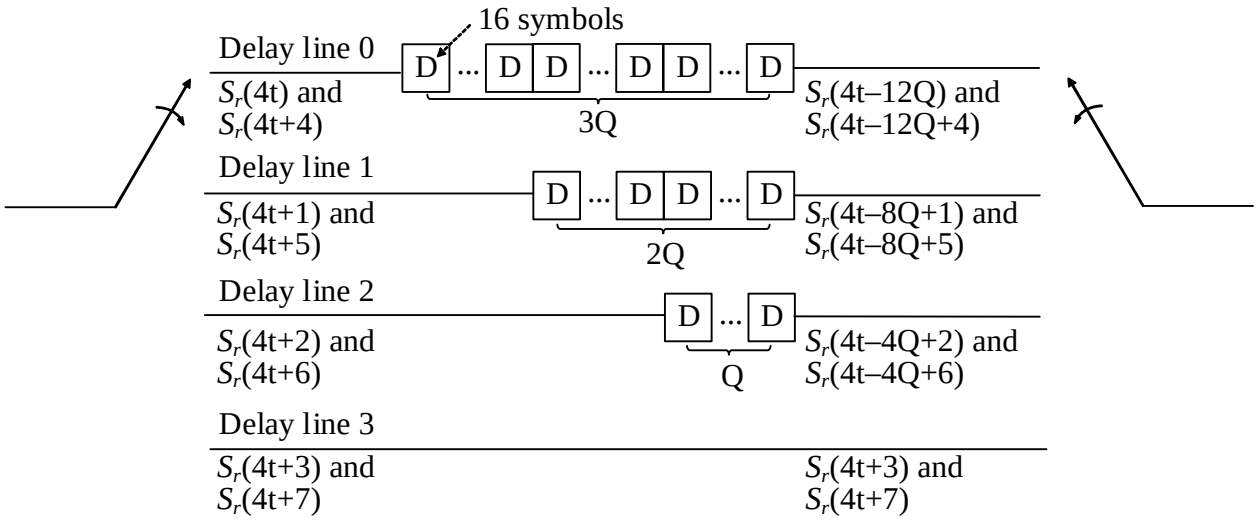


FIG. 46(a)

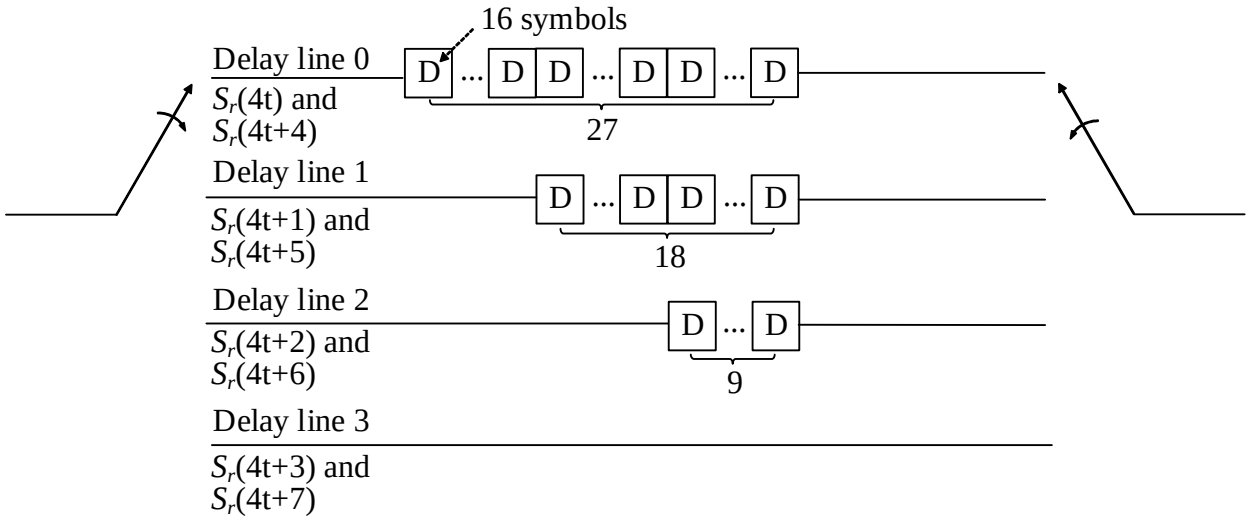


FIG. 46(b)

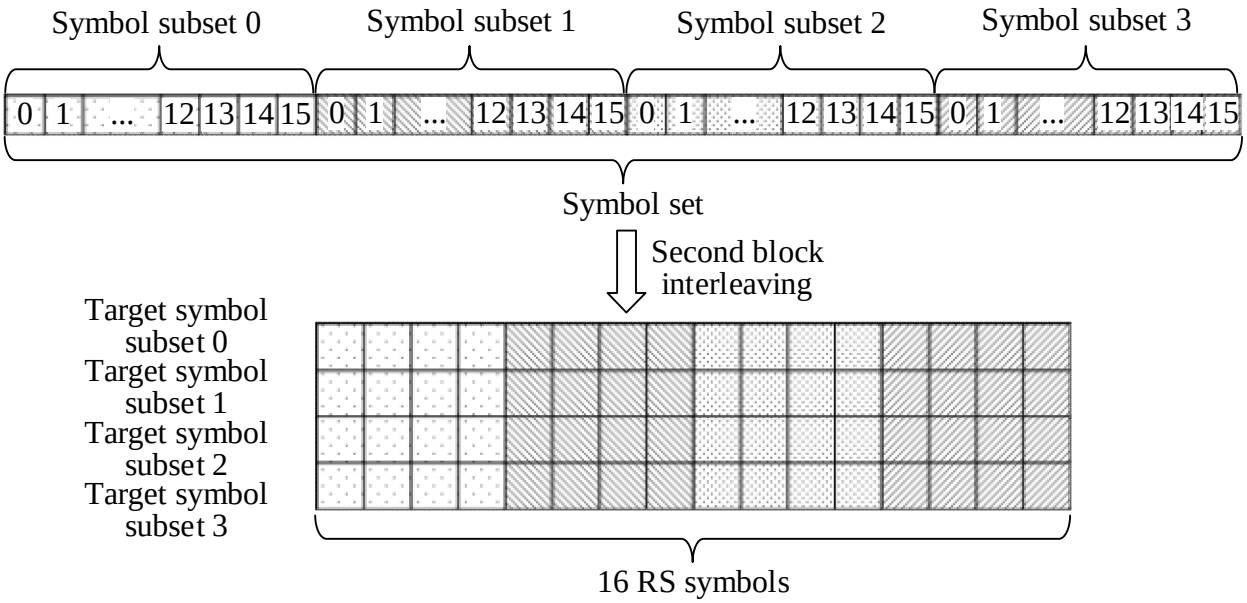


FIG. 46(c)

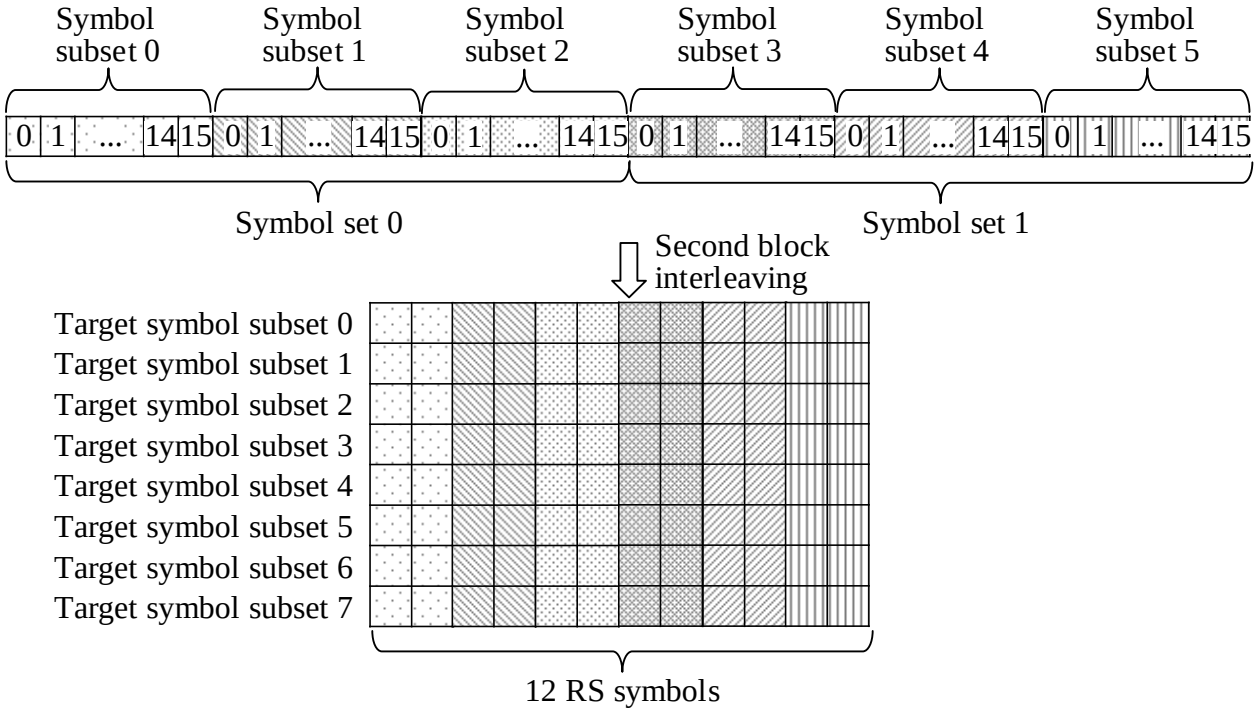


FIG. 47

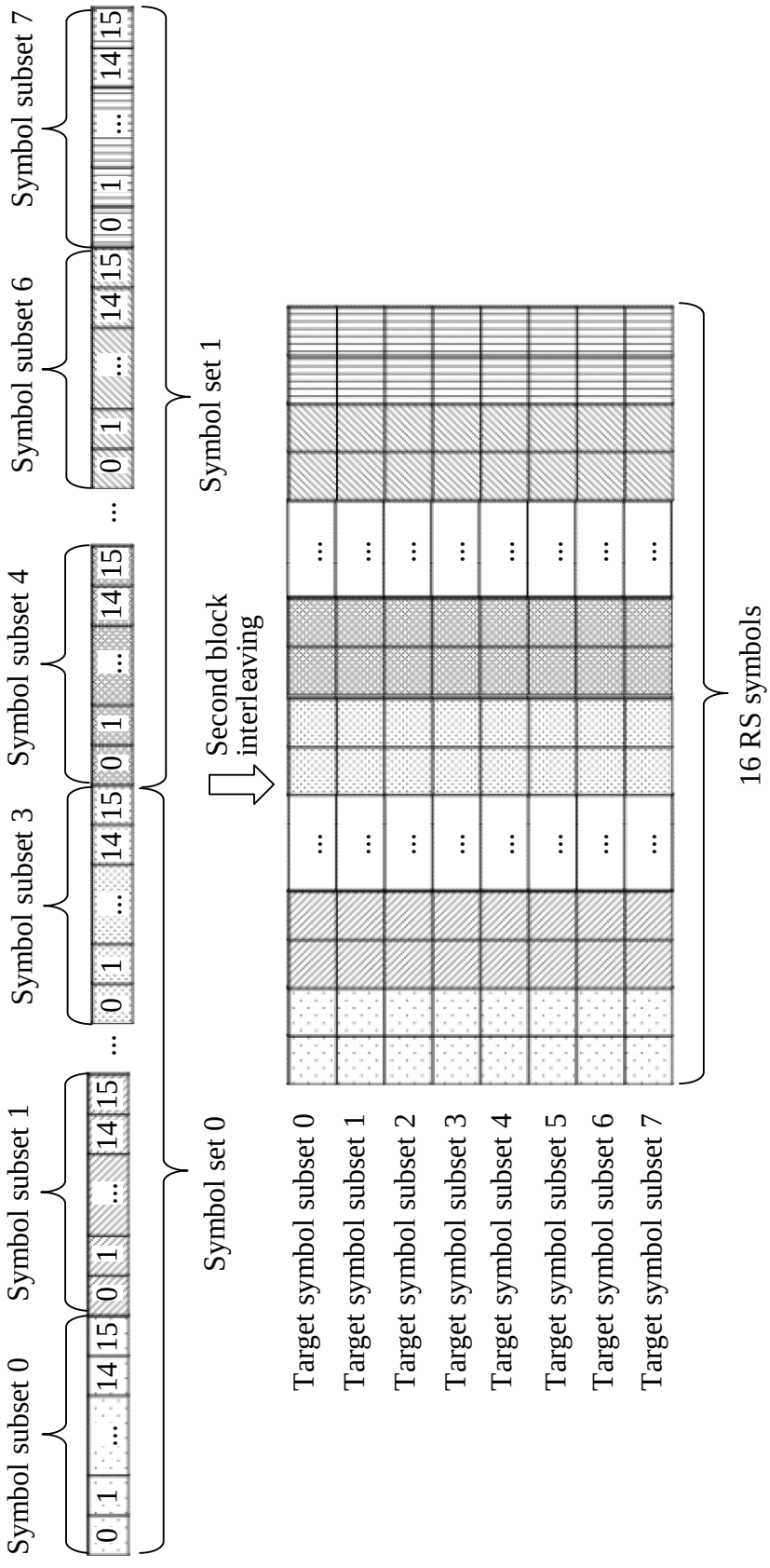

Symbol subset 0
Symbol subset 1
Symbol subset 3
Symbol subset 4
Symbol subset 6
Symbol subset 7
0 1 ... 14 15
Symbol set 0
Symbol set 1
Second block interleaving
Target symbol subset 0
Target symbol subset 1
Target symbol subset 2
Target symbol subset 3
Target symbol subset 4
Target symbol subset 5
Target symbol subset 6
Target symbol subset 7
16 RS symbols

FIG. 48

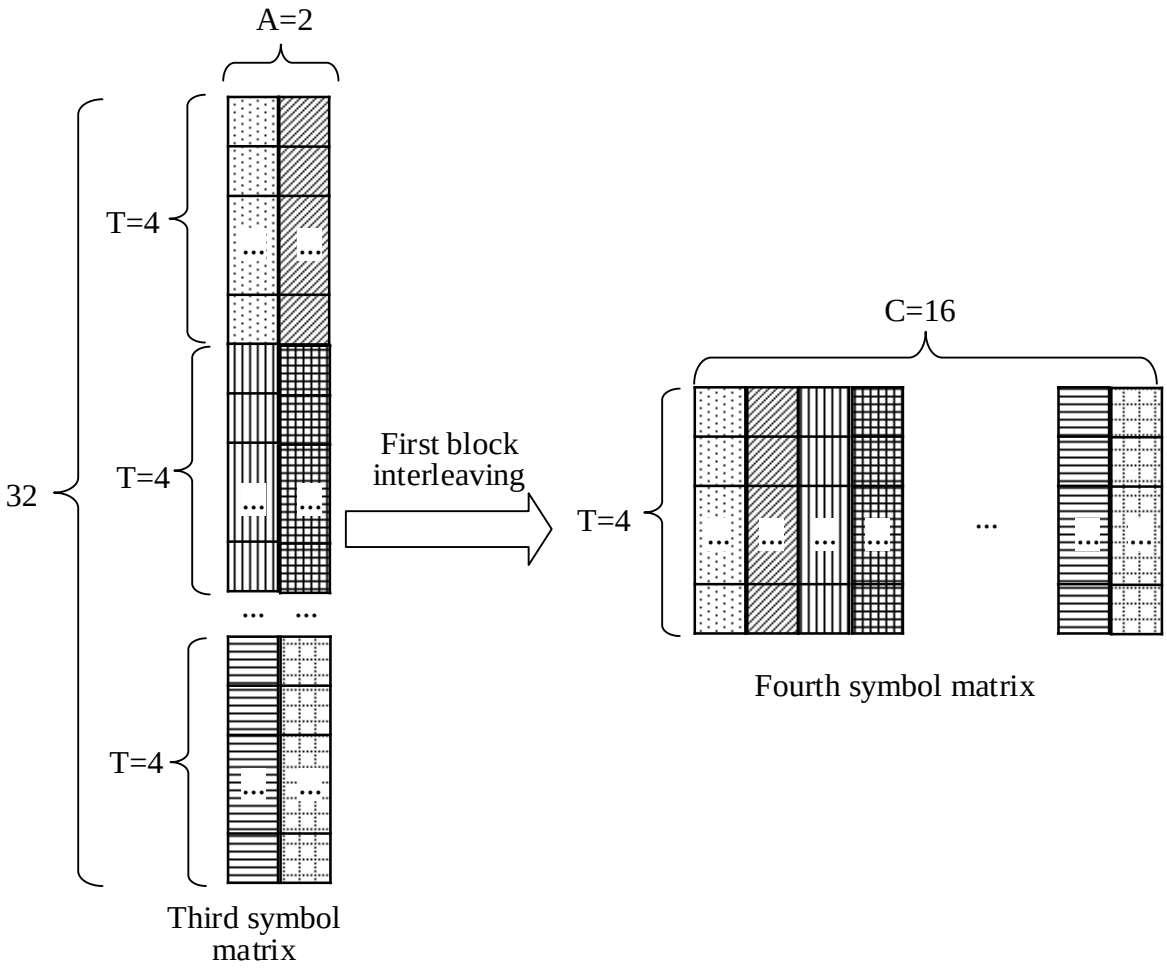


FIG. 49

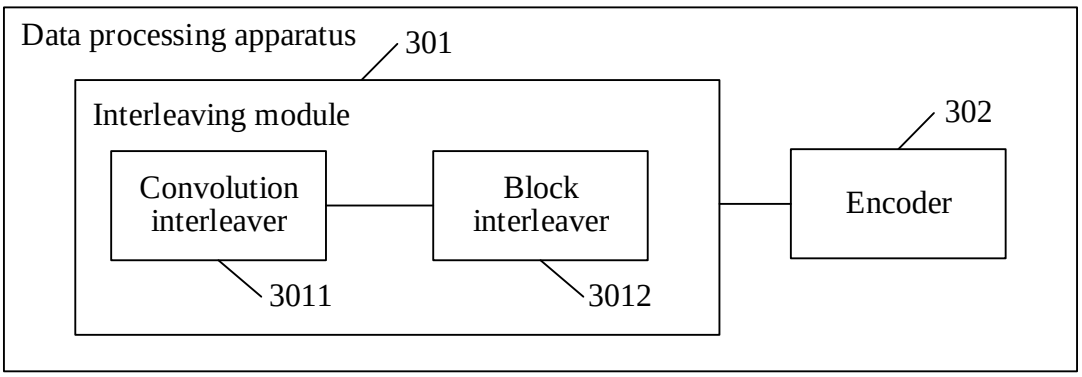


FIG. 50(a)

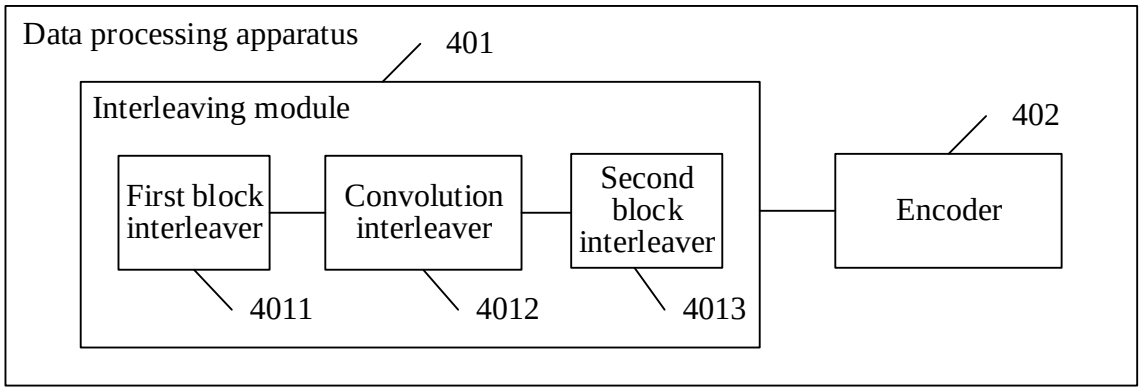


FIG. 50(b)

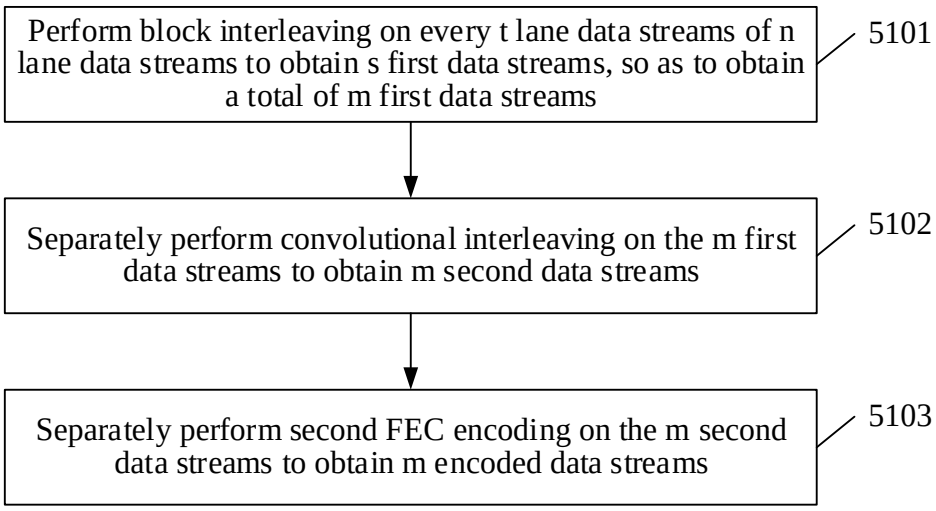


FIG. 51

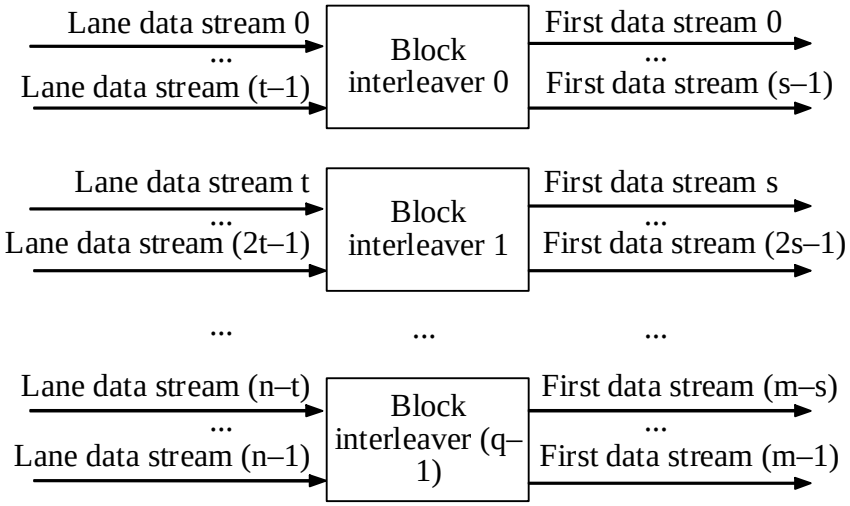


FIG. 52

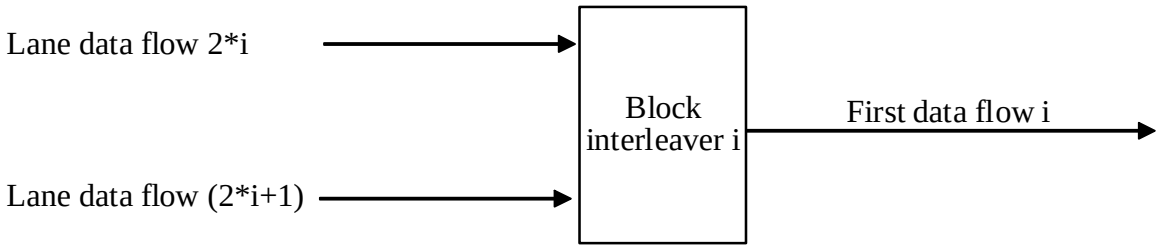


FIG. 53

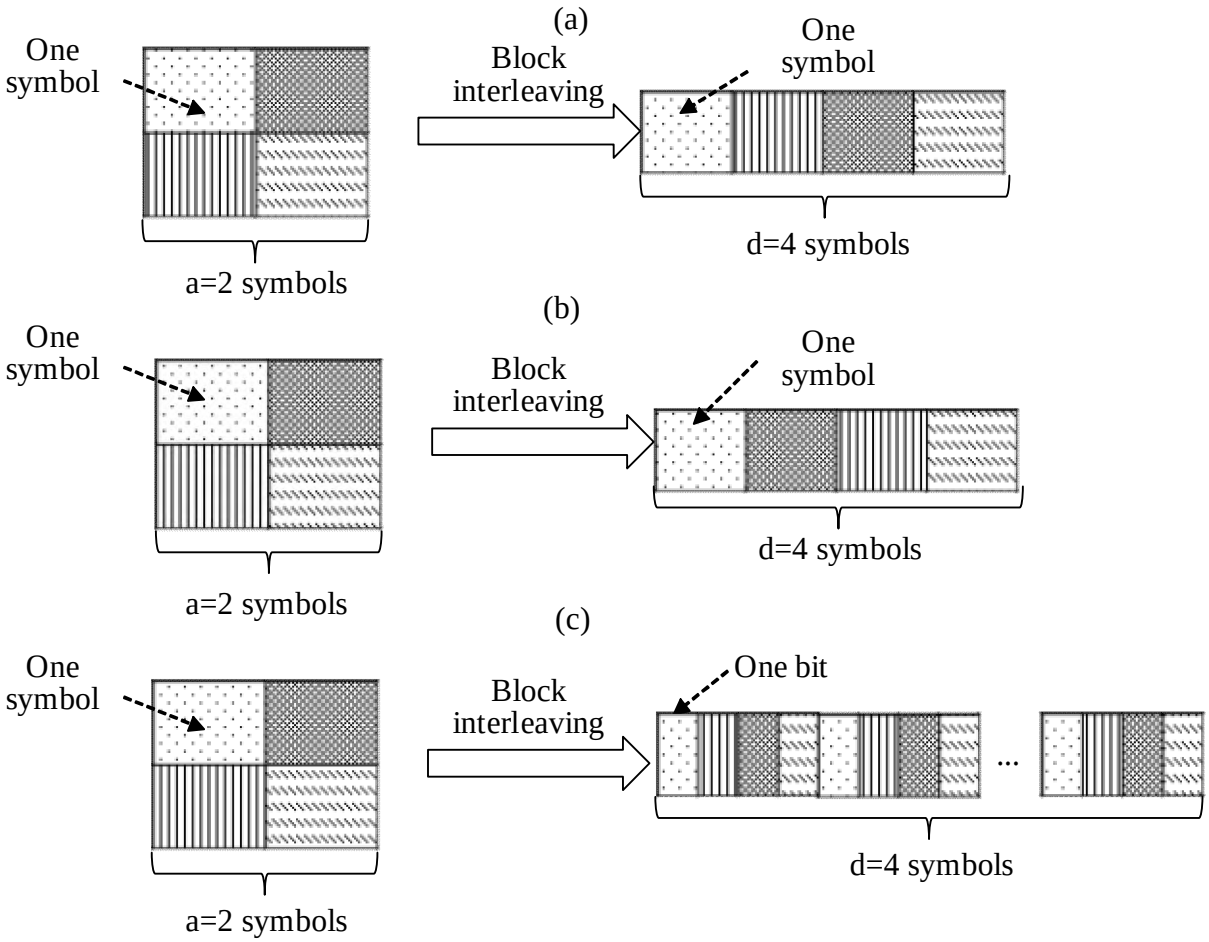


FIG. 54

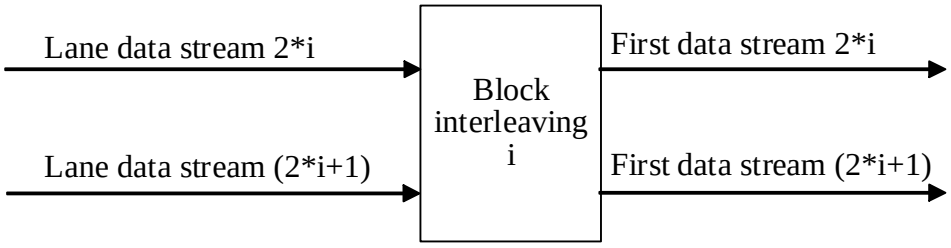


FIG. 55

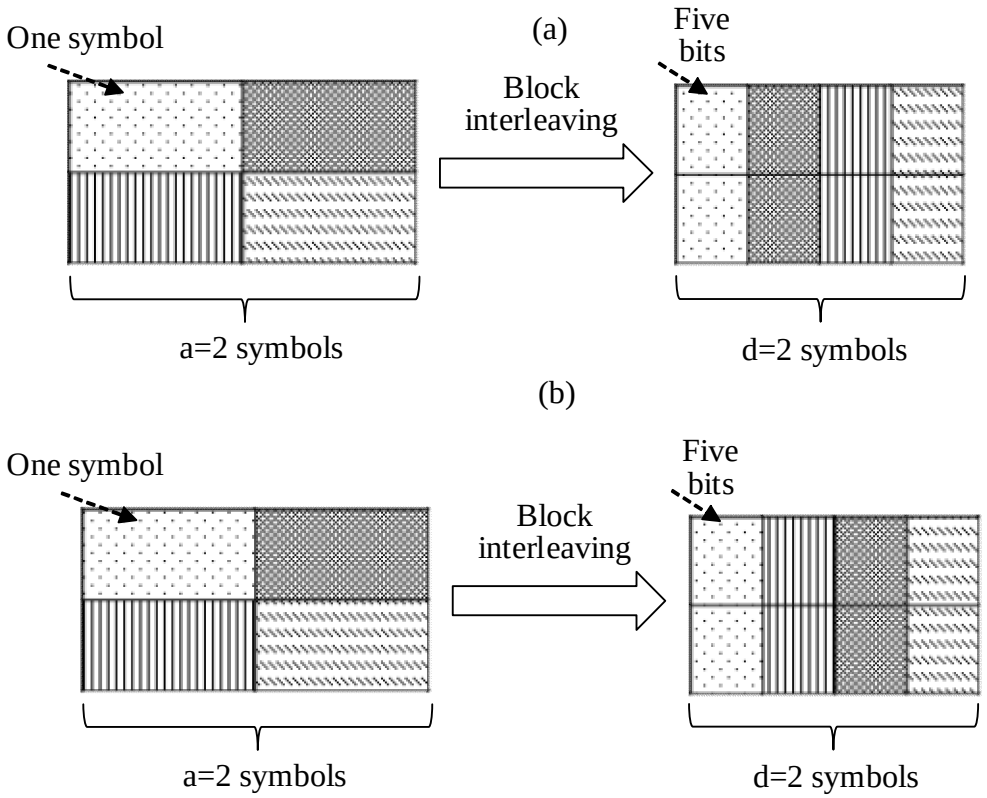

One symbol
(a)
Five bits
Block interleaving
a=2 symbols
d=2 symbols
(b)
One symbol
Five bits
Block interleaving
a=2 symbols
d=2 symbols

FIG. 56

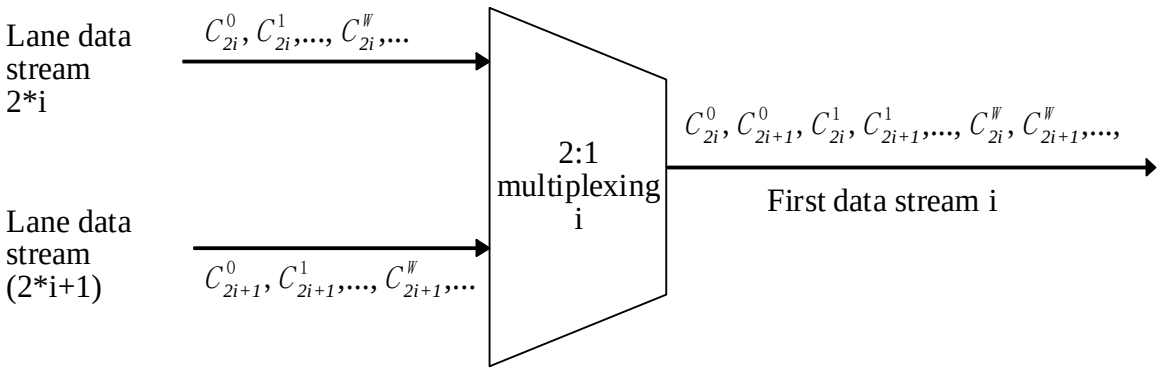

Lane data stream 2*i
$C_{2i}^{0}, C_{2i}^{1},..., C_{2i}^{W},...$
Lane data stream (2*i+1)
$C_{2i+1}^{0}, C_{2i+1}^{1},..., C_{2i+1}^{W},...$
2:1 multiplexing i
$C_{2i}^{0}, C_{2i+1}^{0}, C_{2i}^{1}, C_{2i+1}^{1},..., C_{2i}^{W}, C_{2i+1}^{W},...,$
First data stream i

FIG. 57

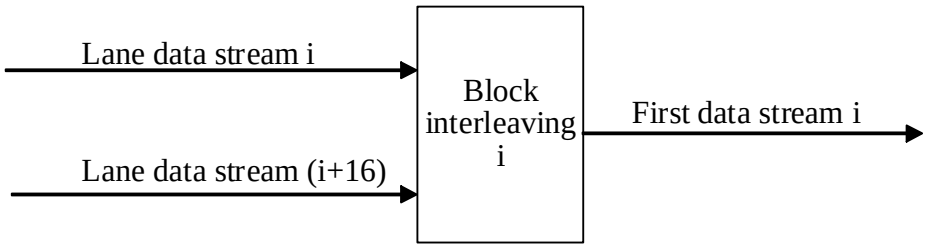


FIG. 58

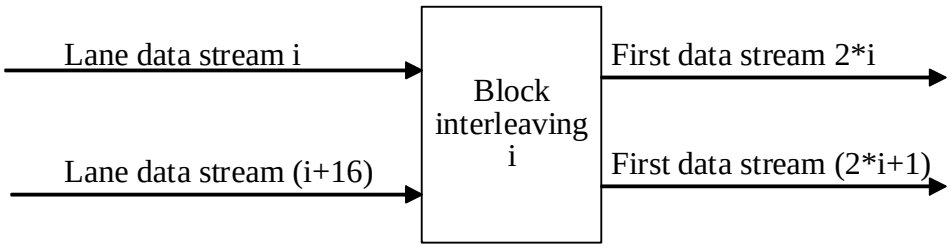


FIG. 59

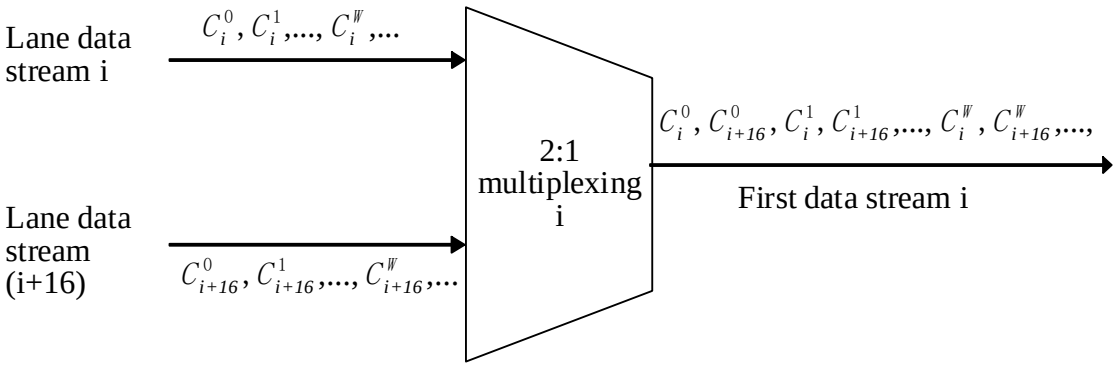


FIG. 60

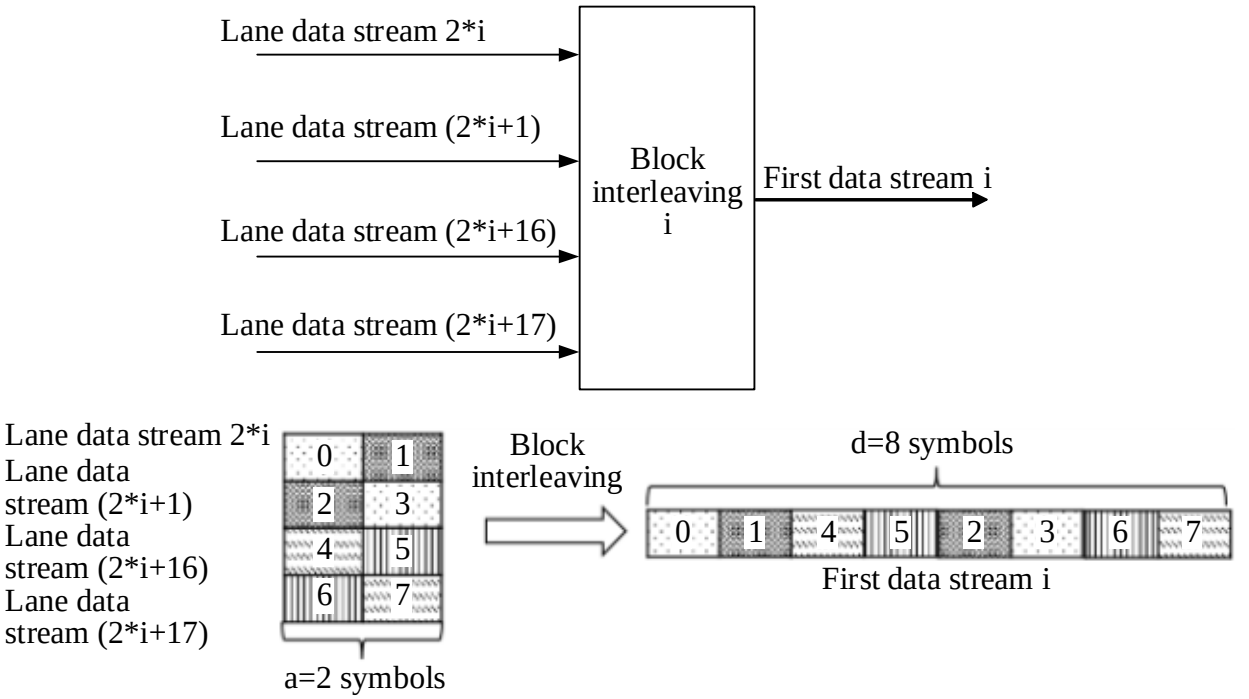

Lane data stream 2*i
Lane data stream (2*i+1)
Lane data stream (2*i+16)
Lane data stream (2*i+17)
Block interleaving i
First data stream i
Lane data stream 2*i
Lane data stream (2*i+1)
Lane data stream (2*i+16)
Lane data stream (2*i+17)
0
1
2
3
4
5
6
7
a=2 symbols
Block interleaving
d=8 symbols
0
1
4
5
2
3
6
7
First data stream i

FIG. 61

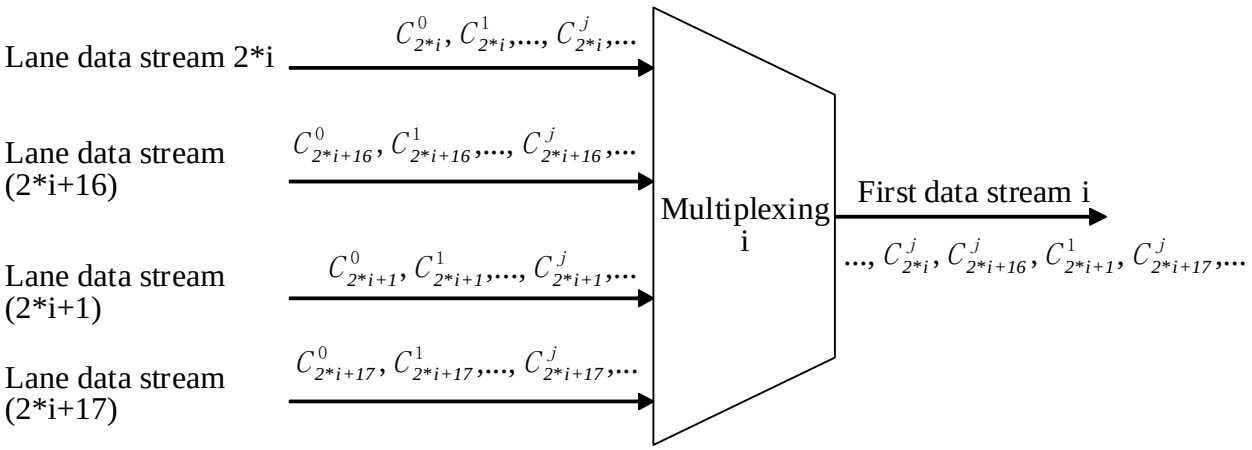

Lane data stream 2*i
$C^0_{2*i}, C^1_{2*i}, \ldots, C^j_{2*i}, \ldots$
Lane data stream (2*i+16)
$C^0_{2*i+16}, C^1_{2*i+16}, \ldots, C^j_{2*i+16}, \ldots$
Lane data stream (2*i+1)
$C^0_{2*i+1}, C^1_{2*i+1}, \ldots, C^j_{2*i+1}, \ldots$
Lane data stream (2*i+17)
$C^0_{2*i+17}, C^1_{2*i+17}, \ldots, C^j_{2*i+17}, \ldots$
Multiplexing i
First data stream i
$\ldots, C^j_{2*i}, C^j_{2*i+16}, C^1_{2*i+1}, C^j_{2*i+17}, \ldots$

FIG. 62

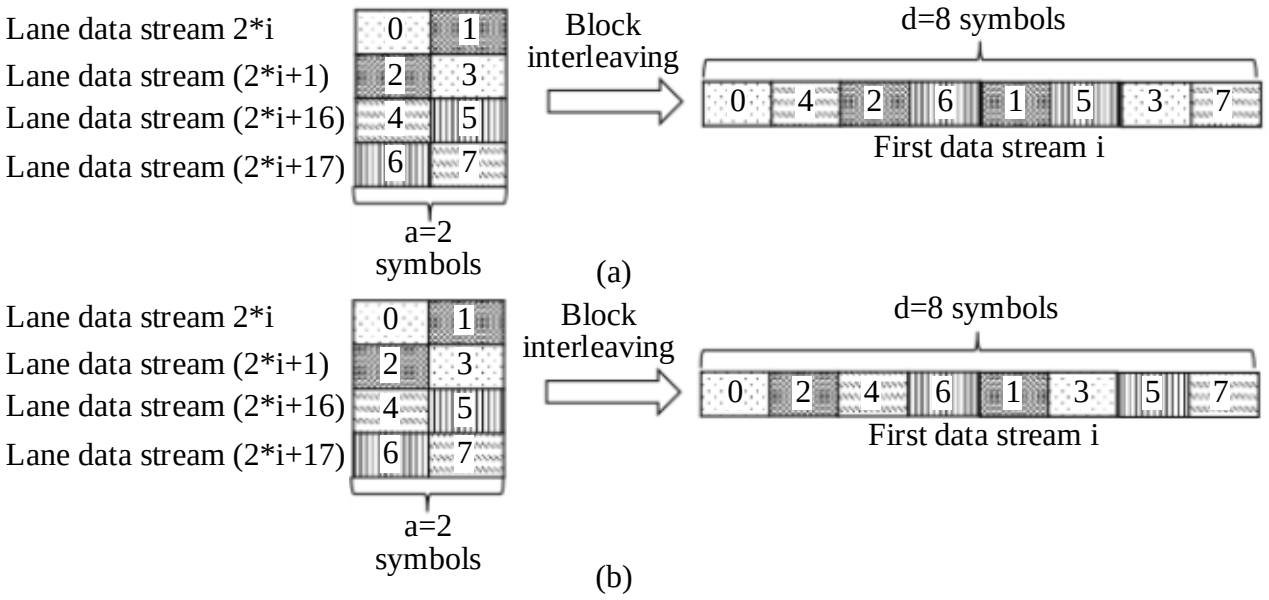

Lane data stream 2*i
Lane data stream (2*i+1)
Lane data stream (2*i+16)
Lane data stream (2*i+17)
0
1
2
3
4
5
6
7
a=2 symbols
Block interleaving
d=8 symbols
0 4 2 6 1 5 3 7
First data stream i
(a)
Lane data stream 2*i
Lane data stream (2*i+1)
Lane data stream (2*i+16)
Lane data stream (2*i+17)
0
1
2
3
4
5
6
7
a=2 symbols
Block interleaving
d=8 symbols
0 2 4 6 1 3 5 7
First data stream i
(b)

FIG. 63

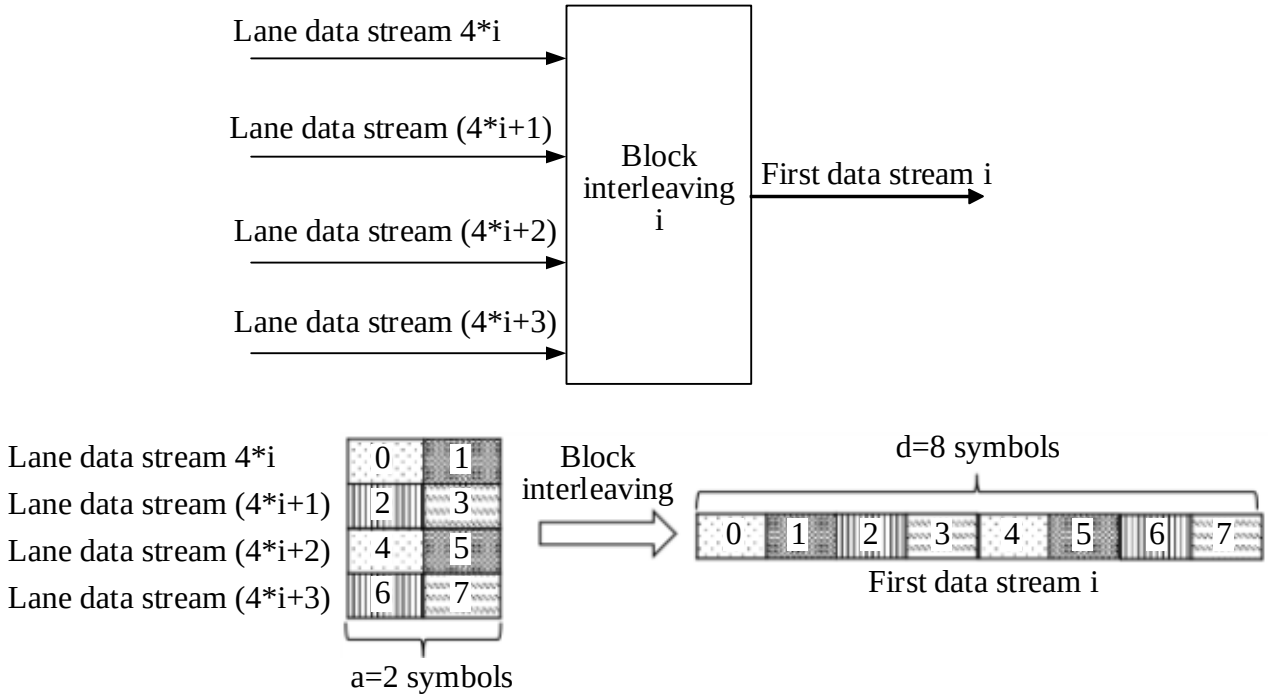

Lane data stream 4*i
Lane data stream (4*i+1)
Lane data stream (4*i+2)
Lane data stream (4*i+3)
Block interleaving i
First data stream i
Lane data stream 4*i
Lane data stream (4*i+1)
Lane data stream (4*i+2)
Lane data stream (4*i+3)
0
1
2
3
4
5
6
7
a=2 symbols
Block interleaving
d=8 symbols
0 1 2 3 4 5 6 7
First data stream i

FIG. 64

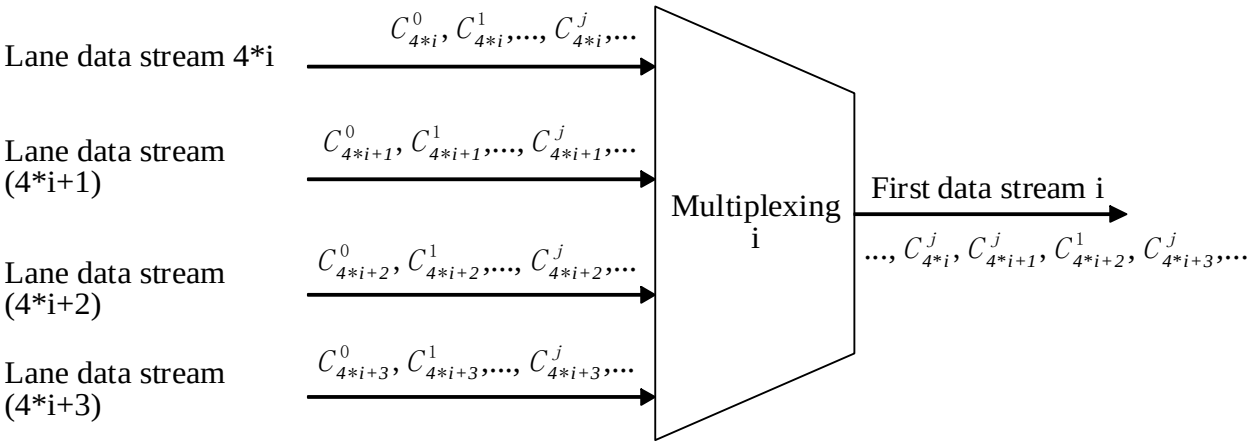

Lane data stream 4*i
$C^0_{4*i}, C^1_{4*i}, \ldots, C^j_{4*i}, \ldots$
Lane data stream (4*i+1)
$C^0_{4*i+1}, C^1_{4*i+1}, \ldots, C^j_{4*i+1}, \ldots$
Lane data stream (4*i+2)
$C^0_{4*i+2}, C^1_{4*i+2}, \ldots, C^j_{4*i+2}, \ldots$
Lane data stream (4*i+3)
$C^0_{4*i+3}, C^1_{4*i+3}, \ldots, C^j_{4*i+3}, \ldots$
Multiplexing i
First data stream i
$\ldots, C^j_{4*i}, C^j_{4*i+1}, C^1_{4*i+2}, C^j_{4*i+3}, \ldots$

FIG. 65

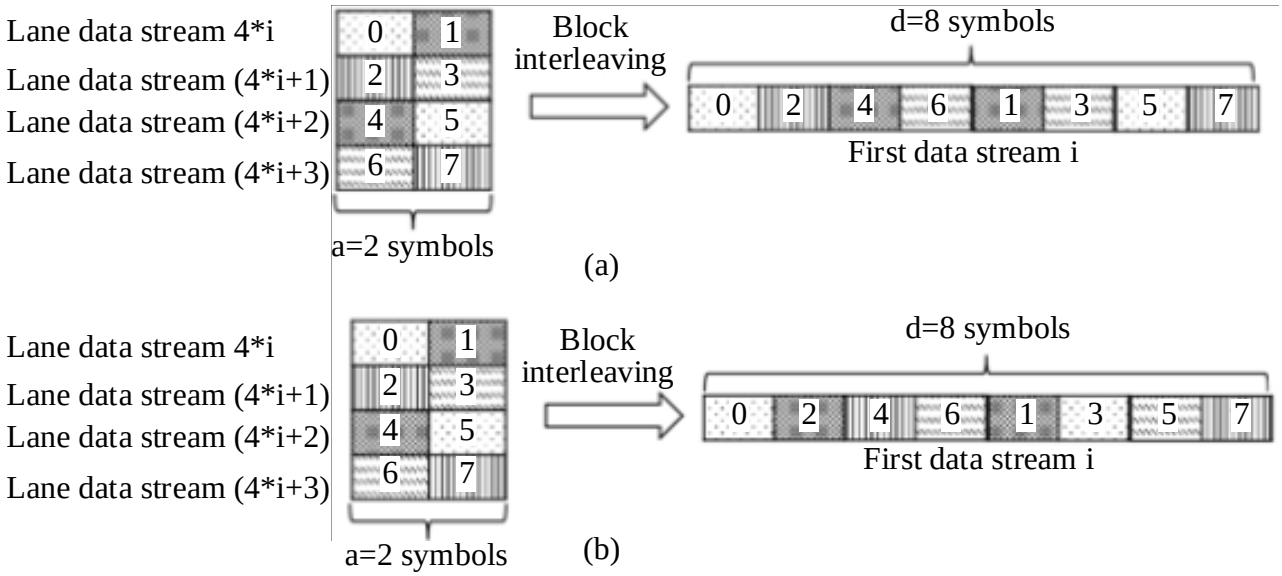

Lane data stream 4*i
Lane data stream (4*i+1)
Lane data stream (4*i+2)
Lane data stream (4*i+3)
0 1
2 3
4 5
6 7
a=2 symbols
Block interleaving
d=8 symbols
0 2 4 6 1 3 5 7
First data stream i
(a)
Lane data stream 4*i
Lane data stream (4*i+1)
Lane data stream (4*i+2)
Lane data stream (4*i+3)
0 1
2 3
4 5
6 7
a=2 symbols
Block interleaving
d=8 symbols
0 2 4 6 1 3 5 7
First data stream i
(b)

FIG. 66

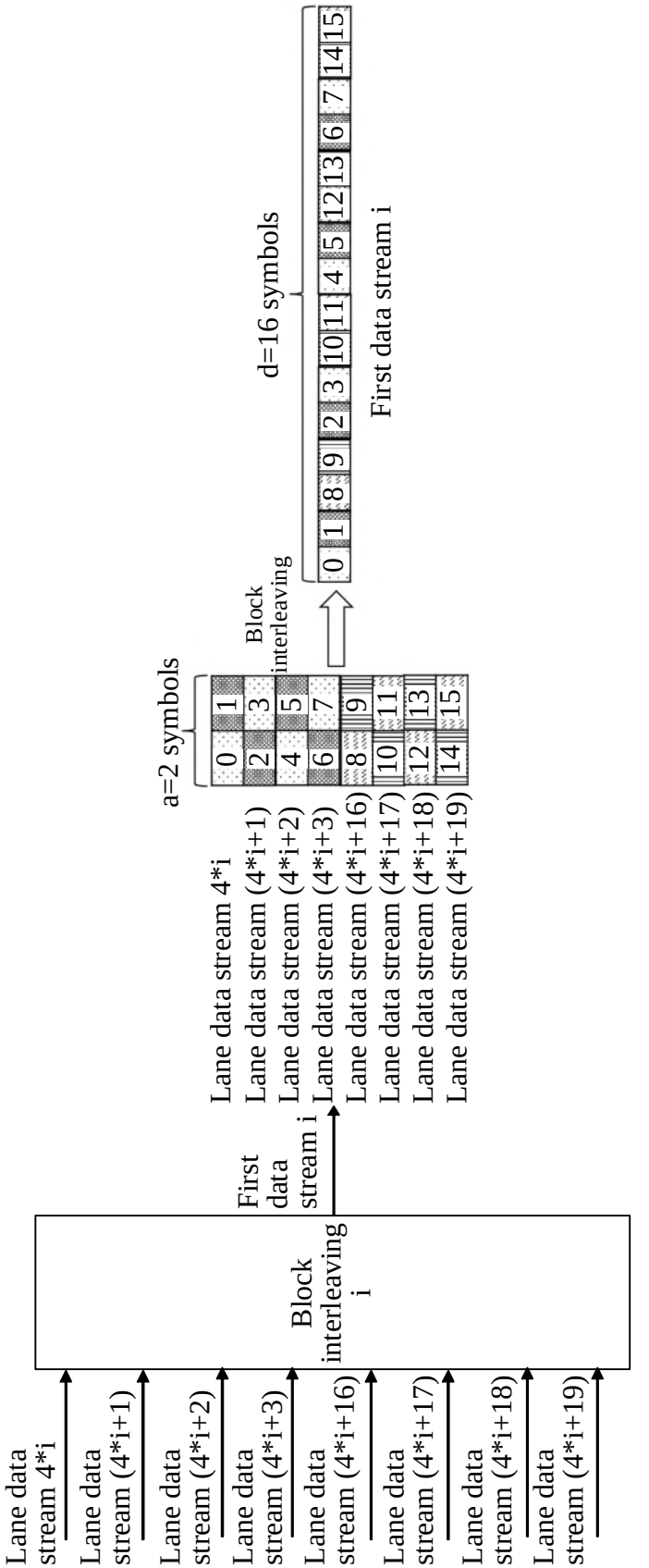

Lane data stream 4*i
Lane data stream (4*i+1)
Lane data stream (4*i+2)
Lane data stream (4*i+3)
Lane data stream (4*i+16)
Lane data stream (4*i+17)
Lane data stream (4*i+18)
Lane data stream (4*i+19)
Block interleaving i
First data stream i
Lane data stream 4*i
Lane data stream (4*i+1)
Lane data stream (4*i+2)
Lane data stream (4*i+3)
Lane data stream (4*i+16)
Lane data stream (4*i+17)
Lane data stream (4*i+18)
Lane data stream (4*i+19)
a=2 symbols
Block interleaving
d=16 symbols
First data stream i

FIG. 67

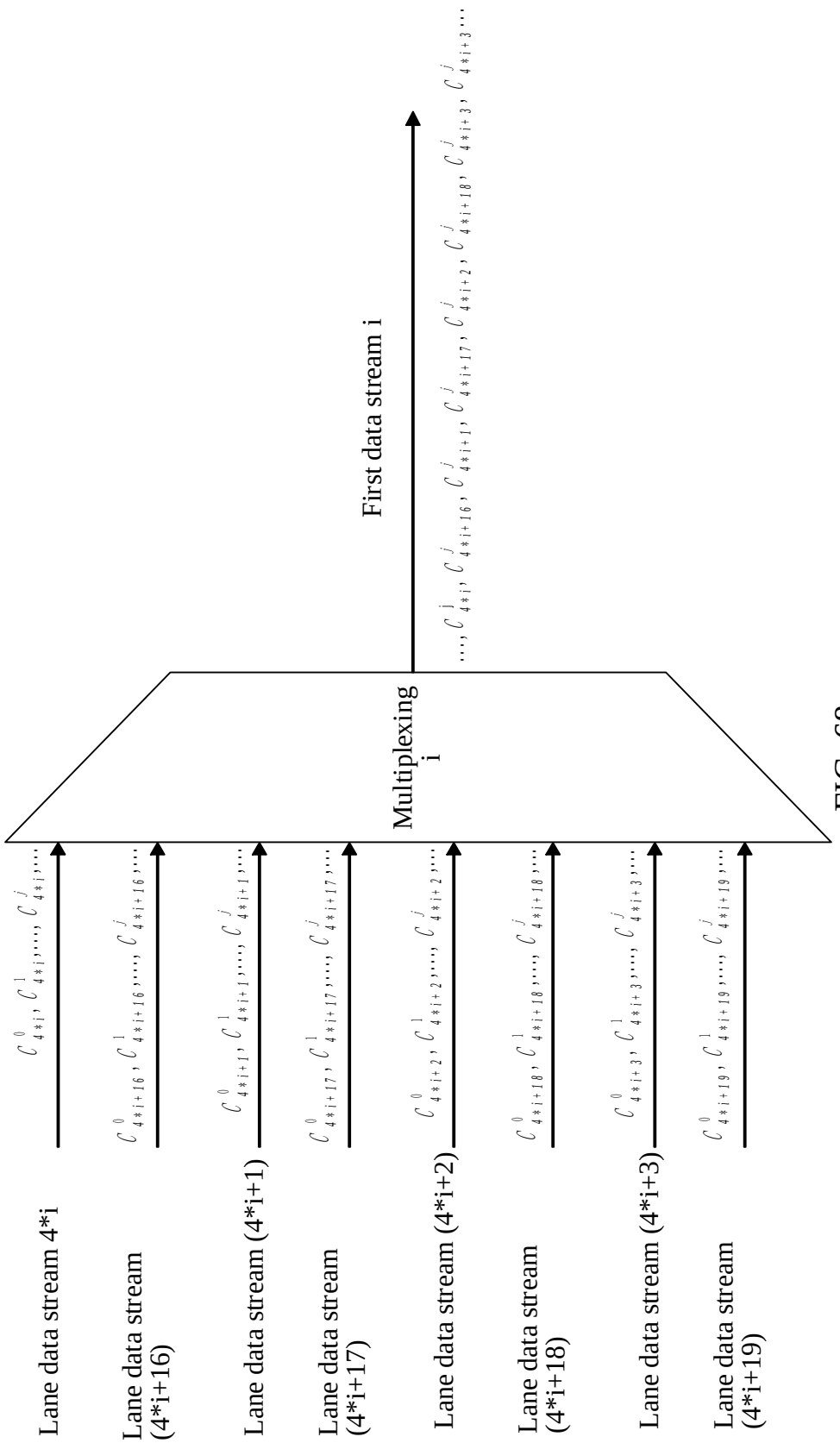

Lane data stream 4*i
Lane data stream (4*i+16)
Lane data stream (4*i+1)
Lane data stream (4*i+17)
Lane data stream (4*i+2)
Lane data stream (4*i+18)
Lane data stream (4*i+3)
Lane data stream (4*i+19)
Multiplexing i
First data stream i

FIG. 68

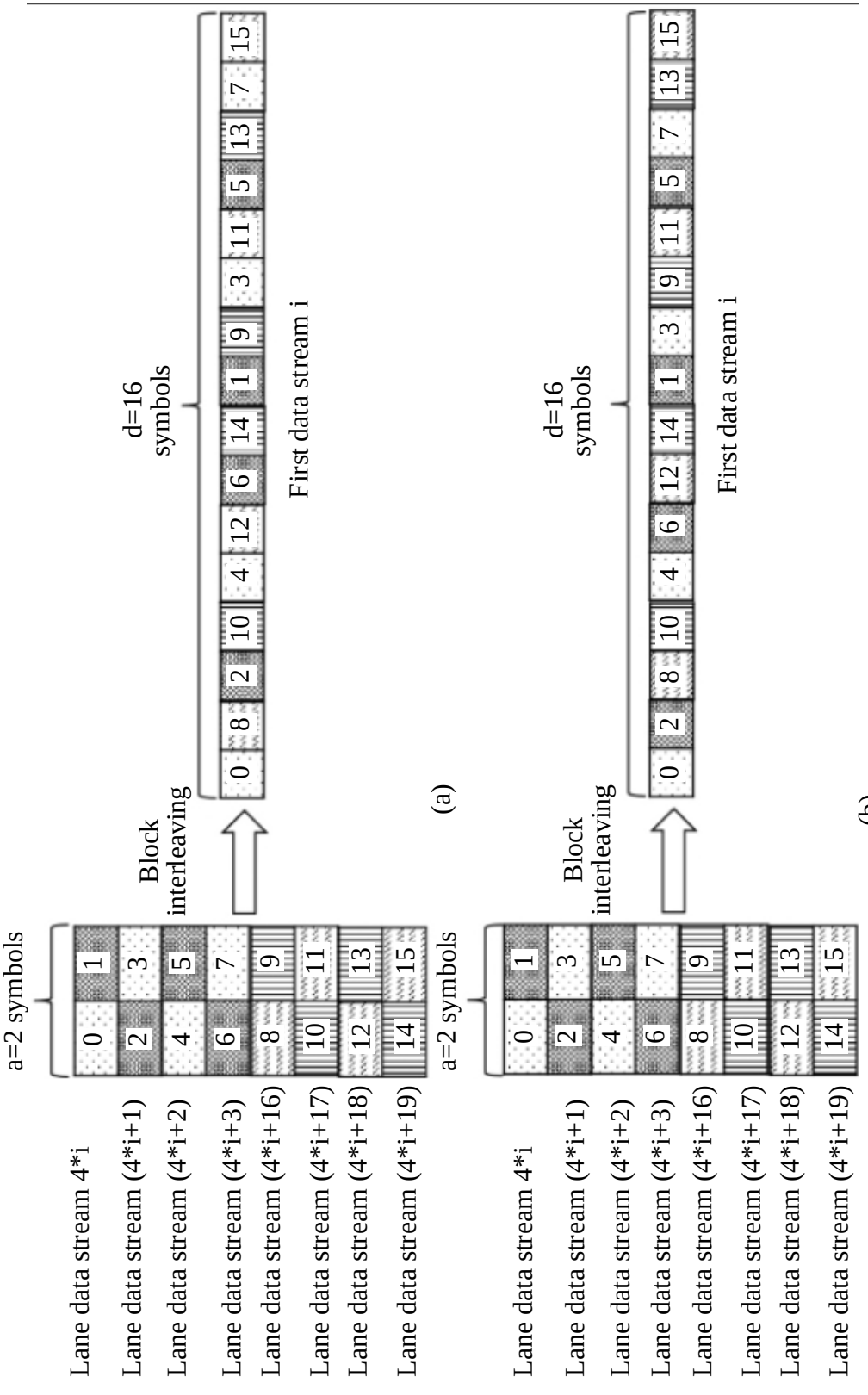

a=2 symbols
Lane data stream 4*i
Lane data stream (4*i+1)
Lane data stream (4*i+2)
Lane data stream (4*i+3)
Lane data stream (4*i+16)
Lane data stream (4*i+17)
Lane data stream (4*i+18)
Lane data stream (4*i+19)
Block interleaving
d=16 symbols
First data stream i
(a)
(b)

FIG. 69

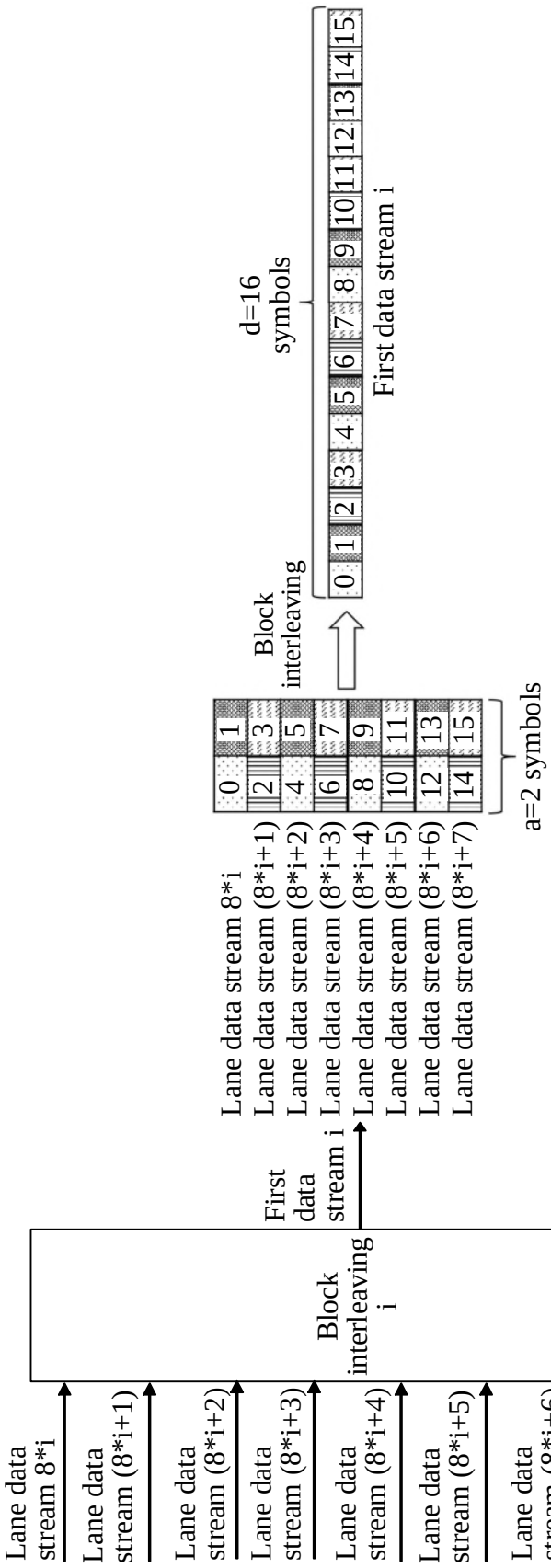

Lane data stream 8*i
Lane data stream (8*i+1)
Lane data stream (8*i+2)
Lane data stream (8*i+3)
Lane data stream (8*i+4)
Lane data stream (8*i+5)
Lane data stream (8*i+6)
Lane data stream (8*i+7)
Block interleaving i
First data stream i
Lane data stream 8*i
Lane data stream (8*i+1)
Lane data stream (8*i+2)
Lane data stream (8*i+3)
Lane data stream (8*i+4)
Lane data stream (8*i+5)
Lane data stream (8*i+6)
Lane data stream (8*i+7)
a=2 symbols
Block interleaving
d=16 symbols
First data stream i

FIG. 70

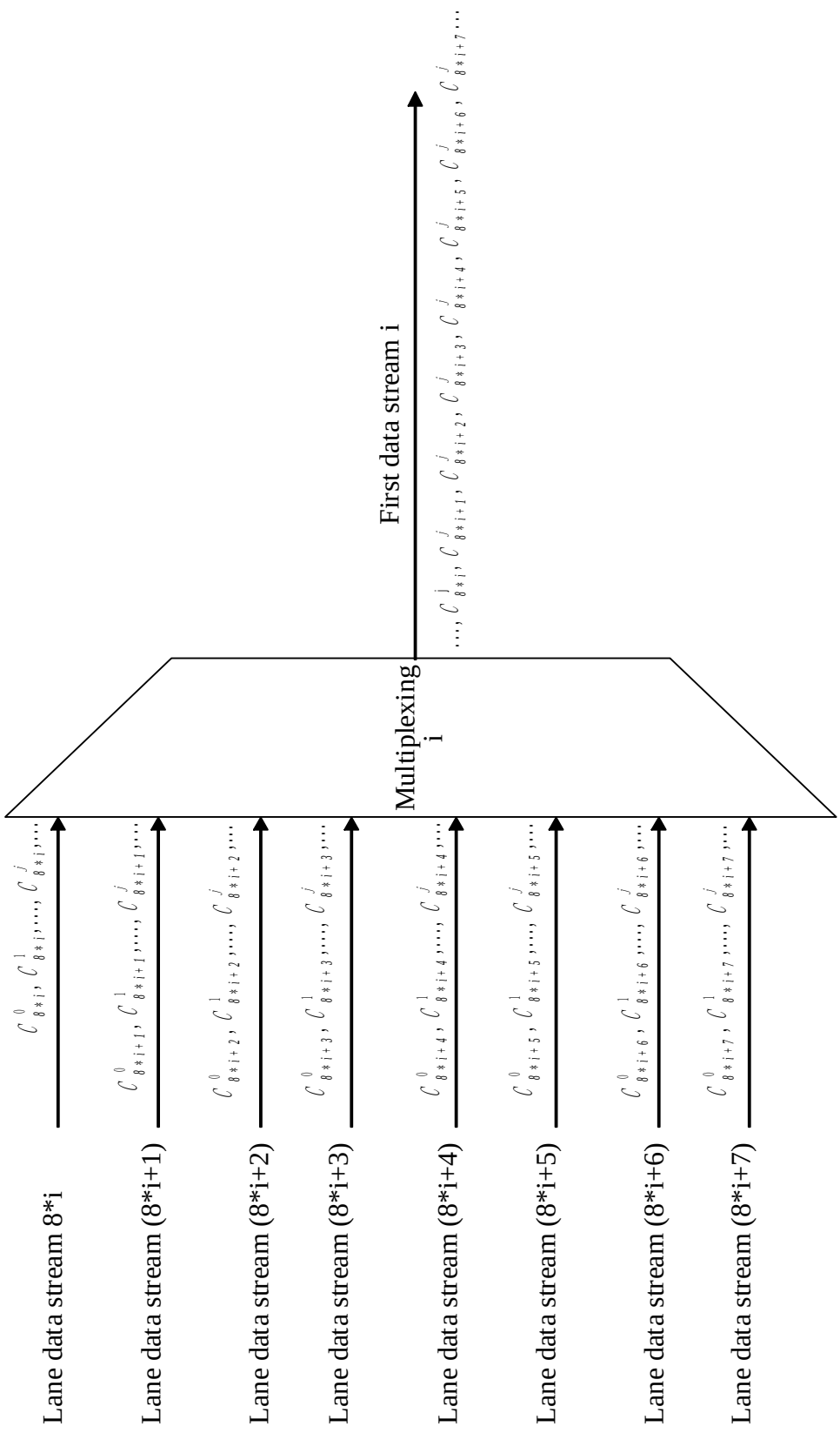

Lane data stream 8*i
Lane data stream (8*i+1)
Lane data stream (8*i+2)
Lane data stream (8*i+3)
Lane data stream (8*i+4)
Lane data stream (8*i+5)
Lane data stream (8*i+6)
Lane data stream (8*i+7)
Multiplexing
i
First data stream i

FIG. 71

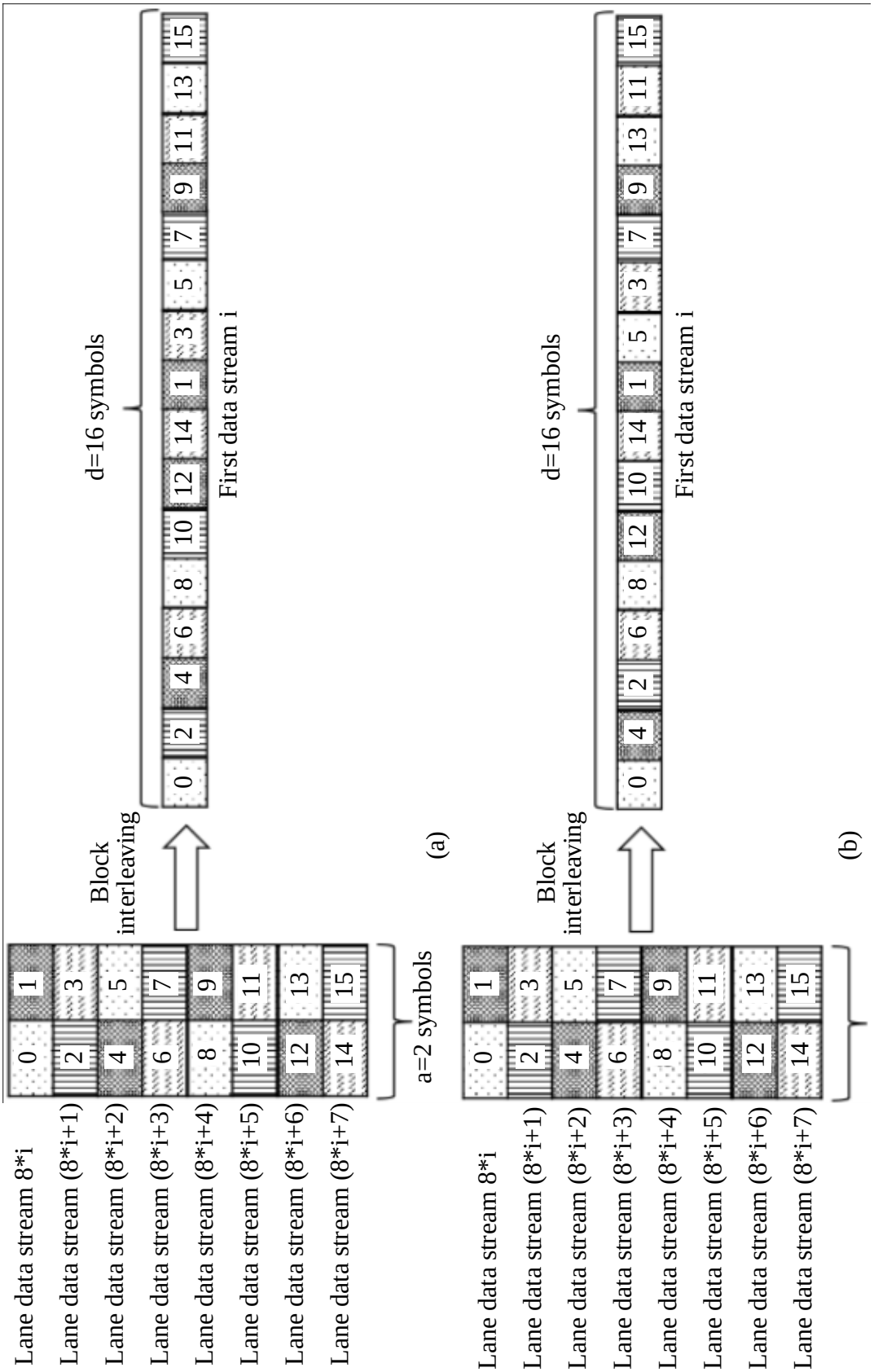

Lane data stream 8*i
Lane data stream (8*i+1)
Lane data stream (8*i+2)
Lane data stream (8*i+3)
Lane data stream (8*i+4)
Lane data stream (8*i+5)
Lane data stream (8*i+6)
Lane data stream (8*i+7)
a=2 symbols
Block interleaving
d=16 symbols
First data stream i
(a)
(b)

FIG. 72

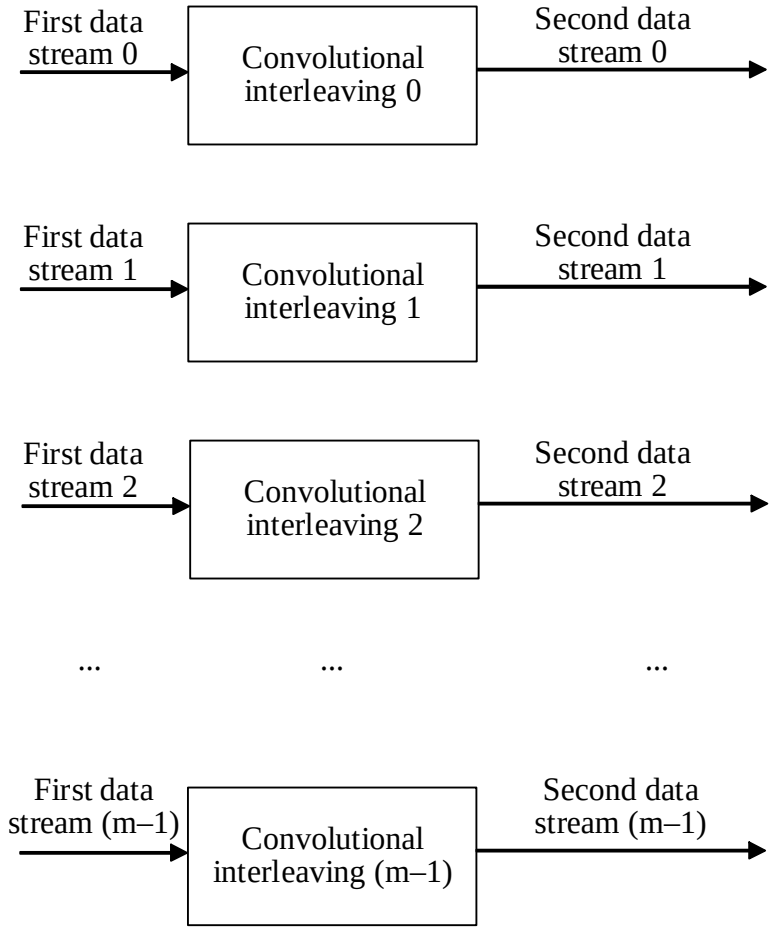

First data stream 0
Convolutional interleaving 0
Second data stream 0
First data stream 1
Convolutional interleaving 1
Second data stream 1
First data stream 2
Convolutional interleaving 2
Second data stream 2
...
...
...
First data stream (m–1)
Convolutional interleaving (m–1)
Second data stream (m–1)

FIG. 73

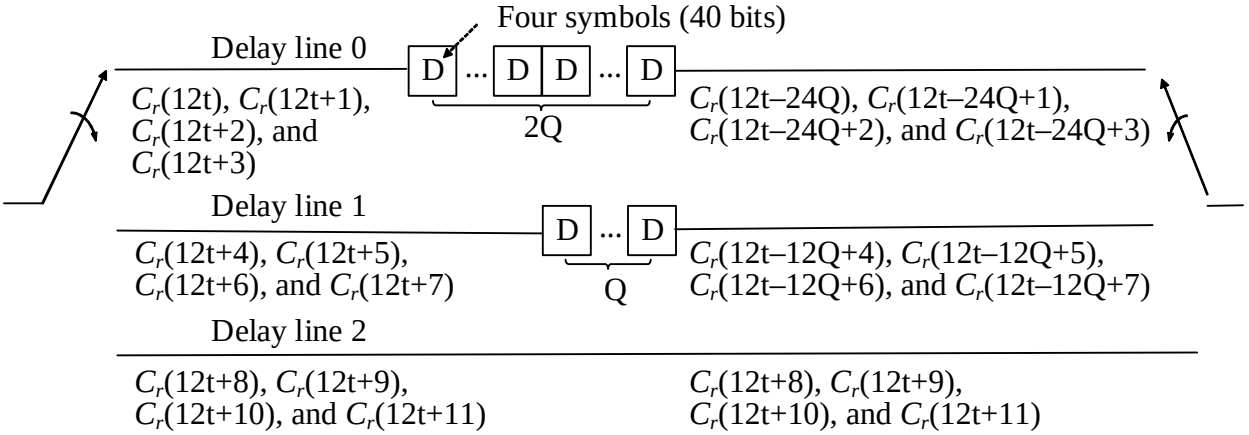

Four symbols (40 bits)
Delay line 0
D ... D D ... D
2Q
$C_r(12t)$, $C_r(12t+1)$, $C_r(12t+2)$, and $C_r(12t+3)$
$C_r(12t–24Q)$, $C_r(12t–24Q+1)$, $C_r(12t–24Q+2)$, and $C_r(12t–24Q+3)$
Delay line 1
D ... D
Q
$C_r(12t+4)$, $C_r(12t+5)$, $C_r(12t+6)$, and $C_r(12t+7)$
$C_r(12t–12Q+4)$, $C_r(12t–12Q+5)$, $C_r(12t–12Q+6)$, and $C_r(12t–12Q+7)$
Delay line 2
$C_r(12t+8)$, $C_r(12t+9)$, $C_r(12t+10)$, and $C_r(12t+11)$
$C_r(12t+8)$, $C_r(12t+9)$, $C_r(12t+10)$, and $C_r(12t+11)$

FIG. 74

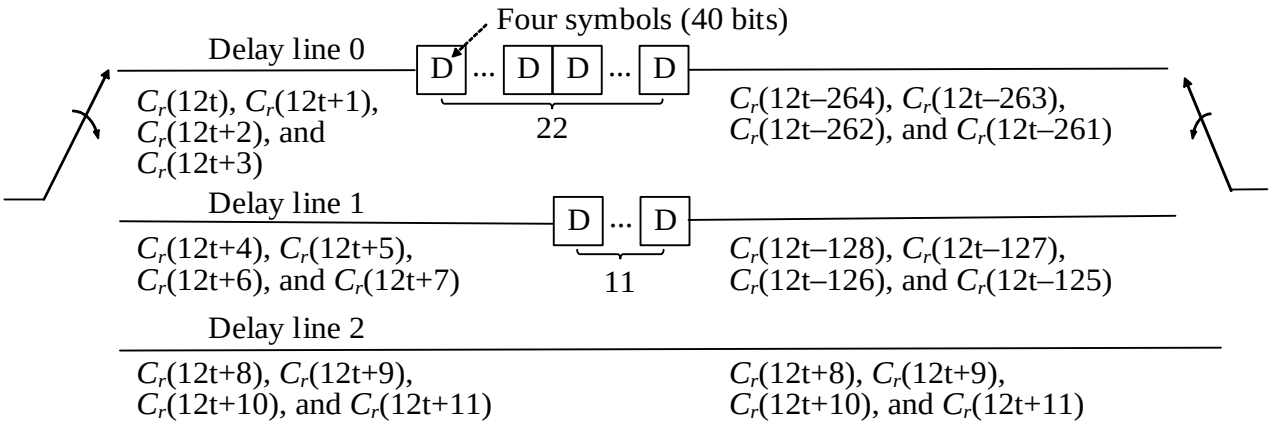


FIG. 75

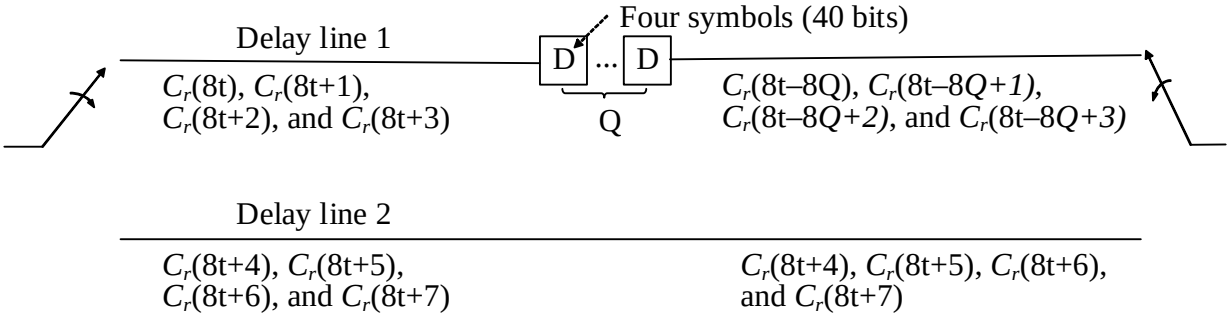


FIG. 76

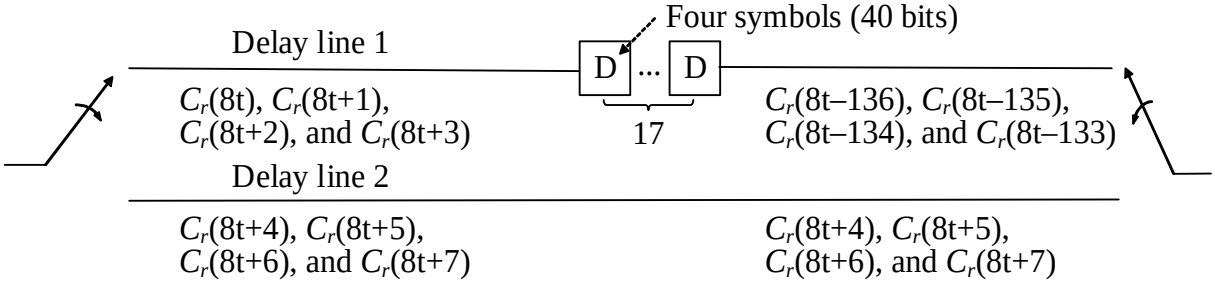


FIG. 77

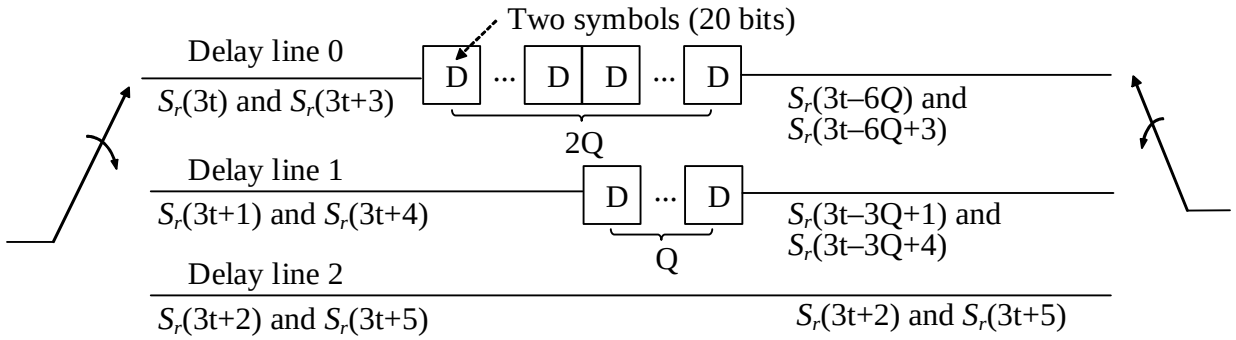


FIG. 78

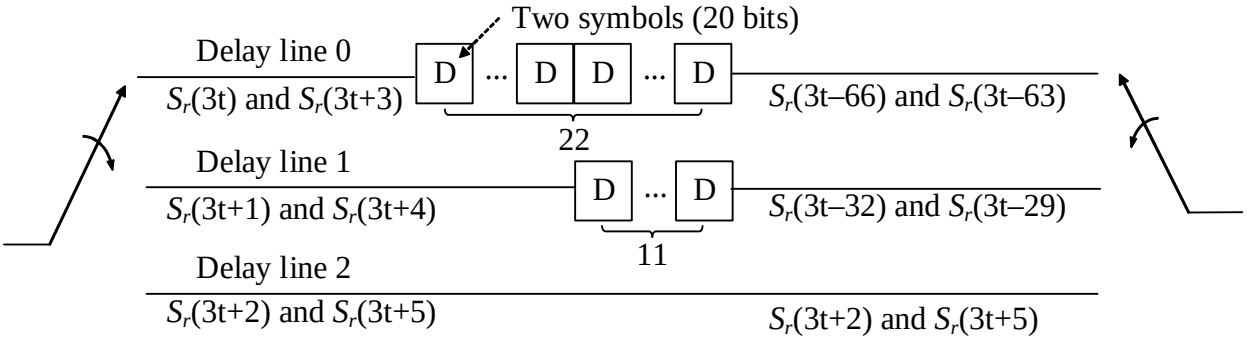


FIG. 79

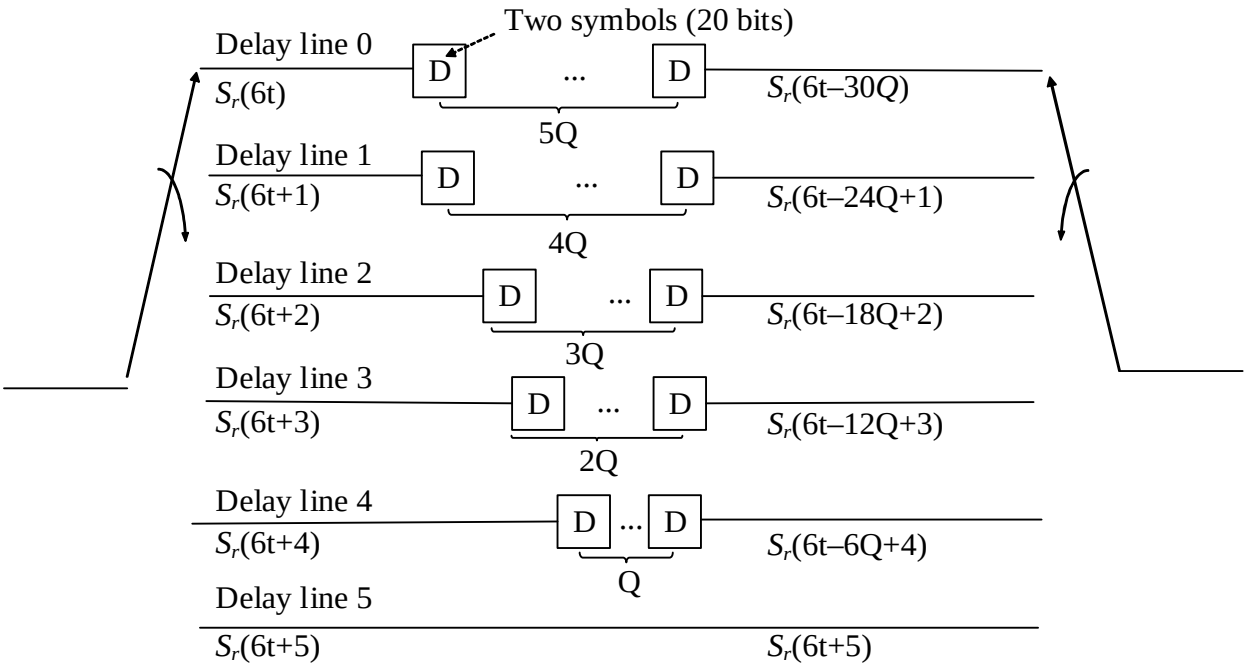


FIG. 80

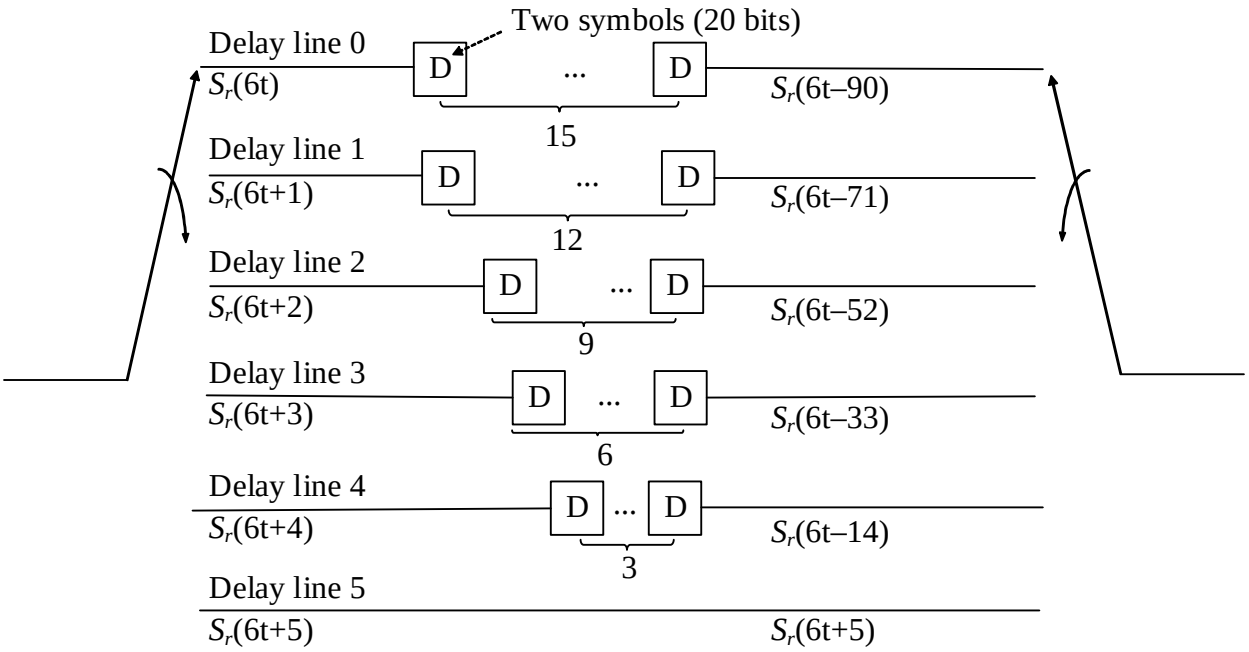


FIG. 81

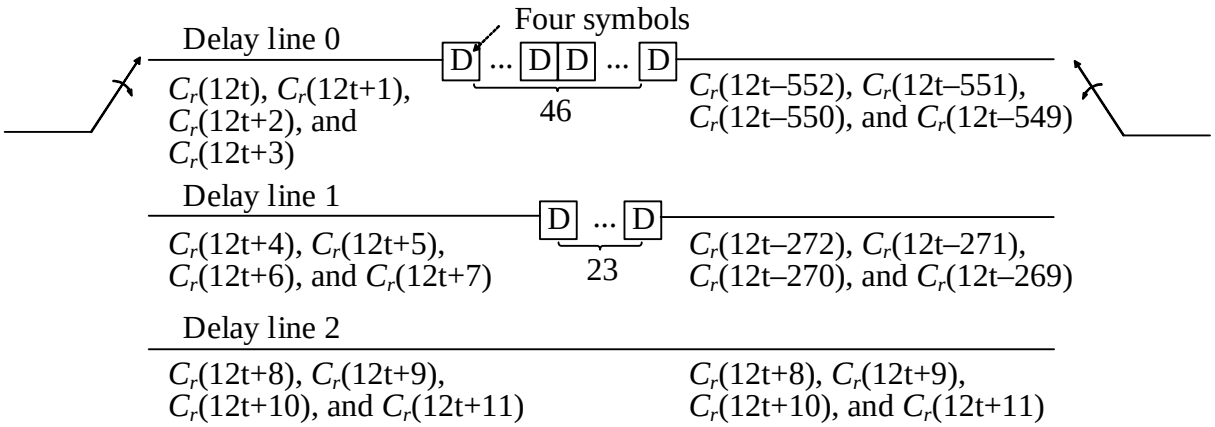


FIG. 82

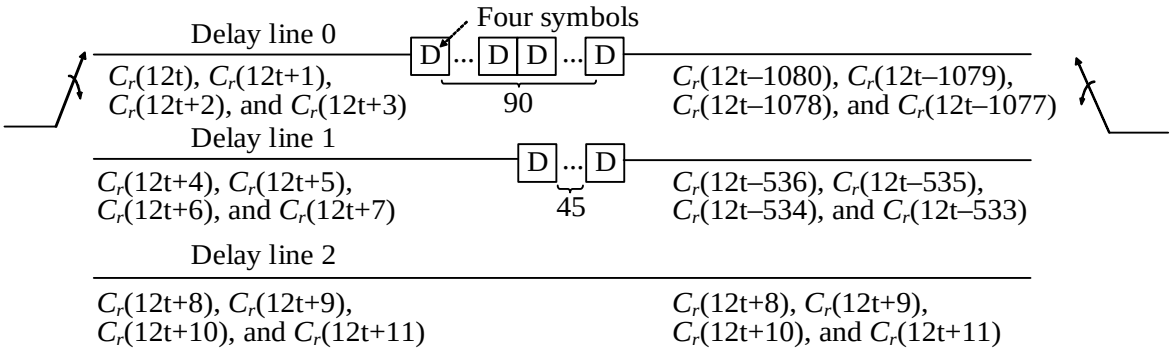


FIG. 83

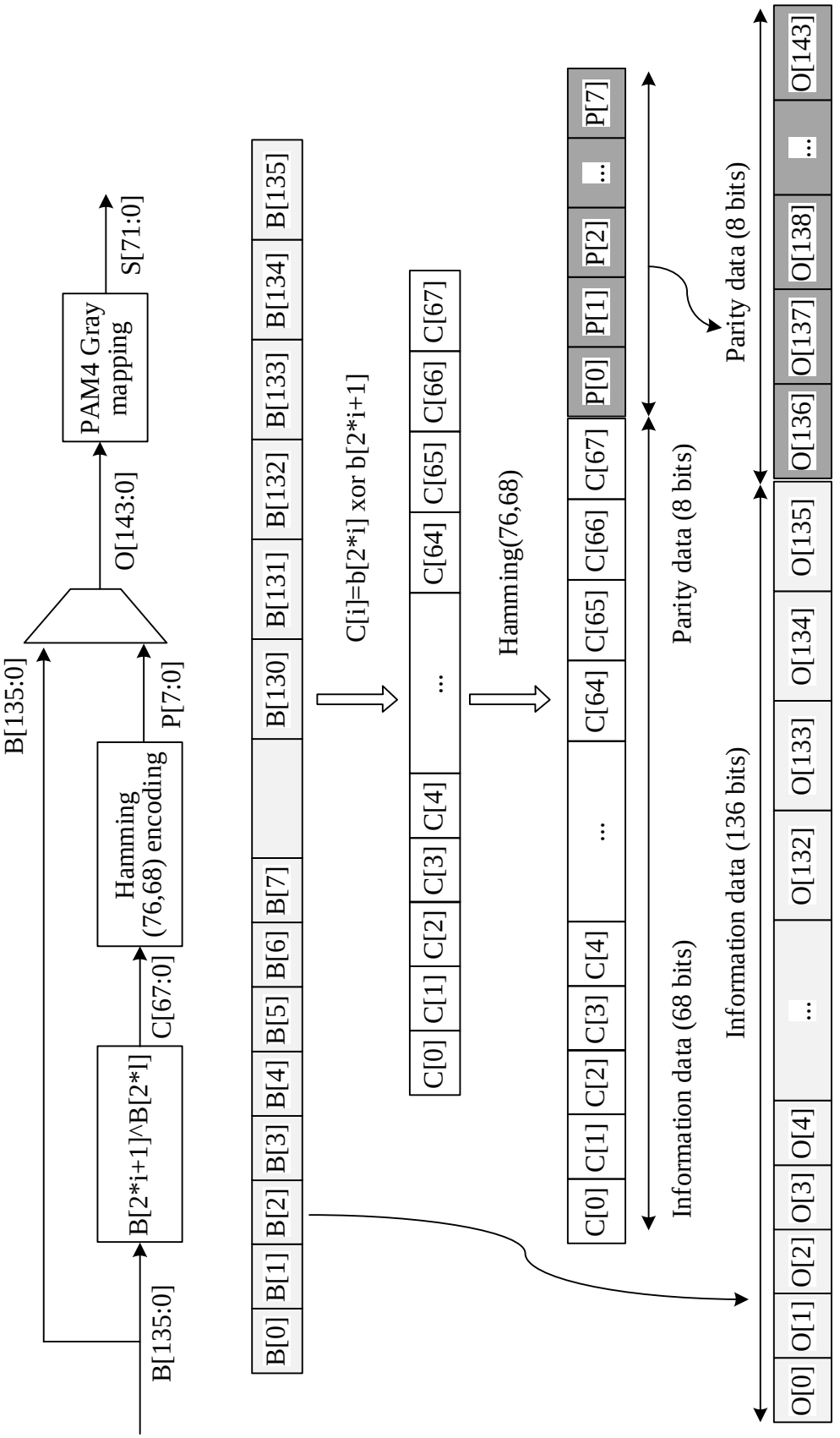

B[135:0]
B[2*i+1]^B[2*I]
C[67:0]
Hamming (76,68) encoding
P[7:0]
B[135:0]
O[143:0]
PAM4 Gray mapping
S[71:0]
B[0] B[1] B[2] B[3] B[4] B[5] B[6] B[7] ... B[130] B[131] B[132] B[133] B[134] B[135]
C[i]=b[2*i] xor b[2*i+1]
C[0] C[1] C[2] C[3] C[4] ... C[64] C[65] C[66] C[67]
Hamming(76,68)
C[0] C[1] C[2] C[3] C[4] ... C[64] C[65] C[66] C[67] P[0] P[1] P[2] ... P[7]
Information data (68 bits)
Parity data (8 bits)
Information data (136 bits)
Parity data (8 bits)
O[0] O[1] O[2] O[3] O[4] ... O[132] O[133] O[134] O[135] O[136] O[137] O[138] ... O[143]

FIG. 84

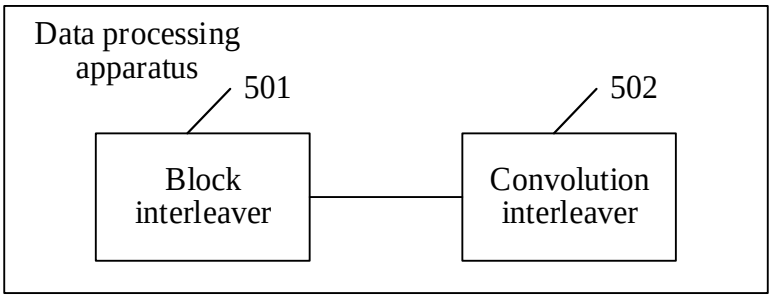


FIG. 85

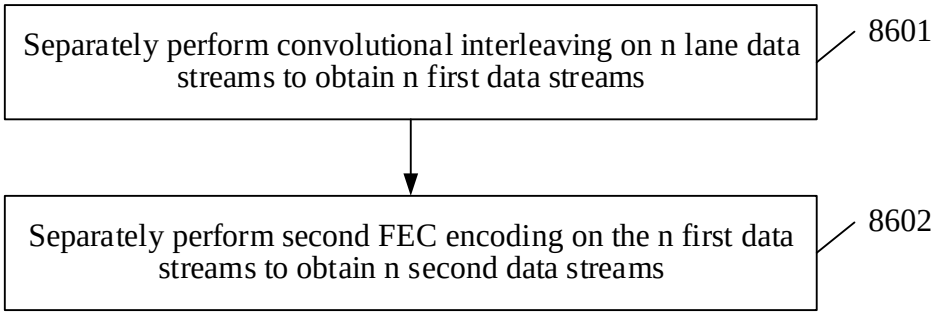


FIG. 86

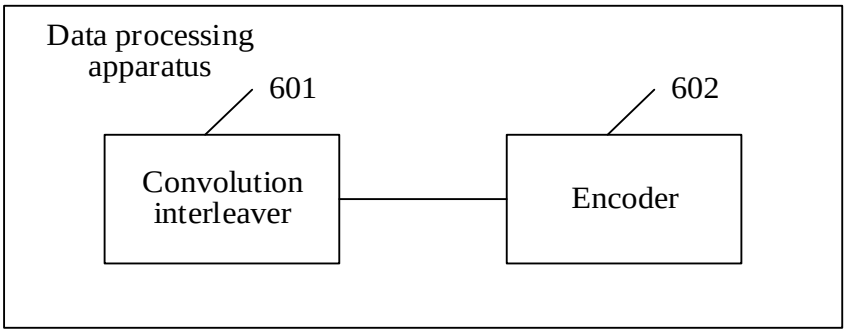


FIG. 87

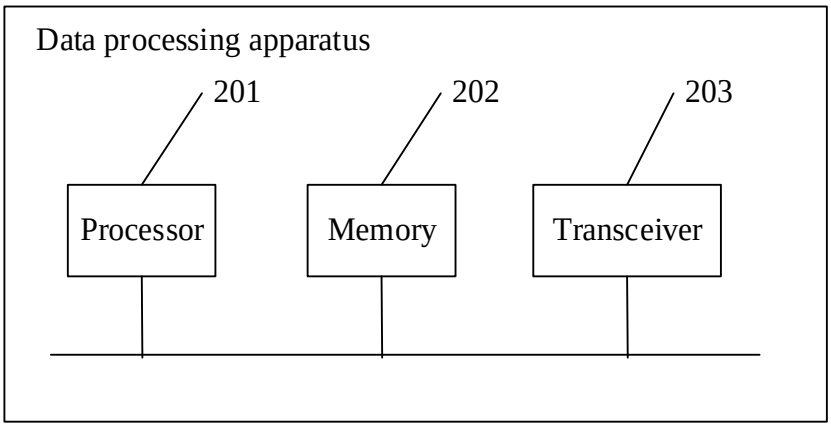


FIG. 88