

ABSTRACT

A semiconductor memory device includes active regions including first impurity regions and second impurity regions, word lines on the active regions and extended in a first direction, bit lines on the word lines and extended in a second direction crossing the first direction, the bit lines being connected to the first impurity regions, first contact plugs between the bit lines, the first contact plugs being connected to the second impurity regions, landing pads on the first contact plugs, respectively, and gap-fill structures filling spaces between the landing pads, top surfaces of the gap-fill structures being higher than top surfaces of the landing pads.

FIG. 2