

WHAT IS CLAIMED IS:—**CLAIMS**

1. An apparatus (200) configured for bit packing data having various bit widths in a computer system, the apparatus comprising:

a first plurality of bit locations (202) in the computer system, each bit location of the first plurality of bit locations each having comprising a register (304) with a predetermined number of bit slots (206) and temporarily storing one or more bits in respective slots each bit slot of the predetermined number of bit slots configured to temporarily store a respective bit of a predetermined number of bits of data, the predetermined number of bits corresponding to one of a number of different data bit widths; and

a fixed bit packing network (208) configured to pack ~~data~~ the predetermined number of bits of a number of different bit widths from the first plurality of bit locations (202) to a second plurality of bit locations (210) in the computer system, wherein the fixed bit packing network is configured to pack the predetermined number of bits by routing all bits of the predetermined number of bits stored in a same particular bit slot position (320) in the predetermined number of bit slots within each respective bit locations location of the first plurality of bit locations by routing the bits into (202) to bit slots (322) of a register (306) of a same particular bit location in of the second plurality of bit locations (210) to form bit bundles (328) in respective ones of the second plurality of bit locations- (210),

wherein the fixed bit packing network (208) includes fixed point-to-point connections between the bit slots in the first plurality of bit locations (202) and the bit slots in the second plurality of bit locations (210), and is configured to

accommodate each of the number of different data bit widths input to the first plurality of bit locations, and

pack data from the first plurality of bit locations into the second plurality of bit locations.

2. The apparatus (200) of claim 1, further comprising:

the second plurality of bit locations (202) contained within a memory device, wherein the memory device is further configured to store the bit bundles- (328).

3. The apparatus (200) of claim 2, wherein the second plurality of bit locations (210) comprises a plurality of memory cells in the memory device.

4. The apparatus (200) of claim 3, wherein the number of bits in a bit bundle (328) corresponds to a memory data word size of the memory device.

5. The apparatus (200) of claim 1, wherein the fixed bit packing network ~~includes fixed point-to-point connections between bit slots in the first plurality of bit locations and bit slots in the second plurality of bit locations.~~

6. ~~The apparatus of claim 1, wherein fixed bit packing network~~(208) comprises a portion of one of a computation datapath network or a memory datapath.

76. The apparatus (200) of claim 1, wherein the bits in the first plurality of bit locations (202) are generated by a single-instruction, multiple data-(SIMD)₂ unit having a number of lanes.

87. The apparatus (200) of claim 76, wherein ~~the size of each bit bundle (328) has a size that~~ is a multiple of the number of lanes of the SIMD unit.

98. The apparatus (200) of claim 1, wherein the apparatus is further operable for an unpacking operation wherein bit bundles (328) in the plurality of second bit locations (210) are unpacked to the plurality of first bit locations by reverse operation of the fixed bit packing network~~;~~ (208).

109. A method (700) of operating a computational circuitry, comprising:

storing (702) one or more bits in at least one of a first plurality of bit locations ~~each having~~(202), each bit location of the first plurality of bit locations comprising a register (304) with a predetermined number of bit slots (206) and each bit slot of the predetermined number of bit slots configured to temporarily store the one or more bits in a respective slots~~bit of the a predetermined number of bit slots~~bits of data, the predetermined number of bits corresponding to one of a number of different data bit widths; and

packing (704) bits to a second plurality of bit locations~~;~~ (210), the packing utilizing a fixed bit packing network (208) configured to pack ~~data bits of a the predetermined~~ number of ~~different bit widths~~ bits from the first plurality of bit locations (202) to the second plurality of bit locations~~;~~ (210), wherein the fixed bit packing network (208) is configured to transmit-pack

the predetermined number of bits by routing all bits of the predetermined number of bits stored in a same particular bit slot positionsposition (320) in the predetermined number of bit slots within each respective bit locationslocation of the first plurality of bit locations into(202) to bit slots of a same particular register (306) of a bit location inof the second plurality of bit locations (210) to form bit bundles (328) in respective ones of the second plurality of bit locations- (210), wherein the fixed bit packing network (208) includes fixed point-to-point connections between the bit slots in the first plurality of bit locations (202) and the bit slots in the second plurality of bit locations (210), and is configured to

accommodate each of the number of different data bit widths input to the first plurality of bit locations, and

pack data from the first plurality of bit locations into the second plurality of bit locations.

~~1410.~~ The method (700) of claim ~~109~~, further comprising:

storing the bit bundles (328) in a memory device, wherein the second plurality of bit locations are contained within a memory device, and ~~wherein the memory device is further configured to store the bit bundles.~~

~~14211.~~ The method (700) of claim ~~1410~~, wherein the number of bits in a bit bundle corresponds to a memory data word size of the memory device.

~~14312.~~ The method (700) of claim ~~109~~, wherein the fixed bit packing network ~~includes fixed point-to-point connections between bit slots in the first plurality of bit locations and a bit slots in the second plurality of bit locations.~~

~~14.~~ ~~The method of claim 10, wherein fixed bit packing network(208) comprises a portion of one of a computation datapath network or a memory datapath.~~

~~14513.~~ The method (700) of claim ~~109~~, wherein the predetermined number of bits of the data in the first plurality of bit locations are received from a SIMD unit having a number of lanes.

~~14614.~~ The method (700) of claim ~~14513~~, wherein ~~the size of~~ each bit bundle has a size that is a multiple of the number of lanes of the SIMD unit.

1715. The method (700) of claim 109, further comprising executing an unpacking operation wherein bit bundles in the plurality of second bit locations are unpacked to the plurality of first bit locations by reverse operation of the fixed bit packing network.

~~18. An apparatus configured for bit packing data having various bit widths in a computer system, the apparatus comprising:~~

~~—— means for storing one or more bits in at least one of a first plurality of bit locations each having a predetermined number of bit slots in the bit locations and configured to temporarily store the one or more bits in respective slots of the predetermined number of bit slots, the predetermined number of bits corresponding to one of a number of different data bit widths; and~~

~~—— means for packing bits to a second plurality of bit locations, the packing utilizing a fixed bit packing network configured to pack data bits of a number of different bit widths from the first plurality of bit locations to the second plurality of bit locations, wherein the network is configured to route bits stored in a bit slot positions in respective bit locations of the first plurality of bit locations into bit slots of a same bit location in the second plurality of bit locations to form bit bundles in respective ones of the second plurality of bit locations.~~

~~19. The apparatus of claim 18, further comprising:~~

~~—— a memory device, wherein the apparatus is further configured to store the bit bundles into the memory device including the second plurality of bit locations that is holding a bit bundle.~~

~~20. The apparatus of claim 19, wherein the second plurality of bit locations comprises a plurality of memory cells in the memory device.~~

~~21. The apparatus of claim 20, wherein the number of bits in a bit bundle corresponds to a memory data word size of the memory device.~~

~~22. The apparatus of claim 18, wherein the fixed bit packing network includes fixed point-to-point connections between bit slots in the first plurality of bit locations and a bit slots in the second plurality of bit locations.~~

23. — ~~The apparatus of claim 18, wherein fixed bit packing network comprises a portion of one of a computation datapath network or a memory datapath.~~

24. — ~~The apparatus of claim 18, wherein the bits in the first plurality of bit locations are received from a SIMD unit having a number of lanes.~~

25. — ~~The apparatus of claim 24, wherein the size of each bit bundle is a multiple of the number of lanes of the SIMD unit.~~

26. — ~~The apparatus of claim 18, wherein the apparatus is further operable for an unpacking operation wherein bit bundles in the plurality of second bit locations are unpacked to the plurality of first bit locations by reverse operation of the fixed bit packing network.~~

27. — ~~An apparatus for bit packing in a computer system, the apparatus comprising:~~

— ~~processing circuitry configured for:~~

— ~~storing one or more bits in at least one of a first plurality of bit locations each having a predetermined number of bit slots in the bit locations and configured to temporarily store the one or more bits in respective slots of the predetermined number of bit slots, the predetermined number of bits corresponding to one of a number of different data bit widths; and~~

— ~~packing bits to a second plurality of bit locations, the packing utilizing a fixed bit packing network configured to pack data bits of a number of different bit widths from the first plurality of bit locations to the second plurality of bit locations, wherein the network is configured to transmit bits stored in a bit slot positions in respective bit locations of the first plurality of bit locations into bit slots of a same bit location in the second plurality of bit locations to form bit bundles in respective ones of the second plurality of bit locations.~~

28. — ~~The apparatus of claim 27, further comprising:~~

— ~~a memory device, wherein the apparatus is further configured to store the bit bundles into the memory device including the second plurality of bit locations that is holding a bit bundle.~~

29. — ~~The apparatus of claim 28, wherein the second plurality of bit locations comprises a plurality of memory cells in the memory device.~~

30. — ~~The apparatus of claim 29, wherein the number of bits in a bit bundle corresponds to a memory data word size of the memory device.~~

31. — ~~The apparatus of claim 27, wherein the fixed bit packing network includes fixed point-to-point connections between bit slots in the first plurality of bit locations and a bit slots in the second plurality of bit locations.~~

32. — ~~The apparatus of claim 27, wherein fixed bit packing network comprises a portion of one of a computation datapath network or a memory datapath.~~

33. — ~~The apparatus of claim 27, wherein the bits in the first plurality of bit locations are received from a SIMD unit having a number of lanes.~~

34. — ~~The apparatus of claim 33, wherein the size of each bit bundle is a multiple of the number of lanes of the SIMD unit.~~

35. — ~~The apparatus of claim 27, wherein the apparatus is further operable for an unpacking operation wherein bit bundles in the plurality of second bit locations are unpacked to the plurality of first bit locations by reverse operation of the fixed bit packing network.~~