Method for Forming Variable-K Gate Dielectric

Abstract

A method for forming a gate dielectric having regions with different dielectric constants. A low-K dielectric layer is formed over a semiconductor structure. A dummy dielectric layer is formed over the low-K dielectric layer. The dummy dielectric layer and low-K dielectric layer are patterned to form an opening. The dummy dielectric layer is isontropically etched selectively to the low-K dielectric layer to form a stepped gate opening. A high-K dielectric layer is formed over the dummy dielectric and in the stepped gate opening. A gate electrode is formed on the high-K dielectric layer.

Fig. 6

162162

G00001