

**METHOD FOR PRODUCING A MICROELECTRONIC DEVICE ON FD-SOI
SUBSTRATE, CORRESPONDING DEVICE AND INTEGRATED CIRCUIT
INCORPORATING SAME**

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Technical field

[001] The invention relates to the microelectronics industry, or semiconductor industry, and concerns the fabrication of a microelectronic structure on an SOI (Silicon-On-Insulator) substrate. The invention also concerns the microelectronic structure obtained by such a fabrication method.

[002] The invention is applicable notably to the fabrication of integrated semiconductor devices, such as microelectromechanical systems (MEMS) or nanoelectromechanical systems (NEMS), or microelectronic or optoelectronic devices such as image sensors (or imagers) in CMOS (Complementary Metal-Oxide-Semiconductor) technology, or any other microelectronic device produced using this technology.

Prior art

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[003] Since the 1950s, the microelectronics industry has been on a quest for miniaturization of microelectronic devices, the basic element of which is the field-effect transistor and in particular the MOS (Metal-Oxide-Semiconductor) transistor, notably in CMOS (Complementary Metal-Oxide-Semiconductor) technology, which is used as an element for switching between two different electrical states corresponding to two opposite logic states (1 or 0 in binary logic). The miniaturization of MOS transistors has brought with it better control over their electrical properties and notably the amount of current flowing per unit time through the conduction channel of these transistors, on which their switching speed depends.

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[004] However the speed of the current is primarily determined by the material it passes through. Since microelectronic chip manufacturers are more or less limited to the use of silicon (Si) substrates, they have concentrated their efforts on increasing the switching speed

by reducing the size of the transistors, for example MOS transistors, notably in CMOS technology.

[005] In this regard, silicon-on-insulator substrates or SOI substrates are widely used these
5 days for the fabrication of transistor-based microelectronic devices. However, after several decades of advances in technological methods, the industry is finding it more and more difficult to reduce the size of transistors any further.

[006] For this reason, the technique developed some 20 years ago by the laboratory of the
10 Commissariat à l’Energie Atomique et aux Energies Alternatives (C.E.A.), Leti, and its partners, known as FD-SOI (Fully-Depleted Silicon-On-Insulator), proposed a new ultra-thin MOS transistor architecture, with a channel which can thus be fully depleted (FD), in other words devoid of dopants. FD-SOI made it possible to meet the challenges posed by miniaturization while combining high performance and low energy consumption, notably
15 in integrated circuits for millimetre wave and radiofrequency wave (RF) analogue applications up to 100 GHz, for example for 5G telephony. FD-SOI technology in fact makes it possible to attain technological nodes at or below 10 nm, even 7 nm.

[007] FD-SOI technology differs from conventional SOI structures which are thicker, such
20 as conventional MOS transistor technology in which the channel is formed in a bulk silicon substrate, and FinFET (Fin Field-Effect Transistor) technology offered by Intel®, in which a fin field-effect transistor, which is a non-planar or 3D transistor, is constructed on a bulk substrate wherein the gate is placed on two, three or four sides of the channel, forming a multi-gate structure. Compared to these technologies, FD-SOI technology makes it possible
25 to increase the current flow speed because the components are fashioned not from bulk silicon but from an ultra-thin silicon layer placed on a thin insulating oxide layer itself placed on the silicon substrate which no longer needs to be doped. Thus, the transistors produced on an SOI substrate, which are planar transistors and therefore easier to produce than FinFET transistors, are less sensitive to current leakage between the source and their
30 drain, on the one hand, and the silicon of the carrier substrate on the other hand, which increases the speed at which they switch without it being necessary to make them any smaller.

[008] However, it is also known that the current flow speed also depends on the crystalline structure of the silicon. This is why SOI substrates currently tend towards the use of strained silicon for the production of active zones of microelectronic devices such as the channel in transistors in CMOS technology. The use of strained silicon or sSi is currently one of the most important factors in the acceleration of CMOS on silicon technology. To be specific, the improvement in the mobility of the electrical charge carriers which is obtained through the application of an appropriate stress to the structure of the crystal lattice makes it possible to increase the speed of these charge carriers in the channel of the MOS transistor, which results in a higher current for a fixed supply voltage and fixed gate oxide thickness.

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[009] In practice, strained silicon (sSi) is a layer of silicon in which the silicon atoms are stretched (tension) or compressed (compression) beyond their normal interatomic distance. A layer of strained silicon under tension may be obtained by placing a thin layer of silicon on a silicon-germanium (SiGe) substrate. When the atoms of the silicon layer are aligned on the atoms of the underlying silicon-germanium layer (which are spaced a little further apart from one another, compared to those of a bulk silicon crystal), the bonds between the silicon atoms are stretched, giving rise to a deformed lattice of silicon atoms. This improves the mobility of these charge carriers, which results in better performance of the chip and lower energy consumption. Electrons can thus move 70% more quickly, which means that sSi NMOS transistors can have a switching speed increased by 35%.

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[010] FD-SOI technology and the use of sSi may be combined, in order to pool the respective advantages of these two major technological advances. This consists in bonding a strained silicon (sSi) film on top of a very thin buried oxide (BOX) layer formed on a non-doped silicon carrier. The bonding of a strained silicon film (sSi) on such a substrate is described, for example, in prior art documents EP 1923912 A1 and US 5691231 A.

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[011] The thinness of the buried oxide (BOX) layer under the strained silicon (sSi) film gives rise to bonding problems when the thin film is continuous (in other words has no patterns). This is due notably to the fact that the gaseous hydrogen in the atmosphere in which the bonding operation is carried out must be absorbed by the BOX in order for bonding to take place, and when the BOX is very thin then there is a risk of bonding defects. The solution disclosed in document EP 1923912 A1 for the bonding of a portion of a donor

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wafer comprising the active layer of the microelectronic device on a carrier wafer provides a satisfactory response to the problems of bonding of the sSi film on the BOX.

[012] However it has become apparent that the subsequent creation of etched patterns forming shallow trench isolation (STI) between components produced in respective adjacent positions in the active layer of the microelectronic device in turn gives rise to problems. Shallow trench isolation (STI), also known as box isolation, prevents leakage of electrical current between adjacent components of a microelectronic device which are produced on the same semiconductor substrate as long as said laterally adjacent components are isolated from one another by such an isolation trench. STI technology has generally been used, for many years, in CMOS technologies at 250 nanometres and below.

[013] However, when it is sought to create active zones isolated from one another and each comprising a respective portion of a strained silicon (sSi) film, it has been found that the stress on the sSi tends to relax, in other words to diminish at the edges of the active zones created, where said sSi film is cut. This occurs when etching the patterns intended to be filled with insulator to form the isolation trenches STI, since said etching physically ruptures the sSi film.

[014] Document US20060071274A1 discloses a method for forming a bonded SOI wafer, which comprises a first dielectric layer at the surface and trenches filled with a dielectric extending from the surface towards the inside in the semiconductor. This first wafer is bonded (after being turned over) on a second wafer to form a bonded wafer comprising a bulk substrate, i.e. the substrate of the second wafer, a buried dielectric layer covering the bulk, and a semiconductor-on-insulator (SOI) layer covering the buried dielectric layer, the trenches filled with dielectric extending upwards from the buried dielectric layer in the SOI layer.

[015] Document FR3051595A1 discloses an improvement to a method for fabricating a strained silicon-on-insulator (sSOI) substrate, which consists in transferring at least part of a stress present in a strained silicon-germanium (Si-Ge) layer located at the surface of a receiver substrate, to an initially relaxed single crystal silicon (Si) layer of a donor substrate

which is transferred by bonding to said receiver substrate by means of a dielectric layer intended to form the buried insulator layer of an SOI.

Summary of the invention

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[016] The aim of the invention is to overcome at least some of the prior art disadvantages, and more specifically to propose an alternative to the formation of shallow trench isolation (STI) in accordance with current practice, which prevents relaxation of the stress in the silicon in disjointed portions of a continuous strained silicon film as a result of the formation of said isolation trenches which divide said continuous film into said disjointed portions, in order to maintain the good electrical conductivity properties thereof.

[017] To this end, the invention relates to a method for the fabrication of a microelectronic device, said method comprising:

- 15 - providing a first wafer comprising a carrier substrate;
- forming, on the carrier substrate of the first wafer, first isolation trenches;
- providing a second wafer comprising a donor substrate;
- forming, on the donor substrate of the second wafer, a strained silicon film,
- bonding the second wafer on the first wafer, such that the strained silicon film is located on the first wafer by means of at least one layer of insulating material formed, before bonding, on the first wafer after the formation of the first trenches and/or on the second wafer after the formation of the strained silicon film,
- 20 - removing the donor substrate while keeping the layer of insulating material and the strained silicon film on the first wafer;
- 25 - forming second isolation trenches around and/or along portions of the strained silicon film.

[018] Thus, embodiments of the invention are based on the combination of:

- bonding of a donor wafer comprising a strained silicon film to be transferred onto a carrier wafer having patterns forming isolation trenches (STI); on the one hand, and,
- 30 - additional oxidation of the strained silicon film which is carried out after the transfer of said film onto the carrier wafer, on the other hand,

so as to create other shallow isolation trenches (STI) which join up with the insulation of the STI trenches already present at a deeper level, without cutting through the strained silicon film. Advantageously, the strained silicon film is not cut, to be specific, because it is simply converted locally into silicon dioxide. There is therefore no relaxing of the stress in the silicon in the respective portions of the strained silicon film which are created by forming said isolation trenches.

[019] Some preferred but non-limiting aspects of the method are set out below.

[020] In some embodiments, it may be provided that:

- 10 - the first isolation trenches formed in the carrier substrate of the first wafer are trenches referred to as “shallow trenches”, or STI, the depth of which is greater than approximately 5 nm, or between approximately 5 nm and approximately 300 nm, preferably between approximately 50 nm and approximately 300 nm, and even more preferentially between approximately 70 nm and approximately 300 nm; and/or
- 15 - the second isolation trenches have a depth equal to or greater than the thickness of the strained silicon film, for example between approximately 10 nm and approximately 20 nm, for example of the order of 15 nm.

[021] The insulating material of the first trenches, the insulating material of the second trenches and/or the insulating material of the layer of insulating material may be silicon dioxide (SiO₂).

[022] In some embodiments, the first trenches may be formed in the carrier substrate by etching through a first mask produced beforehand by photolithography in a layer of hard material such as for example a nitride, which covers the carrier substrate provided via an associated layer of insulating material, residues of said first mask and of said associated layer of insulating material being removed from the carrier substrate after the formation of said first trenches.

30 [023] In some embodiments, the method further comprises the formation of third isolation trenches produced through a second mask produced beforehand by photolithography in a layer of hard material such as for example a nitride, which is deposited on top of an associated layer of insulating material itself deposited on the layer of strained silicon after

removal of the donor substrate, residues of said second mask and of said associated layer of insulating material being removed after the formation of said third trenches.

[024] For example, the second isolation trenches join up with the first trenches via the layer
5 of insulating material so as to form an isolation structure around and along the strained silicon film.

[025] The second trenches may be produced by local oxidation of the silicon of the strained silicon film. For example the local oxidation of the silicon of the strained silicon film is
10 thermal oxidation, for example oxidation of LOCOS type.

[026] In some embodiments, the removal of the donor substrate may be carried out by grinding, by selective removal, or by fracture by implantation, for example using the Smart-Cut® method.

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[027] The donor substrate of the second wafer may comprise a layer of silicon-germanium, Si-Ge, adapted to stress the silicon of the strained silicon film.

[028] In some embodiments, it is also possible to create at least one opening through the
20 thickness of one of the second trenches and through the layer of insulating material so as to expose the underlying carrier substrate, in an area of said carrier substrate in which there are no first trenches, and, furthermore, the silicon (Si) of the carrier substrate is grown upwards by epitaxial growth in the opening, at least up to and including the level of the layer of insulating material.

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[029] In some embodiments, at least some of the second isolation trenches may have the same horizontal dimensions as associated first trenches, and are respectively aligned vertically with said associated first trenches.

[030] According to a second aspect of the invention, also proposed is a microelectronic structure obtained by implementing the fabrication method according to the first aspect above, said structure comprising disjointed active zones at the surface of the same carrier substrate, isolated from one another by deep and less deep isolation trenches, each active
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zone having a respective portion of strained silicon film, and said strained silicon film portions resting on the same insulating layer which is itself located above the carrier substrate.

5 [031] The strained silicon may be for example of the fully-depleted silicon-on-insulator type.

[032] The insulating material of the first trenches, the insulating material of the second trenches and/or the insulating material of the layer of insulating material may be silicon
10 dioxide (SiO₂).

[033] The second trenches may have non-vertical sides.

[034] According to a third aspect, there is proposed an integrated circuit comprising the
15 microelectronic structure according to the second aspect above, and further comprising at least one field-effect transistor of MOS type produced in an active zone of said microstructure of which the portion of strained silicon film serves as fully-depleted silicon-on-insulator (FD-SOI) substrate in which the channel of the MOS transistor is produced.

20 **Brief description of the drawings**

[035] Further aspects, aims, advantages and features of the invention will become clearer on reading the following detailed description of preferred embodiments of the invention. This description is provided by way of non-limiting example and refers to the appended
25 drawings, in which:

- Figure 1A to Figure 1C are schematic views, in vertical section, at respective steps of its preparation, of an example of a carrier wafer having shallow isolation trenches (STI) produced, in accordance with embodiments of the invention, before bonding of the donor wafer to said carrier wafer;
- 30 - Figure 2 is a schematic view, in vertical section, of an example of a donor wafer comprising a layer of strained silicon, intended to be transferred by bonding to the carrier wafer of Figure 1C;

- Figure 3A schematically depicts the bonding, to the carrier wafer, of the donor wafer with its layer of strained silicon, after said donor wafer has been turned over vertically;
- Figure 3B is a schematic view showing, in vertical section, the new wafer obtained after the bonding schematically depicted by Figure 3A;
- Figure 4 is a schematic view, in vertical section, of the wafer of Figure 3B after removal of the substrate of (what was) the donor wafer;
- Figure 5 is schematic view, in vertical section, of the wafer of Figure 4 after formation of an oxide isolation layer then a nitride protective passivation layer;
- Figure 6 shows, in vertical section, the wafer of Figure 5 after the formation, through the oxide and nitride layers, of wells exposing the layer of strained silicon which was transferred onto the carrier wafer;
- Figure 7 is a schematic view, in vertical section, of the wafer after filling of the wells of Figure 6 with insulating material so as to form isolation trenches by local oxidation of the strained silicon, which isolation trenches join up with the trenches located at a deeper level already produced in the substrate of the carrier wafer before the transfer of the strained silicon film by bonding of the donor wafer;
- Figure 8 shows the microstructure of Figure 7 after removal of the hard mask of dielectric nitride;
- Figure 9 is a schematic view, in vertical section, of the wafer ultimately obtained after removal of the oxide residues, and planarization;
- Figure 10 is a flow diagram schematically depicting steps of an example of implementation of the method according to the invention; and,
- Figure 11 is a schematic view, in vertical section, of an example of an electronic circuit obtained by the method, after creating openings allowing access to the silicon of the carrier substrate.

Description of detailed embodiments

[036] In the figures and in the remainder of the description, the same reference numerals designate identical or similar elements. Furthermore, the various elements are not shown to scale, for the sake of clarity in the figures. Moreover, the various embodiments and variants described are not mutually exclusive and may be combined with one another.

[037] In the text below, the terms “substantially”, “around” and “of the order of” mean to within 10%, and preferably to within 5%. Moreover, the expression “between ... and ...”, or equivalent expressions, mean that the limits are included, unless expressly stated
5 otherwise.

[038] The expression “formed on the basis of”, used with reference to a material and an element of interest, means that the material is a compound formed of a plurality of elements including at least said element of interest.

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[039] The expression “material mainly comprising” an element of interest means a material in which at least 50% of the volume is made up of, or comprises, said element of interest.

[040] The term "wafer" designates a very thin plate of single crystal semiconductor
15 material, on which microelectronic devices can be produced. Wafers are used in the microelectronics industry as a carrier for the fabrication of microstructures, to fabricate microelectronic devices, before they are integrated in packaging to obtain an integrated circuit. Wafers include a base made of doped semiconductor material, such as silicon (Si), gallium arsenide (GaAs) or indium phosphide (InP). This doped semiconductor material
20 serves as a substrate for the creation of microstructures forming the active microelectronic devices which are used in the composition of integrated circuits, transistors, power semiconductor products, MEMS or NEMS, etc. Such fabrication uses design techniques such as, for example and without limitation: photolithography, doping, etching, deposition of other materials in layers or by diffusion or by any other physical/chemical reaction,
25 polishing, etc. The wafers produced industrially have dimensions generally between 25.4 mm (1" technology) and 300 mm (8" technology), for a thickness of the order of 0.7 mm.

[041] “Layer” means an extent of crystalline material the thickness of which along the axis Z is smaller, for example ten times or even twenty times smaller, than its longitudinal
30 dimensions of width and length in the plane XY.

[042] “Anisotropic etching” means that the speed of etching of the silicon is not the same in all directions during the etching process. On the contrary, only the vertical direction of

the silicon is etched during the etching process, the lateral direction not being etched. Conversely, in “isotropic etching” there is no preferred direction of etching, such that all of the surfaces exposed are etched simultaneously, regardless of their orientation in space, in other words whether they are horizontal, vertical, or inclined.

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[043] Chemical-Mechanical Polishing or CMP is a process for smoothing surfaces using the combined action of mechanical abrasion forces and chemical attack of the surface of a material to be treated using an abrasive polishing suspension or slurry, which has the effect of removing one or more materials at the surface of the wafer and eliminating any
10 topography at the surface, resulting in the planarization of the surface of the wafer exposed to this process. The duration of the CMP process depends on the speed of removal and on the thickness of the material to be removed before an etch stop, if there is one, is reached.

[044] The term "photoresist" designates a material used in photolithography, more
15 particularly a polymer resin, which is sensitive to light and is used to form a pattern on a wafer. This is achieved using an optical mask made up of opaque zones and transparent zones which define the pattern to be reproduced on the wafer, through which the photoresist is illuminated. The photoresist has its properties modified in the transparent zones of the optical filter by virtue of this illumination. Thus, for example, a "positive" photoresist is a
20 light-sensitive polymer which, when exposed to ultraviolet (UV) light, is converted to a soluble material: areas exposed to this illumination can then be dissolved using a solvent, leaving behind (referred to as revelation by those skilled in the art) a layer with recessed patterns which can be used as a mask for the formation of a structure through the mask thus formed. For example, the structure may be formed by etching a pre-existing underlying
25 material which is selective to the material of the mask, or by ion implantation in this underlying material, or by deposition of a new material in the areas exposed by the mask.

[045] Lastly, a direct orthogonal three-dimensional reference frame (X,Y,Z) is defined here and for the remainder of the description, wherein the axes X and Y form a plane parallel
30 to the main plane of the carrier wafer in question, and wherein the axis Z is oriented substantially orthogonally to the main plane of the wafer, this axis Z being oriented in the direction of the axis of gravity. In the remainder of the description, the terms “vertical” and “vertically” are understood to be relative to an orientation substantially parallel to the axis

Z, and the terms “horizontal” and “horizontally” relative to an orientation substantially parallel to the plane (X,Y). Furthermore, the terms “top” and “bottom” together with their derivatives (such as “above” and “below”, or “on top of” and “under”), as well as the terms “lower” and “upper”, used to qualify an element of the microstructure in question, are to be
5 understood to relate to a position increasing when moving away from the wafer upwards, i.e. in the vertical direction +Z.

[046] The term “back” and the term “front”, on the other hand, are used with reference to the side of a wafer via which the various treatments are, or have been, carried out to produce
10 the microstructure in question. As these treatments are systematically carried out from above when the wafer is placed flat in an enclosure used to carry out the treatment, the “front” side is generally (and by default) the top side of the wafer. However, when a wafer or a die cut from a wafer is turned over vertically, its front side becomes the bottom side and its back side becomes the top side. The term “back” assigned to the semiconductor substrate of an
15 individual wafer or die is also used in reference to this convention, in the sense that it refers to the part of the substrate which is furthest from the side of said wafer or said die on which treatments have been carried out on the substrate, and which is always referred to as the back side even when the wafer or die has been turned over vertically.

20 [047] In the description of embodiments of the method below, the microelectronic device of interest is formed on a carrier wafer, from a base carrier wafer and a donor wafer which are assembled by bonding after the donor wafer has been turned over vertically so as to form a new carrier wafer onto which a strained silicon film has been transferred. This wafer is intended for the fabrication of an integrated semiconductor product, for example in CMOS
25 technology, and the aim of the method is the fabrication of the shallow isolation trenches (STI) in a manner compatible with preserving the advantages of FD-SOI technology. The embodiments of the method described may be adapted to the specific aspects of each application concerned, without departing from the teachings of the invention.

30 [048] As shown in Figure 1A, the carrier wafer 1 is based on a carrier substrate 11, for example a substrate made of single crystal silicon. The carrier substrate 11 is lightly doped, for example with P-type doping. Such doping may be obtained by inserting in the substrate electron acceptor atoms such as boron (B) atoms.

[049] With reference to steps 101 and 102 of the flow diagram of Figure 10, step 101 consists of the deposition on the substrate 11 of a protective layer 12, typically based on oxide (Ox), then the deposition in step 102 of a layer of hard material, for example based
 5 on dielectric nitride (Nx), intended to form a hard mask for a subsequent etching operation for the purpose of forming shallow isolation trenches or STI (Shallow Trench Isolation).

[050] The oxide of the layer 12 may be, for example, silicon dioxide (SiO₂). The deposition of SiO₂ may consist of chemical deposition, such as for example low-pressure
 10 chemical vapour deposition (LPCVD) so as to form high temperature oxide (HTO). It may also consist of the chemical deposition, for example plasma-enhanced chemical vapour deposition (PECVD), of TEOS (short for tetraethyl orthosilicate), of chemical formula Si(OCH₂CH₃)₄ or more simply Si(OEt)₄ as silicon dioxide (SiO₂) seed, followed by simple hydrolysis which then makes it possible to form SiO₂ by release of ethanol
 15 (CH₃CH₂OH). Alternatively, the deposition may also be performed by a physical method, such as cathode sputtering, or centrifugation deposition methods (spin-off).

[051] The dielectric nitride of the layer 13 may be, for example, silicon nitride or Si₃N₄ (SiN for short). This hard material may be deposited by chemical vapour deposition (CVD),
 20 for example low-pressure chemical vapour deposition (LPCVD). Such a method is carried out at a relatively high temperature. Alternatively, the layer 13 of silicon nitride may be formed by plasma-enhanced chemical vapour deposition (PECVD), which is carried out at a relatively low temperature and under vacuum. The layer of SiN thus obtained may have a thickness, for example, of around a hundred nanometres (nm). Other dielectric materials,
 25 notably nitrides of titanium (TiN) and of tungsten (W), as well as various types of nitride oxides, may also be used, alternatively or in addition to silicon nitride (SiN).

[052] With reference now to Figure 1B, the preparation of the carrier wafer 1 continues with the production of isolation trenches 14, in other words shallow isolation trenches (STI),
 30 in the thickness of the substrate 11 of the wafer 1. According to a mode of implementation, and with reference to the flow diagram of Figure 10, this comprises the following sequence of steps:

- a photolithography step 103 defining the zones to be etched in the layer 13 of Si₃N₄ and the protective layer 12 made of SiO₂, by the formation of a hard mask for this etching;
- a step 104 of etching of the layer 13 and the layer 12, made of Si₃N₄ and SiO₂ respectively, through the hard mask formed in step 103, so as to hollow out wells intended to form the isolation trenches (STI) 14 in the silicon 11; and,
- a gapfill step 105 of filling of the trenches with insulating material so as to form said STI.

10 [053] Step 103 involves insulation of the mask needed to perform the etching by a standard photolithographic method.

[054] In step 104, the selective etching of the silicon nitride of the layer 13, then of the silicon dioxide (SiO₂) of the protective layer 12, may be anisotropic etching such as reactive ion etching (RIE). This is a variation of plasma etching (dry etching, highly anisotropic) combining the selectivity of chemical etching and the anisotropy of physical etching. The plasma may then be a fluorocarbon plasma, based on a gas such as carbon tetrafluoride (CF₄) for example, or based on sulphur hexafluoride (SF₆) or based on nitrogen trifluoride (NF₃), or any combination of these gases. The layer of insulating material to be etched, partially protected by the etching mask formed for example by a layer of silicon dioxide which is partially opened up, is placed in a chamber which is placed under vacuum. This chamber has two horizontal and parallel electrodes, the lower electrode serving as plate for receiving the wafer. Once the vacuum has been created in the chamber, the gas is introduced therein. Next, a strong radiofrequency (RF) electric field, for example of around 100 volts per metre or more, is applied to the lower electrode. This generates, in the chamber, a plasma, in other words a partially ionized gas. To be specific, some of the electrons in the molecules of gas are drawn off by the electric field, which ionizes said molecules. The top side of the wafer is then bombarded with ions which breaks it up in the areas not protected by the hard mask. Alternatively, the selective etching in step 104 may be chemical etching (or wet etching) by a solution based on hydrofluoric (HF) acid for example, or physical etching (or dry etching), in other words plasma etching.

[055] Step 105 is a gapfill step consisting in filling the trenches 14 formed previously in step 104 with a thick oxide, for example silicon dioxide (SiO_2). This step 105 makes it possible to deposit the insulating material from the top surface of the microstructure down to the bottom of the trenches 14. Chemical-mechanical polishing or CMP makes it possible
 5 to remove the excess SiO_2 deposited on the surface, and to smooth the top surface of the microstructure as shown in Figure 1B which depicts the microstructure after the sequence of steps 103, 104 and 105. As will be appreciated by those skilled in the art, the oxide deposited in step 105 in the trenches 14 makes it possible to produce the isolation trenches STI in the substrate 11 of the carrier wafer 1 even before the deposition of the layer of
 10 strained silicon by transfer from the donor wafer 2.

[056] In some embodiments, the depth of the trenches 14 is greater than approximately 5 nm. It may be between approximately 5 nm and approximately 300 nm, preferably between approximately 50 nm and approximately 300 nm, and even more preferentially
 15 between approximately 70 nm and approximately 300 nm.

[057] Alternatively, the trenches 14 may be filled with a silicon nitride (SiN), for example Si_3O_4 , instead of silicon dioxide SiO_2 .

20 [058] With reference now to Figure 1C, the next step 106 is a step of chemical-mechanical polishing (CMP) with an etch stop on the silicon of the substrate 11, which allows simultaneous removal of the nitride hard mask of the layer 13, and of the residues of silicon dioxide of the layer 12. Where applicable, this involves lightly oxidizing the silicon of the substrate 11 after the CMP etching is stopped, to reestablish protection by a thin layer of
 25 silicon dioxide (SiO_2). Alternatively, the CMP etching may be stopped on the nitride. The nitride is then removed chemically and the silicon dioxide is removed for example by wet chemical removal using a solution of hydrofluoric (HF) acid, for example.

[059] The diagram in Figure 2 shows the donor wafer 2 which comprises a strained silicon
 30 (sSi) film. For example, the sSi film is a thin layer 23 of silicon (Si) in which the silicon atoms are stretched beyond their normal interatomic distance. This may be obtained by depositing the thin layer of silicon 23 on a substrate 22 based on silicon-germanium (SiGe), by any appropriate silicon deposition method, said SiGe substrate 22 being itself formed on

a base substrate 21 made of Silicon. When the atoms of the thin layer of silicon 23 are aligned on the atoms of the underlying silicon-germanium layer 22 (which are spaced a little further apart from one another, compared to those of a bulk silicon crystal), the bonds between the silicon atoms of the layer 23 are stretched, giving rise to a deformed lattice of silicon atoms. Spacing apart these silicon atoms reduces the atomic forces which interfere with the movement of electrons through the channel of a MOS transistor formed in this strained silicon (sSi) layer 23. This improves the mobility of these charge carriers, which results in better performance of the transistor and lower energy consumption. The donor wafer 2 then comprises a layer of oxide 24, for example based on silicon dioxide (SiO₂). Alternatively, instead of the silicon dioxide SiO₂, the layer 24 may be made of another insulating material, notably another oxide, for example a metal oxide such as aluminium oxide (Al₂O₃), germanium oxide (GeO₂), tin oxide (SnO₂) is a semi-conductor and lead oxide (PbO₂), hafnium oxide (HfO₂) or tantalum oxide (Ta₂O₅).

[060] Note that the production of the donor wafer 2 as shown in Figure 2 is not described in detail herein, to avoid weighing down the present description unnecessarily. It in fact has no particular bearing on the implementation of the method of the invention. If necessary, those skilled in the art may refer to the literature available in the prior art on the subject of FD-SOI technology.

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[061] With reference to the schematic view of Figure 3A, in step 107 the donor wafer 2 is turned over vertically, then aligned and bonded to the carrier wafer 1, so as to produce the microstructure 3 shown in Figure 3B (which may sometimes be referred to as the new carrier wafer 3, in the text below). Those skilled in the art will appreciate that, from the point of view of the top surface of the microstructure 3, the oxide of the layer of oxide 24 of the donor wafer 2 becomes buried oxide (BOX). For the sake of simplicity in the illustration, this BOX is shown in Figure 3A as being only on the donor wafer 2, but the carrier wafer 1 may also likewise have a layer of oxide deposited after step 106 of CMP concerning it, to promote the bonding conditions. Alternatively, provision may be made for only the carrier wafer 1 to have this layer of oxide, and not the donor wafer 2.

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[062] With reference to Figure 4, the substrate 21-22 of (what was) the donor wafer 2 is then removed, represented by step 108 of the flow diagram of Figure 10.

[063] In some embodiments, this may be achieved using the SmartCut® method invented by the C.E.A, according to which the microstructure 3 made up of the donor wafer 2 bonded on the original carrier wafer 1 is subjected to a heat treatment capable of splitting the
 5 microstructure 3 directly below the layer 23 of strained silicon (sSi). The wafer 2 will first be implanted with hydrogen (H) or helium (He), etc., so as to create this weakened zone.

[064] Alternatively, the removal of the substrate 21-22 from the microstructure 3 may be achieved mechanically by grinding, or chemically/mechanically by chemical-mechanical
 10 polishing or CMP. In yet other variants, removal may be achieved by chemical wet etching.

[065] Step 109 then consists of the deposition on the microstructure 3 of Figure 4 of an insulating layer 32 based on oxide (Ox), then the deposition of a layer 33 of nitride (Nx) in step 110. The microstructure 3 shown in Figure 5 is thus obtained. The layer of oxide 32
 15 may be silicon dioxide (SiO₂). The layer of nitride 33, formed on top of the layer 32, may be silicon nitride (SiN). The layers 32 and 33 may be produced by the same technological processes as described above with reference to Figure 1A in relation to the layers 12 and 13, respectively, of the carrier wafer 1. These processes are not described again here.

20 [066] With reference to Figure 6, next comes a step of photolithography 111 and a step of selective etching 112 of the wells 34 that pass through the layer of oxide 32 and the layer of nitride 33, all of which have a bottom on the top face of the layer 23 of strained silicon (sSi), in order to form shallow isolation trenches by oxidation of the sSi of said layer 23 thus exposed. Again in this case, the step of photolithography 111 and the step of selective
 25 etching 112 making it possible to obtain this result are similar to steps 103 and 104 which have already been described, and are therefore not described in detail again here.

[067] Step 113, in accordance with the embodiments of the invention, consists of local oxidation of the strained silicon (sSi) of the layer 23 which is exposed at the bottom of the
 30 wells 34. Thus, supplementary isolation trenches denoted SSTI are produced, based on silicon dioxide (SiO₂) obtained by the local oxidation of the strained silicon (sSi). In the rest of the figures, "SSTI" designates these thin buried oxide trenches 34. The oxidation may be carried out by LOCOS and the structure shown in Figure 7 is obtained, in which the SSTI

join up with the STI initially formed in the substrate 11 of the original carrier wafer. Those skilled in the art will appreciate that, because of the use of the LOCOS method, the sides of the trenches 34 are not vertical, but are slightly inclined in the vertical direction Z.

5 [068] In some embodiments, the supplementary isolation trenches SSTI 34 have a depth equal to or greater than the thickness of the strained silicon film 23, for example between approximately 10 nm and approximately 20 nm, for example of the order of 15 nm.

[069] LOCOS (LOCAl Oxidation of Silicon) is a micro-fabrication method which forms
 10 silicon dioxide SiO₂ in defined areas of a silicon wafer, with the Si-SiO₂ interface below the surface of the wafer itself. This technology was originally developed (before being replaced by shallow trench isolation or STI) in order to isolate MOS field-effect transistors from one another so as to thus limit interference between transistors. The main advantage of this technique lies in the formation, localized around the MOS transistors, of structures
 15 made of silicon dioxide penetrating under the surface of the wafer, which is something that cannot be easily achieved by etching. In the context of the embodiments of the invention, use is likewise made of thermal oxidation of the regions of strained silicon (sSi) which are exposed by the hard mask 33, at a temperature of between 800 and 1200°C, either using water vapour (wet oxidation) or dioxygen (dry oxidation). In both cases, and under the effect
 20 of heat, the oxygen (O₂) penetrates deep into the wafer, reacts with the strained silicon (sSi) that it encounters in the layer 23 and converts it into silica, forming a structure within the volume of the strained silicon (sSi).

[070] Advantageously, the use of the LOCOS technique under the conditions of the
 25 embodiments of the invention makes it possible to form zones 100, 200 and 300 of the strained silicon (sSi) film 23 which are disjointed and isolated from one another, without the sSi being relaxed, in other words without the stress in the sSi being relaxed because it is never opened up. The isolation oxide SSTI thus formed joins up with the deeper isolation oxide STI (in other words the gapfill forming the shallow isolation trenches STI which were
 30 produced in wells 14 formed in the silicon substrate of the original carrier wafer 1 before bonding of the donor wafer 2 for the transfer onto the carrier wafer 1 of the strained silicon (sSi) film 23. This advantageous feature, utilized in the embodiments of the invention, is documented for example in the scientific article by I. De Wolf, J. Vanhellemont,

A. Romano-Rodríguez, H. Norström, H. E. Maes; “Micro-Raman study of stress distribution in local isolation structures and correlation with transmission electron microscopy”, *Journal of Applied Physics* 71 (2), pp. 898–906 (1992); 15 January 1992 (<https://doi.org/10.1063/1.351311>), to which those skilled in the art may refer as necessary.

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[071] Next, step 114 may consist of the removal of the hard mask 33 made of silicon nitride (SiN) and of the residues of silicon dioxide (SiO₂) of the insulating layer 32, so as to obtain the microstructure of Figure 8. For example, the removal of the hard mask made of silicon nitride Si₃N₄ may be carried out by a first chemical wet etching using a solution based on
 10 phosphoric acid (H₃PO₄), for example diluted to 85%, and brought to a temperature of approximately 180°C. The removal of the silicon dioxide (SiO₂) of the insulating layer 32 may then be carried out by a second wet etching, for example based on hydrofluoric (HF) acid. Alternatively, the removal of the hard mask 33 and of silicon dioxide of the insulating layer 32 may be carried out in a single etching operation, for example wet etching based on
 15 hydrofluoric (HF) acid.

[072] As will be appreciated by those skilled in the art, the regions 100, 200 and 300 of this microstructure are disjointed regions of strained silicon (sSi) on a thin insulating layer, namely the insulation (SiO₂ in the example) of the underlying layer 24 of buried oxide
 20 (BOX). By virtue of the implementation of the proposed method, the stress on the sSi in the regions 100, 200 and 300 has not been relaxed, even though said regions 100, 200 and 300 are isolated from one another laterally and vertically by supplementary isolation trenches or SSTI formed in the vertical extension of the isolation trenches STI which were formed at a deeper level in the bulk substrate 11 of the original carrier wafer before the bonding step
 25 107. Microelectronic devices, such as for example MOS transistors or more complex devices in CMOS technology, may thus be produced in the active zones corresponding to the regions 100, 200 and 300 by utilizing the combined advantages of FD-SOI technology and a strained silicon substrate, described in the introduction to this description.

30 [073] In other words, the microelectronic structure 3 depicted in Figure 9, which is produced according to embodiments of the fabrication method according to the invention, includes active zones 100, 200 and 300 that are disjointed (in other words, not continuous) at the surface of the same carrier substrate 11 and isolated from one another by shallow

isolation trenches (STI) 14 extended vertically by supplementary isolation trenches (SSTI) 34 through the buried oxide (BOX) layer 24, each active zone having a respective portion of strained silicon (sSi) film 23, and said sSi film portions resting on the same insulating layer 24 which is itself located above the carrier substrate 11.

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[074] An integrated circuit may comprise the above microelectronic structure, and furthermore at least one field-effect transistor of MOS type produced in an active zone like the zones 100, 200 and 300 of said microstructure in which the portion of strained silicon film 23 serves as fully-depleted silicon-on-insulator (FD-SOI) substrate in which the
10 channel of the MOS transistor may be produced. This transistor thus benefits from the combined advantages of FD-SOI technology and the good electrical conductivity properties contributed by the stress on the silicon.

[075] As those skilled in the art will appreciate, the junction between the insulating
15 material, namely the silicon dioxide (SiO_2) which fills the wells 34 so as to form supplementary isolation trenches (SSTI) and the wells 14 of the shallow isolation trenches (STI) so as to form the final isolation structures, is created through the buried oxide (BOX) of the layer 24 of silicon dioxide (SiO_2), which is continuous. This is why it is referred to as a STI-BOX-SSTI complex isolation structure.

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[076] At least some of the supplementary isolation trenches SSTI 34 have the same horizontal dimensions as the associated shallow isolation trenches STI 14, and are respectively aligned horizontally with said associated trenches 14. In other words, each of these trenches 34 is exactly superimposed with a trench 14 in the vertical direction Z,
25 without the vertical projection of one protruding beyond the other in the longitudinal direction X or in the transverse direction Y. These trenches 34 and 14 are thus said to be aligned vertically. An example of such aligned trenches is shown at the bottom right of the diagram of an example of a structure 3' shown in Figure 11 (see below).

30 [077] According to another advantage of the implementation of the method, it is possible to obtain, in a single process, relatively deep isolations, namely in this case for example the STI between the active zones 100 and 200, the thickness of which may preferably be between approximately 70 nm and approximately 300 nm, and at the same time relatively

shallow isolations such as in this case the SSTI between the active zones 200 and 300 for example, the thickness of which is between approximately 10 nm and 20 nm approximately, bearing in mind that these depths are considered in the vertical direction Y. MOS transistors on FD-SOI substrate may be formed in the zones 200 and 300, respectively, in respective wells in the silicon substrate 11 which have identical doping (type of doping, and level of doping). By contrast, another MOS transistor on FD-SOI substrate may be produced in zone 100 in a well in the silicon substrate 11 which may have different doping, by virtue of the presence of the relatively deep isolation STI which separates it from the well in the silicon substrate 11 which corresponds to the zone 200 or to the zone 300.

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[078] According to another advantage, furthermore, it is possible to place a device produced on the wafer 2 on silicon-on-insulator (SOI) substrate on top of an STI, such that it will then be very far from any silicon of the carrier wafer 1. Therefore, in operation, it will be very far from a polarizing electric field, which makes it a single structure.

15

[079] Lastly, there is nothing to prevent the formation, by etching, of third isolation trenches distinct from the second supplementary isolation trenches SSTI 34. These third trenches may be produced through a second mask, produced beforehand by photolithography in the layer of hard material 33 of Figure 5 which in the example is a nitride, and which is deposited on top of the associated layer of insulating material 32, which is itself deposited on the layer of strained silicon 23 after the removal of the donor substrate 22. Residues of this second mask and of said associated layer of insulating material are removed after the formation of said third trenches. Forming trenches by etching with the aid of a mask does indeed result in the loss of stress in the sSi film, but this loss may be acceptable in some applications in which third isolation trenches may thus be produced in addition to the second supplementary isolation trenches SSTI 34 already formed by oxidation, which make it possible to maintain the stress in the sSi film 23.

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[080] Lastly, with reference to another example of a microelectronic structure 3' shown in Figure 11 (obtained by the same steps of the method as the structure 3 in Figure 9) and as represented by block 115 in the flow diagram of Figure 10, it is possible to make at least one opening through the thickness of one (or more) supplementary trench(es) (SSTI) 34 and through the layer 24 of buried oxide (BOX) so as to expose the underlying bulk silicon substrate 11, as in the region 400 and in the region 700 in the example shown. In Figure 11,

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the supplementary isolation trench 34 which is thus passed through is shown surrounded by a frame in dotted line. For example, the openings 400 and 700 may be produced by etching, through a hard mask obtained by photolithography, of the insulating material (SSTI) of the layer 34 and of the insulating material (BOX) of the layer 24 in order to expose the underlying carrier substrate 11, in respective zones of said carrier substrate 11 in which there are no shallow isolation trenches 14 (STI). Since the etching mask is produced after the trenches STI and SSTI, it is possible to align the alignment patterns of any of these trenches.

[081] Note that the opening 400 divides the supplementary isolation trench SSTI 34 in question into two such derived trenches SSTI, which have smaller horizontal dimensions and which are horizontally adjacent. In the example shown in Figure 11, the derived trench SSTI on the right hand side is aligned vertically with a shallow isolation trench STI 14 with which it is associated and with which it is in continuity of material by means of a portion of the layer 24 of buried oxide BOX associated with them. This mutual alignment results from the alignment of the masks used to form these three respective elements, and provides a complex isolation structure (STI-BOX-SSTI) in the form of a unitary isolation trench made of SiO₂.

[082] Once the openings 400 and 700 have been formed in the SSTI, it is possible to grow the silicon (Si) of the carrier substrate 11 upwards, by epitaxial growth, in said openings 400 and 700, at least up to and including the level of the layer 24 of insulating material (BOX). Access is thus provided to the silicon (Si) of the carrier substrate 11 without relaxing the stress of the film 23 of strained silicon (sSi) in the active zones 500 and 600 shown in Figure 11.

[083] More generally, if it is necessary to make new trenches at the surface of the microelectronic structure 3' for access to the silicon of the carrier substrate 11, bearing in mind that this cannot be done by direct etching of the layer 23 of strained silicon (sSi) without this resulting in the loss of stress of said sSi film, then this may be carried out in a supplementary isolation trench SSTI 34 produced as described above. This etching in an SSTI trench does not in fact result in relaxation of the sSi of the film 23, *i.e.*, does not affect the stress of the film 23 of sSi.

[084] This offers the possibility, where applicable, of producing in these regions 400 and 700, microelectronic devices of NOSO (Not-On-SOI) type, in and/or on the carrier substrate 11 which is a bulk substrate based on doped silicon. It is thus possible to produce active components, for example in conventional CMOS on bulk substrate, in active zones below
5 the surface of the bulk substrate 11 shown, in the region 400 or the region 700, in addition to components, such as the transistor 601 shown, which may be produced in the active zones 500 and 600 in FD-SOI on strained silicon film.

[085] Another possibility offered by the zones 400 and 700 providing access to the silicon
10 of the substrate 11, is for example the ability to polarize (via metallizations, not shown) a well in the substrate 11 forming an active zone in which the source and the drain of the transistor 601 are produced. In Figure 11, this polarization via the zone 400 is symbolized by the arrow 401. It is also possible to polarize the deep well between the shallow isolation
15 trenches (STI) 14, via the zone 700 in Figure 11 which is located on the other side of one of these trenches relative to the well in question. In Figure 11, this polarisation via the zone 700 is symbolized by the arrow 701.

[086] Particular embodiments have been described. Various alternatives and modifications will be apparent to those skilled in the art. For example, the bulk substrate 11 of the carrier
20 wafer 1 does not necessarily have to be doped. It may be a non-doped silicon substrate if components do not need to be produced in this substrate, unlike the possibility described above with reference to the regions 400 and 700.

CLAIMS

1. Method for the fabrication of a microelectronic device, said method comprising:
 - providing a first wafer (1) comprising a carrier substrate (11);
 - 5 - forming, on the carrier substrate (11) of the first wafer (1), first isolation trenches (14);
 - providing a second wafer (2) comprising a donor substrate (21-22);
 - forming, on the donor substrate (21-22) of the second wafer (2), a strained silicon film (23);
 - 10 - bonding the second wafer (2) on the first wafer (1), such that the strained silicon film (23) is located on the first wafer (1) by means of at least one layer of insulating material (24) formed, before bonding, on the first wafer (1) after the formation of the first trenches and/or on the second wafer (2) after the formation of the strained silicon film (23);
 - 15 - removing the donor substrate (21-22) while keeping the layer of insulating material (24) and the strained silicon film (23) on the first wafer (1); and,
 - forming second isolation trenches (34) around and/or along portions of the strained silicon film (23).
- 20 2. Method according to Claim 1, wherein:
 - the first isolation trenches (14) formed in the carrier substrate (11) of the first wafer (1) are trenches referred to as “shallow trenches”, or STI, the depth of which is greater than approximately 5 nm, or between approximately 5 nm and approximately 300 nm, preferably between approximately 50 nm and approximately
 - 25 300 nm, and even more preferentially between approximately 70 nm and approximately 300 nm; and/or
 - the second isolation trenches (34) have a depth equal to or greater than the thickness of the strained silicon film (23), for example between approximately 10 nm and approximately 20 nm, for example of the order of 15 nm.
- 30 3. Method according to Claim 1 or Claim 2, wherein the insulating material of the first trenches (14), the insulating material of the second trenches (34) and/or the insulating material of the layer of insulating material (24) is silicon dioxide, SiO₂.

4. Method according to any one of Claims 1 to 3, wherein the first trenches (14) are formed in the carrier substrate (11) by etching through a first mask produced beforehand by photolithography in a layer of hard material (13) such as for example a nitride, which covers the carrier substrate provided via an associated layer of insulating material (12), residues of said first mask (13) and of said associated layer of insulating material (12) being removed from the carrier substrate (11) after the formation of said first trenches (14).
5. Method according to any one of Claims 1 to 4, further comprising the formation of third isolation trenches produced through a second mask produced beforehand by photolithography in a layer of hard material (33) such as for example a nitride, which is deposited on top of an associated layer of insulating material (32) itself deposited on the layer of strained silicon (23) after removal of the donor substrate, residues of said second mask (33) and of said associated layer of insulating material (32) being removed after the formation of said third trenches.
6. Method according to any one of Claims 1 to 5, wherein the second isolation trenches (34) join up with the first trenches (14) via the layer of insulating material (24) so as to form an isolation structure around and along the strained silicon film (23).
7. Method according to any one of Claims 1 to 6, wherein the second trenches (34) are produced by local oxidation of the silicon of the strained silicon film (23), said local oxidation of the silicon of the strained silicon film (23) being for example thermal oxidation, for example oxidation of LOCOS type.
8. Method according to any one of Claims 1 to 7, wherein the removal of the donor substrate (21-22) is carried out by grinding, by selective removal, or by fracture by implantation, for example using the Smart-Cut® method.
9. Method according to any one of Claims 1 to 8, wherein the donor substrate (21-22) of the second wafer (2) comprises a layer (22) of silicon-germanium, Si-Ge, adapted to stress the silicon of the strained silicon film (23).

10. Method according to any one of Claims 1 to 9, wherein at least one opening (400) is created through the thickness of one of the second trenches (34) and through the layer of insulating material (24) so as to expose the underlying carrier substrate (11), in an area of said carrier substrate (11) in which there are no first trenches (14), and wherein, furthermore,
5 the silicon (Si) of the carrier substrate (11) is grown upwards by epitaxial growth in the opening (400), at least up to and including the level of the layer of insulating material (24).
11. Method according to any one of Claims 1 to 10, wherein at least some of the second isolation trenches (34) have the same horizontal dimensions as associated first trenches (14),
10 and are respectively aligned vertically with said associated first trenches (14).
12. Microelectronic structure obtained by implementing the fabrication method according to any one of Claims 1 to 11, said structure comprising disjointed active zones (100, 200, 300) at the surface of the same carrier substrate (11), isolated from one another by deep and
15 less deep isolation trenches (14-24-34), each active zone having a respective portion of strained silicon film (23), and said strained silicon film portions resting on the same insulating layer (24) which is itself located above the carrier substrate (11).
13. Microelectronic structure according to Claim 12, wherein the insulating material of the
20 first trenches (14), the insulating material of the second trenches (34) and/or the insulating material of the layer of insulating material (24) is silicon dioxide, SiO₂.
14. Microelectronic structure according to Claim 12 or Claim 13, wherein the second
25 trenches (34) have non-vertical sides.
15. Integrated circuit comprising the microelectronic structure according to one of Claims 12 to 14, and further comprising at least one field-effect transistor of MOS type produced in an active zone (100, 200, 300) of said microstructure of which the portion of strained silicon film (23) serves as fully-depleted silicon-on-insulator (FD-SOI) substrate in which
30 the channel of the MOS transistor is produced.