WHAT IS CLAIMED IS:

1. A three-dimensional semiconductor device, comprising:

a stack structure that includes a plurality of gate electrodes stacked on a first substrate;

a plurality of channel regions that penetrate the stack structure and extend in a direction perpendicular to a top surface of the first substrate;

a first interlayer dielectric layer on the stack structure;

a first connection layer that penetrates the first interlayer dielectric layer, and is electrically connected with the plurality of channel regions and with at least one of the plurality of gate electrodes; and

a peripheral circuit structure on the first interlayer dielectric layer,

wherein the peripheral circuit structure includes a plurality of peripheral circuit elements on a first surface of a second substrate, the peripheral circuit elements being electrically connected to the plurality of channel regions and at least one of the plurality of gate electrodes,

wherein the first substrate has a first crystal plane parallel to the top surface of the first substrate,

wherein the second substrate has a second crystal plane parallel to the first surface of the second substrate,

wherein an arrangement direction of atoms of the first crystal plane that are exposed on the top surface of the first substrate intersects an arrangement direction of atoms of the second crystal plane that are exposed on the first surface of the second substrate, and

wherein the first connection layer includes a plurality of bit lines, the bit

lines connecting with the plurality of channel regions and extending in a <110> crystal direction of silicon of the first substrate.

2. The device of claim 1, wherein the first crystal plane of the first substrate and the second crystal plane of the second substrate are a {100} crystal plane of silicon.

3. The device of claim 1 or claim 2, wherein a <110> crystal direction of silicon of the first substrate is parallel to a <100> crystal direction of silicon of the second substrate.

4. The device of claim 1 or claim 2, wherein a <100> crystal direction of silicon of the first substrate has an angle of 45º with a <100> crystal direction of silicon of the second substrate.

5. The device of any one of claims 1 to 4, further comprising:

a second interlayer dielectric layer on the first surface of the second substrate, the second interlayer dielectric layer covering the plurality of peripheral circuit elements,

wherein the first interlayer dielectric layer is in contact with the second interlayer dielectric layer.

6. The device of claim 5, further comprising:

a second connection layer that penetrates the second interlayer dielectric layer, and is electrically connected with at least one of the plurality of peripheral

circuit elements.

7. The device of claim 6, wherein the first connection layer and the second connection layer are in contact with each other at an interface between the first interlayer dielectric layer and the second interlayer dielectric layer.

8. The device of any one of claims 1 to 7, wherein a second surface of the second substrate is in contact with the first interlayer dielectric layer, the second surface being opposite to the first surface.

9. The device of any one of claims 1 to 8,

wherein one of the peripheral circuit elements includes a transistor, and

wherein a source and a drain of the transistor are spaced apart from each other in a <100> crystal direction of silicon of the second substrate.

10. A three-dimensional semiconductor device, comprising a cell structure and a peripheral circuit structure that are stacked on one another,

wherein the cell structure includes:

a plurality of gate electrodes that are stacked on a top surface of a first substrate;

a channel region that vertically penetrates the plurality of gate electrodes; and

a bit line on the plurality of gate electrodes and connected to the channel region,

wherein the peripheral circuit structure includes:

at least one transistor on a top surface of a second substrate; and

a connection layer on the at least one transistor,

wherein the bit line extends in a first direction,

wherein a <100> crystal direction of the first substrate intersects a <100> crystal direction of the second substrate, and

wherein the bit line extends in a <110> crystal direction of a crystal structure of the first substrate.

11. The device of claim 10,

wherein the top surface of the first substrate is a {100} crystal plane of the crystal structure of the first substrate,

wherein the top surface of the second substrate is a {100} crystal plane of the crystal structure of the second substrate, and

wherein a <110> crystal direction of the crystal structure of the first substrate is parallel to the <100> crystal direction of the crystal structure of the second substrate.

12. The device of claim 11,

wherein the <110> crystal direction of the crystal structure of the first substrate is the same as the first direction, and

wherein the <100> crystal direction of the crystal structure of the second substrate is the same as the first direction.

13. The device of any one of claims 10 to 12,

wherein the peripheral circuit structure is disposed on the cell structure,

and

wherein the bit line is electrically connected to the connection layer.

14. The device of any one of claims 10 to 13,

wherein the peripheral circuit structure is disposed such that the connection layer faces the cell structure, and

wherein the connection layer and the bit line are in direct contact with each other.

15. The device of any one of claims 10 to 14,

wherein the peripheral circuit structure is disposed such that the second substrate faces the cell structure, and

wherein the peripheral circuit structure further includes a via that penetrates the second substrate, the via connecting the connection layer to the bit line.

16. The device of any one of claims 10 to 15,

wherein the cell structure is disposed on the peripheral circuit structure, and

wherein the cell structure further includes a contact plug that penetrates the first substrate, the contact plug connecting the bit line to the connection layer.

17. A three-dimensional semiconductor device, comprising:

a stack structure that includes a plurality of gate electrodes stacked on a first substrate;

a plurality of channel regions that penetrate the stack structure and extend in a direction perpendicular to a top surface of the first substrate;

a first interlayer dielectric layer on the stack structure;

a first connection layer that penetrates the first interlayer dielectric layer to come into electrical connection with the plurality of channel regions and with at least one of the plurality of gate electrodes; and

a peripheral circuit structure on the first interlayer dielectric layer,

wherein the peripheral circuit structure includes:

at least one transistor on a top surface of a second substrate;

a second connection layer on the at least one transistor; and

a second interlayer dielectric layer on the top surface of the second substrate, the second interlayer dielectric layer covering the at least one transistor,

wherein the first substrate has a first crystal plane parallel to the top surface of the first substrate,

wherein the second substrate has a second crystal plane parallel to the top surface of the second substrate,

wherein a <100> crystal direction of the first crystal plane intersects a <100> crystal direction of the second crystal plane,

wherein a source and a drain of the at least one transistor are spaced apart from each other along a direction perpendicular to an extending direction of the first connection layer, and

wherein the first connection layer includes a plurality of bit lines, the bit lines connecting with the plurality of channel regions and extending in a <110> crystal direction of the first crystal plane of the first substrate.

18. The device of claim 17,

wherein the first substrate and the second substrate have a diamond crystal structure, and

wherein the first crystal plane of the first substrate and the second crystal plane of the second substrate are a {100} crystal plane.

19. The device of claim 17 or claim 18, wherein the <100> crystal direction of the first crystal plane has an angle of 45° with respect to the <100> crystal direction of the second crystal plane.