ABSTRACT OF THE DISCLOSURE

PMOS TRANSISTOR STRAIN OPTIMIZATION WITH RAISED JUNCTION REGIONS

Optimal strain in the channel region of a PMOS transistor is provided by silicon alloy material in the junction regions of the device in a non-planar relationship with the surface of the substrate. The silicon alloy material, the dimensions of the silicon alloy material, as well as the non-planar relationship of the silicon alloy material with the surface of the substrate are selected so that the difference between the lattice spacing of the silicon alloy material and of the substrate causes strains in the silicon alloy material below the substrate surface, as well as above the substrate surface, to affect an optimal silicon alloy induced strain in the substrate channel. In addition, the non-planar relationship may be selected so that any strains caused by different lattice spaced layers formed over the silicon alloy material have a reduced effect on the strain in the channel region.