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"PARALLEL COMPARATOR".

The present invention relates to a parallel comparator.

One such known circuit is shown in Figure 1 of the accompanying drawings. It has been used as a parallel comparator in an analog-to-digital (A/D) converter. This circuit is formed as a two-stage differential amplifier so as to steepen the switching characteristics, i.e. to increase the gain.

Accordingly, the circuit shown in Figure 1 has defects. One such defect is that the number of circuit constituting elements is large with the result that the power consumption is high.

Moreover, since comparator outputs OUT_1 to OUT_3 respectively vary with reference to reference voltages V_1 to V_3 , there arises another defect in that the logic circuit construction in the case of conversion into digital signals of binary code is complicated.

Since the A/D converter constructed as a monolithic or hybrid IC has its circuit construction

fixed, it is convenient to extend the output bits.

According to the invention there is provided a parallel comparator including:

- 5 (a) a plurality of comparator portions each having first and second transistors differentially connected;
 - (b) an $(n - x)$ th comparator portion having first and second transistors differentially connected;
 - (c) an $\underline{n}$ th comparator portion having first
10 and second transistors differentially connected; and
 - (d) an $(n + x)$ th comparator portion having first and second transistors differentially connected;
- where $\underline{n}$ and $\underline{x}$ are positive integers and $\underline{n}$ is at least greater than $\underline{x} + 1$ and $\underline{x}$ is equal to 2 or greater than 2;
- 15 wherein said first transistors of said plurality of comparator portions, said $(n-x)$ th comparator portion, said $\underline{n}$ th comparator portion and said $(n+x)$ th comparator portion have their base electrode supplied with an analog input signal whereas said second transistors
- 20 of said above comparator portions have their base electrode supplied with reference voltage having different levels, wherein the collector electrode of said second transistor of said $(n-x)$ th comparator portion and the collector electrode of said first transistor
- 25 of said $\underline{n}$ th comparator portion are commonly connected $(n-x)$ load means, and wherein the collector electrode of said second transistor of said $\underline{n}$ th comparator portion

and the collector electrode of said first transistor of said $(n+x)$ th comparator portion are commonly connected to n th load means.

The parallel comparator may further include:

5 (e) an $(n-x)$ th amplifying transistor having its base electrode connected with said $(n-x)$ th load means;

(f) an n th amplifying transistor having its base electrode connected with said n th load means; and

10 (g) a constant current source commonly connected to the emitter electrode of said $(n-x)$ th amplifying transistor and the emitter electrode of said n th amplifying transistor.

In the case where x = 2; the collector electrode 15 of the second transistor of the $(n-2)$ th comparator portion and the collector electrode of the first transistor of the n th comparator portion may be commonly connected with $(n-2)$ th load means; the collector electrode of the second transistor of the $(n-1)$ th comparator portion 20 and the collector electrode of the first transistor of the $(n+1)$ th comparator portion may be commonly connected with $(n-1)$ th load means; and the collector electrode of the second transistor of the n th comparator portion and the collector electrode of the first transistor of the $(n+2)$ th comparator portion may be commonly 25 connected with n th load means.

The present invention will now be described in greater detail by way of examples with reference

to the remaining figures of the accompanying drawings,
wherein:-

Figure 2 is a circuit diagram of a parallel
comparator (not being an embodiment of the present
5 invention);

Figure 3 shows three waveforms which explain
the operation of the comparator shown in Figure 2;

Figure 4 is a circuit diagram showing a first
preferred embodiment of a parallel comparator;

10 Figure 5 is a set of waveforms for explaining
the operation of the embodiment of Figure 4;

Figures 6A and 6B are circuit diagrams showing
a first form of an A/D converter disclosed in our
Divisional Application No. 8325182 incorporating
15 a second embodiment of a parallel converter;

Figure 7 shows a series of waveforms for
explaining the operation of the embodiment shown in
Figures 6A and 6B;

Figure 8 is a block diagram showing a second
20 form of an A/D converter;

Figures 9A and 9B are circuit diagrams showing
a third form of an A/D converter incorporating a third
embodiment of a parallel converter;

Figure 10 is a block diagram showing the
25 interconnection of two A/D converters in a first
form;

Figure 11 is a block diagram showing the interconnection of two A/D converters in a second form; and

Figure 12 is a block diagram showing the interconnection of four A/D converters.

Referring first to Figure 2, the parallel comparator (which does not form an embodiment of the present invention) comprises a plurality of basic differential transistor circuits which include paired differential transistors Q_{220} , Q_{221} to Q_{226} and Q_{227} , and constant current sources I_0 connected with their respective common emitter electrodes.

The differential transistors Q_{220} to Q_{226} indicated by even numbers have their base electrodes commonly fed with an analog voltage signal V_{IN} , whereas the other differential transistors Q_{221} to Q_{227}

indicated by odd numbers have their base electrodes respectively fed with reference voltages V_1 to V_m ($V_1 < V_2 < V_3 - - - < V_m$).

Moreover, in the order which is started from the comparator portions fed with the lower reference voltage V_1 , the collector electrodes of the adjoining differential transistors are commonly connected with each other and with a plurality of load resistors. The collector electrode of the other differential transistor Q_{221} in the first comparator portion and the collector electrode of one differential transistor Q_{222} in the second comparator portion are commonly connected with each other and with a load resistor R_{221} . The collector electrode of the other differential transistor Q_{223} in the second comparator portion and the collector electrode of one differential transistor Q_{224} in the third comparator are commonly connected with each other and with a load resistor R_{222} . Generally speaking, the collector electrode of the other differential transistor in the n th comparator portion and the collector electrode of the one differential transistor at the $(n + 1)$ th comparator portion are commonly connected with each other and with a load resistor.

Moreover, the collector electrodes of one

③
differential transistor Q_{220} in the lowest comparator portion and of the other differential transistor Q_{227} in the highest comparator portion are commonly connected not with the collector electrode of any transistor but with load resistors R_{220} and R_{224} , respectively.

The outputs of the comparator constructed of the respective load resistors R_{220} to R_{224} are applied to the base electrodes of amplifying transistors Q_{228} to Q_{232} . The emitter electrodes of the transistors Q_{228} to Q_{232} are commonly connected with one another and with a constant current source I_0' . Moreover, the collector electrodes of the transistors Q_{228} to Q_{232} are connected with load resistors R_{225} to R_{229} , respectively, in order to provide outputs OUT_1 to OUT_m .

The operation of this embodiment will now be described with reference to the waveforms shown in Figure 3.

When the analog voltage signal V_{IN} is smaller than V_i , the transistors Q_{220} , Q_{222} , Q_{224} and Q_{226} are rendered non-conductive, whereas the transistors Q_{221} , Q_{223} , Q_{225} and Q_{226} are rendered conductive. As a result, only the amplifying transistor Q_{228} is rendered conductive so that only the output OUT_1 supplied through that transistor is at a low level.

Next, for $V_1 < V_{IN} < V_2$, the transistor Q_{221} is rendered non-conductive because of $V_1 < V_{IN}$, whereas the transistor Q_{222} is rendered non-conductive because of $V_{IN} < V_2$. As a result, a high level is generated from the commonly connected collector electrodes of the transistors Q_{221} and Q_{222} , and only the output OUT_2 supplied through the amplifying transistor Q_{229} is at the low level.

Subsequently, only the output OUT_3 is at the low level in a similar manner for $V_2 < V_{IN} < V_3$.

Since the outputs OUT_1 to OUT_m consecutively take the low level so that they can be made substantially equal to a decimal code, the conversion into the decimal code or binary code can be accomplished remarkably simply.

On the other hand, the amplifying transistors Q_{228} to Q_{232} substantially operate as differential transistors. More specifically, when the amplifying transistor Q_{229} , for example, is changed from the non-conductive to the conductive state, the amplifying transistor Q_{228} is changed from the conductive to the non-conductive state. Thus, only one of the amplifying transistors is rendered conductive.

As a result, the circuit shown in Figure 2 can attain the same high gain as that of the two-stage

differential amplifying circuit shown in Figure 1.

Moreover, in the circuit shown in Figure 2, the number of the resistors and the transistors is reduced and the power consumption is also reduced as a result of
5 firstly the differential transistors which form the comparator portions being commonly connected with each other and with the load resistors, and secondly because the amplifying transistors perform the differential amplifications with the use of the other comparator
10 outputs, and thirdly because the amplifying transistors commonly use a single constant current source.

Moreover, it will be noted that a pair of transistors having their collector electrodes commonly connected can be formed in an identical device forming
15 region (i.e., a well region) so that the size of the chip can be reduced in the manufacture of a monolithic IC.

Referring now to the first embodiment shown in Figure 4, it will be noted that the circuit comprises two comparator groups such that the order of commonly
20 connecting the collectors of the differential transistors forming comparator portions is made to occur between every other comparator.

As shown, there are arranged eight differential transistor circuits which include paired differential

transistors Q_{250} , Q_{251} to Q_{264} , and Q_{265} , and constant current sources I_0 connected to the common emitter electrodes thereof. In similar manner to the foregoing embodiment, the differential transistors Q_{250} to Q_{264} indicated by even numbers have their base electrodes commonly fed with the analog voltage signal V_{IN} , whereas the other transistors Q_{253} to Q_{265} indicated by odd numbers have their base electrodes consecutively fed with the reference voltages V_1 to V_7 (wherein: $V_1 < V_2 < V_3 - - - < V_7$) which are derived by voltage dividing resistors R_{270} to R_{277} . The differential transistor Q_{251} has its base electrode fed with the lowest voltage V_L for underflow detection.

Moreover, in the order of the comparator portions which are fed with the lower reference voltage V_L and the reference voltage V_1 , the collector electrodes of the alternately adjacent differential transistors are commonly connected with each other and with the load resistor.

The collector electrode of the other differential transistor Q_{251} in the first comparator portion and the collector electrode of one differential transistor in the third comparator portion are commonly connected with each other and with the load resistor R_{251} .

Moreover, the collector electrode of the other differential transistor Q_{255} in the third comparator portion and the collector electrode of one differential transistor Q_{258} in the fifth comparator portion are commonly connected with each other and with a load resistor R_{254} . Thus, the collector electrodes are commonly connected between odd numbered comparator portions, and the collector electrodes are likewise similarly connected between even numbered comparator portions from the second comparator portion.

In the first comparator group having its collector electrodes commonly connected between odd numbered comparator portions and the second comparator group having its collector electrodes commonly connected between even numbered comparator portions as described above, load resistors R_{250} , R_{252} , R_{258} and R_{259} are connected, respectively, with the differential transistors Q_{250} and Q_{252} at the lowest comparator portions of the respective groups, i.e., the first and second comparator portions and with the other differential transistors Q_{263} and Q_{265} at the highest comparator portions, i.e., the seventh and eighth comparator portions.

The outputs a to j of the respective comparator portions are fed out through respective

emitter-follower transistors Q_{266} to Q_{275} . Of these, in order to prepare the lowest bit signals A and $\bar{A}$ in accordance with the Gray code, the emitter electrodes of the transistors Q_{269} and Q_{273} and the emitter electrodes of the transistors Q_{268} , Q_{271} and Q_{275} are commonly connected with each other and with a resistor R_{264} and a constant current source I_0' , and a resistor R_{266} and a constant current source I_0' , respectively, to thus constitute level shift circuits.

On the other hand, the emitter electrode of the other transistor Q_{266} is connected with a resistor R_{260} and the constant current circuit which likewise constitute a level shift circuit.

The operation of the embodiment shown in Figure 4 will be explained in greater detail with reference to the waveforms shown in Figure 5.

The transistor Q_{250} is rendered non-conductive for $V_{IN} < V_L$ in order to raise the collector output a to the high level. The transistor Q_{252} is rendered non-conductive for $V_{IN} < V_1$ in order to raise the collector output b to the high level.

On the other hand, the transistor Q_{263} is rendered non-conductive for $V_{IN} > V_6$ in order to raise the collector output i to the high level.

The transistor Q_{265} is rendered non-conductive for $V_{IN} > V_7$ in order to raise the collector output j to the high level.

Moreover, the outputs c to h , which are prepared by making the collector electrodes common amongst the alternate comparator portions, are at the high level only in the case where the paired transistors having their collector electrodes commonly connected are non-conductive together. The output c is at the high level only for $V_L < V_{IN} < V_2$ when the transistors Q_{251} and Q_{254} are rendered non-conductive together. The output d is at the high level only for $V_1 < V_{IN} < V_3$ when the transistors Q_{253} and Q_{256} are rendered non-conductive together. Likewise, the output e is at the high level only for $V_2 < V_{IN} < V_4$; the output f is at the high level only for $V_3 < V_{IN} < V_5$; the output g is at the high level only for $V_4 < V_{IN} < V_6$; and the output h is at the high level only for $V_5 < V_{IN} < V_7$.

Moreover, the circuit shown uses diode OR circuits which makes use of the base and emitter electrodes of the emitter-follower transistors. The inversed lowest bit signal $\bar{A}$ of Gray code can be prepared by taking the logical sum $\underline{b} + \underline{f} + \underline{j}$ of the outputs $\underline{b}$, $\underline{f}$ and $\underline{j}$, and the lowest bit signal A of the Gray code

can be prepared by taking the logical sum $\underline{d} + \underline{h}$ of the outputs $\underline{d}$ and $\underline{h}$.

Incidentally, the other bit signals B, C and so on of Gray code can be prepared by similarly taking the logical sums $\underline{e} + \underline{g}$ and $\underline{g} + \underline{j}$. In order to generate the respective inverted outputs $\bar{B}$ and $\bar{C}$, however, it is necessary to take the logical sums $\underline{c} + \underline{i}$ and $\underline{c} + \underline{e}$, but this is disadvantageous because of the danger that the outputs $\underline{e}$ and $\underline{i}$ are doubly used. In order to avoid this danger, the level-shifted signals $\underline{c}'$ to $\underline{i}'$ are prepared by means of diode OR circuits (not shown).

Incidentally, if the double signals $\underline{e}$ and $\underline{i}$ are prepared through a multi-emitter transistor, the other Gray code signals B, $\bar{B}$, C and $\bar{C}$ can be generated similarly to the Gray code signals A and $\bar{A}$.

Although not shown, the code signals A and $\bar{A}$, B and $\bar{B}$, and C and $\bar{C}$ of opposite phases are fed to and amplified by the differential amplifying circuit in order to realize the high gain.

In the case where the collector electrodes are connected between alternate comparators, as shown, the switching operation of the differential transistors is performed by using the higher and lower ones of a reference voltage as border lines. As a result, a higher-speed operation can be realized than that of the embodiment

shown in Fig. 2. In other words, the frequency characteristics can be increased two times. Moreover, the allowability of the comparator for the dispersion in an input threshold can be enlarged.

5 It should be noted that in the case where the digital signal of Gray code is to be prepared, the lowest bit signal can be directly generated.

 Incidentally, it is possible to simplify the circuit, to reduce the power consumption and to reduce
10 the size of the chip for manufacture of the monolithic IC by making the collector electrodes common and by providing a differential amplifier after the Gray coding.

 Furthermore, it should be noted that the circuit could be made merely by changing the order of the comparators
15 having their collector electrodes commonly connected partly because the lowest big signals A and $\bar{A}$ of Gray code can be directly prepared and partly because the Gray code signal B, for example, is sufficient to be at the high level for $V_2 < V_{IN} < V_6$, as viewed from the waveforms shown in Fig. 5.

20 Referring now to Figs. 6A and 6B, a parallel comparator, which can directly generate the Gray code signal, and a four-bit A/D converter making use of that comparator are shown in detail. It should be noted that
24 the parts enclosed by broken lines are formed in the

monolithic IC.

Resistors R_0 to R_{15} , which are connected in series between the terminals B and F, divides the lowest voltage V_L and the highest V_H each one sixteenth in order to prepare the reference voltages V_1 to V_{15} for the fifteen comparators.

Paired differential transistors Q_3, Q_4 to Q_{31} and Q_{32} together constitute a comparator 1. The transistors Q_4 to Q_{32} indicated by even numbers have their base electrodes fed with the reference voltages V_1 to V_{15} ($V_1 < V_2 < V_3 - - - < V_{15}$), respectively, which are prepared by the resistors R_0 to R_{15} , whereas the transistors Q_3 to Q_{31} indicated by odd numbers have their base electrodes fed with the analog voltage signal V_{IN} coming from the terminal A.

The transistor Q_2 having its base electrode fed with the lowest voltage V_L and the transistor Q_1 having its base electrode fed with the analog voltage signal V_{IN} together constitute the comparator which is provided for underflow detection.

The collector electrodes of the paired differential transistors constituting the fifteen parallel comparators are connected to form three kinds of window type comparators so as to prepare the digital

signals A to C of Gray code.

In order to prepare the lowest bit signals A and $\bar{A}$ of Gray code, the collector electrodes of the alternate comparator portions from the lowest comparator portions Q_3 and Q_4 are commonly connected with each other and with collector resistors R_{19} , R_{22} , R_{25} , R_{27} , R_{30} , R_{32} , and R_{34} , respectively. The collector electrodes of the transistors Q_3 and Q_{32} left uncommon are connected with collector resistors R_{18} and R_{36} .

The collector voltage of the transistors Q_4 and Q_7 made common is at the high level only for $V_1 < V_{IN} < V_3$ because the transistors Q_4 and Q_7 are rendered non-conductive together. The collector voltage of the next transistors Q_8 and Q_{11} made common is at the high level only for $V_3 < V_{IN} < V_5$ because the transistors Q_8 and Q_{11} are rendered non-conductive together. Likewise, the collector voltage of the subsequent transistors made common is consecutively at the high level as the analog voltage is raised.

On the other hand, the collector voltage of the transistor Q_3 is at the high level only for $V_1 > V_{IN}$ because the transistor Q_3 is rendered non-conductive, whereas the collector voltage of the transistor Q_{32} is at the high level only for $V_{15} < V_{IN}$ because the

transistor Q_{32} is rendered non-conductive.

As a result, of the collector voltages made common, the alternate collector voltages of the transistors Q_4 and Q_7 and Q_{12} and Q_{15} become equal to the lowest bit signals A and $\bar{A}$ of Gray code, as shown in Fig. 7.

As a result, the Gray code signal A can be prepared by making common through emitter-follower transistors Q_{36} , Q_{42} , Q_{47} , and Q_{51} , in other words, by effecting passage through the diode OR circuit making use of the base and emitter electrodes of the transistors.

On the other hand, the alternate collector voltages of the transistors Q_8 and Q_{11} , and Q_{16} and Q_{19} made common, whilst including the collector voltages of the transistors Q_3 and Q_{32} , are at the high level when the Gray code signal A is at the low level. As a result, by making the emitter-follower transistors Q_{35} , Q_{39} , Q_{44} , Q_{49} and Q_{53} common, the logic sum output similar to the aforementioned one is generated to prepare the inverted Gray code signal $\bar{A}$.

In order to prepare the second bit signals B and $\bar{B}$ of Gray code, the collector electrodes of the comparator portions of every fourth order from the second comparator portions of Q_5 and Q_6 are commonly connected

with each other and with collector resistors R_{21} , R_{26} and R_{31} , respectively.

The collector electrodes of the transistors Q_5 and Q_{30} left uncommon at both ends are connected with collector resistors R_{20} and R_{35} , respectively.

The collector voltage of the transistors Q_6 and Q_{13} made common is at the high level only for $V_2 < V_{IN} < V_6$ because the transistors Q_6 and Q_{13} are rendered non-conductive together. The collector voltage of the next transistors Q_{14} and Q_{21} made common is at the high level only for $V_6 < V_{IN} < V_{10}$ because the transistors Q_{14} and Q_{21} are rendered non-conductive together. Moreover, the collector voltage of the next transistors Q_{22} and Q_{29} made common is at the high level only for $V_{10} < V_{IN} < V_{14}$ because the transistors Q_{22} and Q_{29} are rendered non-conductive together.

On the other hand, the collector voltages of the transistors Q_5 and Q_{30} at both ends are at the high level only for $V_2 > V_{IN}$ and for $V_{14} < V_{IN}$, respectively, because the transistors Q_5 and Q_{30} are rendered non-conductive, respectively.

As a result, in the collector voltages made common, the alternate collector voltages of the transistors Q_6 and Q_{13} , and Q_{22} and Q_{29} become equal to the second bit signal B of Gray code, as shown in Fig. 7.

As a result, by making common through emitter-follower transistors Q_{38} and Q_{48} , the logic OR output similar to the aforementioned one is generated to prepare the Gray code signal B.

5 On the other hand, both the collector voltages of the transistors Q_5 and Q_{30} at both the ends and the collector voltage of the transistors Q_{14} and Q_{21} made common are at the high level when the Gray code signal B is at the low level. As a result, by making common through
10 emitter-follower transistors Q_{37} , Q_{43} and Q_{52} , the logic sum output similar to the aforementioned one is generated to prepare the inverted Gray code Signal $\bar{B}$.

In order to prepare the third bit signal C of Gray code, moreover, in view of the comparator portions Q_{25}
15 and Q_{26} at intervals of seven from the fourth comparator portions Q_9 and Q_{10} , the collector electrodes of the transistors Q_{10} and Q_{25} are commonly connected with each other and with a collector resistor R_{24} , whereas the collector electrodes of the transistors Q_9 and Q_{26} at both
20 ends are connected with collector resistors R_{23} and R_{33} , respectively.

The collector voltage of the transistors Q_{10} and Q_{25} made common is at the high level only for $V_4 < V_{IN} < V_{12}$ because the transistors Q_{10} and Q_{25} are rendered

non-conductive together. As a result, the Gray code signal C, as shown in Fig. 7, can be prepared.

On the other hand, the collector voltages of the transistors Q_9 and Q_{26} at both the ends are at the high level only for $V_4 > V_{IN}$ and for $V_{12} < V_{IN}$, respectively, because the transistors Q_9 and Q_{26} are rendered non-conductive, respectively. As a result, by making common through emitter-follower transistors Q_{40} and Q_{50} , the logic sum output similar to the aforementioned one is generated to prepare the inverted Gray code signal $\bar{C}$.

Moreover, at the outputs of the comparator portions Q_{17} and Q_{18} using the intermediate voltage V_8 as the reference voltage, there can be directly generated the highest bit signals D and $\bar{D}$ of Gray code as shown in Fig. 7.

On the other hand, the comparator portions Q_1 and Q_2 prepare the underflow signals UF and $\bar{UF}$ for detecting the inequality of $V_L > V_{IN}$.

The Gray code signals A to C and $\bar{A}$ to $\bar{C}$ and the underflow signals UF and $\bar{UF}$ are subjected to level conversions by emitter-follower transistors Q_{33} to Q_{53} , resistors R_{37} to R_{46} and constant current circuits I_{017} to I_{026} and are amplified to the TTL level signals by the actions of differential amplifying transistor circuits Q_{54} , Q_{55} to Q_{62} and Q_{63} .

A master latch circuit 3a which is receptive of the Gray code signal A, comprises: the input transistor Q_{63} ; a feedback input transistor Q_{64} ; the resistor R_{47} connected with the commonly connected collector electrodes of the transistors Q_{63} and Q_{64} ; a diode connected transistor Q_{65} connected with the commonly connected emitter electrodes of the transistors Q_{63} and Q_{64} to effect the level shifts; an emitter load resistor R_{48} ; a transistor Q_{66} having its base electrode fed with the input signal through the level shift transistor; a Schottky barrier diode D_7 (which will be referred to merely as a "diode") and a constant current load circuit I_{038} connected in series with the diode D_7 ; a transistor Q_{67} which is receptive of the output of the diode D_7 ; a collector load resistor R_{49} and an emitter load resistor R_{50} associated with the transistor Q_{67} ; a transistor Q_{68} having its base electrode fed with the emitter output of the transistor Q_{67} ; a diode D_8 for feeding back the collector output to the base electrode of the feedback input transistor Q_{64} ; a diode D_1 connected to the base electrode of the input transistor Q_{63} and constituting a gate circuit; and a diode D_6 and a constant current circuit I_{037} connected to the base electrode of the feedback input transistor Q_{64} and constituting a gate circuit.

Master latch circuits 3b to 3d, which are made receptive

to the other Gray code signals B to D, are constructed in a similar manner.

On the other hand, a master latch circuit 6, which is made receptive of the underflow signal UF, is also constructed, in a basically similar manner to the latch circuit 3a.

The difference therebetween resides in that the diodes D_{11} and D_{12} constituting a gate circuit 7 are connected with the collector electrode of a transistor Q_{72} constituting the inverter circuit of the previous stage, and in that TTL transistors Q_{75} and Q_{76} constituting the gate circuit 7 and having their inputs fed with clock pulses CP are connected with a transistor Q_{74} constituting the inverter circuit of the subsequent stage.

The commonly connected cathode electrode of the diodes D_{11} and D_{12} constituting the gate circuit 7 is connected with an external terminal L so that it is selectively fed with a voltage at zero volts or V_{CC} .

A waveform shaping circuit 9 consists of an inverter circuit IN to prepare the clock pulses CP, which are inverted from the clock pulses $\overline{CP}$ fed from an external terminal K, and to supply the clock pulses CP to the commonly connected cathode electrodes of the diodes D_1 to D_5 which are connected with the base electrodes of the input transistors of the latch circuits and which

constitute the gate circuit. Moreover, the circuit 9 supplies the clock pulses $\overline{CP}$, which are inverted through the TTL transistors Q_{75} and Q_{76} constituting the gate circuit 7, to the commonly connected cathode electrodes of the diodes D_6 and D_9 which are connected with the base electrode of the feedback input transistor and which constitute the gate circuit.

In the master latch circuits 3a to 3d, therefore, when the clock pulses CP are at the high level, the diodes D_1 to D_5 are rendered non-conductive to supply their respective input signals to the input transistors Q_{63} , Q_{69} etc., whereas the feedback input transistors Q_{64} , Q_{70} etc., are rendered non-conductive in response to the low level of the clock pulses $\overline{CP}$ because the diodes D_6 , D_9 etc., are rendered conductive. As a result, the transistors Q_{66} , Q_{67} etc., constituting the inverter circuit are rendered conductive and non-conductive in accordance with the Gray code signals, which are fed through the input transistor Q_{63} , in order to receive the signals.

Since the diodes D_1 to D_5 are rendered conductive whilst the clock pulses CP are at the low level, the input transistors Q_{63} , Q_{69} etc., are rendered non-conductive. On the contrary, since the clock pulses $\overline{CP}$ are at the high level, the diodes D_6 , D_9 etc., are rendered non-conductive.

As a result, when the transistor Q_{67} constituting the

inverter circuit of the subsequent stage is non-conductive in response to the input signal, the feedback diode D_8 is rendered non-conductive whereas the feedback input transistor Q_{64} is rendered conductive. Thus, the latching operation is such that the transistor Q_{66} constituting the inverter circuit of the previous stage is rendered conductive in order to render the transistor Q_{67} non-conductive. On the other hand, if the transistor Q_{67}

constituting the inverter circuit of the subsequent stage is conductive in response to the input signal, the feedback diode D_8 is rendered conductive, whereas the feedback input transistor Q_{64} is rendered non-conductive. As a result, the latching operation is such that the transistor Q_{66} constituting the inverter circuit of the previous stage is rendered non-conductive in order to render the transistor Q_{67} conductive.

In the underflow master latch circuit 6, owing to the provision of the gate circuit 7, when the external terminal L is at zero volts, the diode D_{11} is always rendered conductive in order to render non-conductive the transistor Q_{74} constituting the inverter circuit of the subsequent stage so that the output is always at the low level irrespective of the detection of the underflow in order to interrupt the underflow detecting function.

The necessity for this function will be described later.

A code converting circuit 4 comprises a TTL circuit using multi-emitter transistors.

Multi-emitter transistors Q_{78} to Q_{85} and
5 transistors Q_{85} to Q_{92} prepare the lowest bit signal 2^0
of binary code in response to the Gray code signals A and
 $\bar{A}$ to D and $\bar{D}$. Multi-emitter transistors Q_{93} to Q_{96}
and transistors Q_{97} to Q_{100} prepare the second bit
signal 2^1 in response to the Gray code signals B and $\bar{B}$
10 to D and $\bar{D}$. Multi-emitter transistors Q_{101} and Q_{102}
and transistors Q_{103} and Q_{104} prepare the third bit
signal 2^2 in response to the Gray code signals C and $\bar{C}$
to D and $\bar{D}$. A multi-emitter transistor Q_{105} and a
transistor Q_{106} transmit the Gray code signal D as the
15 highest bit signal 2^3 of binary code.

The multi-emitter transistors are fed with not
only the Gray code signals but also the gate signal CP'
at their emitter electrodes which constitute the gate
input terminals.

20 When the external terminal L/^{is} at zero volts or
when the external terminal L is at V_{CC} and no underflow
detection is performed, the transistor Q_{74} constituting
the inverter circuit of the subsequent stage is non-
conductive so that the clock pulses $\overline{CP}$ are fed out through

the transistors Q_{75} and Q_{76} . On the other hand, only whilst the clock pulses CP are at the high level, the gate signal CP' at the high level effects the code converting operation of the code converting circuit 4.

5 Moreover, in the case where the external terminal L is at V_{CC} and during the underflow detection for $V_L > V_{IN}$, the transistors Q_{69} , Q_{72} and Q_{73} constituting the underflow master latch circuit 6 are rendered non-conductive, whereas the transistor Q_{74} is rendered
10 conductive so that a transistor Q_{77} is rendered conductive to set the gate signal CP' at the low level. As a result, all of the multi-emitter transistors are rendered conductive to raise all the binary code conversion outputs to the high level.

15 A slave latch circuit 4a, which is receptive of the lowest bit signal 2^0 of binary code, comprises: a multi-emitter transistor Q_{109} ; a feedback transistor Q_{110} made receptive of the output of the former transistor; load resistors R_{55} and R_{56} connected with
20 the collector and emitter electrodes of the feedback transistor, respectively; a transistor Q_{111} made receptive of the collector output; load resistors R_{57} and R_{58} connected with the collector and emitter electrodes of the transistor Q_{111} ; and a transistor Q_{112} made

receptive of the emitter output for feeding back the inverted output through the multi-emitter transistor Q_{109} .

A transistor Q_{113} , which is receptive of the emitter output of the transistor Q_{110} , is an output transistor and thus forms an open collector output circuit having its collector electrode connected with an external terminal Q.

The operation of the slave latch circuit 4a is performed such that when the clock pulses CP are at the low level the multi-emitter transistor Q_{109} is rendered conductive to render the feedback transistor Q_{110} non-conductive. As a result, the transistor Q_{111} is rendered conductive and non-conductive in accordance with the code conversion output, thus performing the reception of the code conversion output. Moreover, when the clock pulses CP are at the high level, the ON/OFF outputs of the transistor Q_{111} are positively fed back through the transistor Q_{112} , the multi-emitter transistor Q_{109} and the transistor Q_{110} in order to effect the latching operations.

It should be noted that the operation of introducing the inputs into the master latch circuit are carried out during the former half period when the clock pulses CP are at the high level, whilst the operation of introducing the code-converted inputs into

the slave latch circuits are carried out during the latter half period when the clock pulses CP are at the low level.

The reason why the data transfer is performed by the use of the clock pulses will now be explained.

5 For $V_{IN} \div V_8$, for example, as shown in Figure 7, the Gray code D indicates an intermediate level to judge that, in the TTL circuits for the code converting operations, the circuits for preparing the 2^0 , 2^1 and 2^2 signals are at the high level whereas the circuit for
10 preparing the 2^3 signal is at the low level. Then, the erroneous operations of "0", "0", "0" and "0" as the binary code take place. Therefore, the sampling operation is performed by the master latch circuit at the above referred to instants.

15 It should be noted that Figure 7 shows the waveforms in the case where the external terminal L is at the V_{CC} level. Upon underflow detection, the outputs 2^0 to 2^3 are set at the high level. If the external terminal L is at zero volts, the underflow output and
20 the outputs 2^0 to 2^3 do not vary, as indicated at broken lines in Figure 7.

The circuits of the other slave latch circuits $3b$ to $3d$ and 8 and their operations are similar to those of the slave latch circuit described above.

A bias circuit 10a is provided for driving constant current transistors which constitute constant current circuits I_{01} to I_{016} arranged in the comparator. In order to prevent erroneous operation due to noise, capacitors are connected to the external terminals G and H in order to reduce the impedance of the bias voltage output.

A bias circuit 10b is used to drive the constant current transistors which constitute the constant current circuits I_{017} to I_{063} arranged in the level conversion circuit, the master latch circuit, the code conversion circuit, the slave latch circuit and so on.

The comparator thus directly prepares the digital output signals A and $\bar{A}$ to D and $\bar{D}$ of Gray code and of opposite phases.

As a result, the Gray code signals of high gain can be generated with the use of a remarkably simple circuit including the differential transistor circuits for amplifying those outputs.

In the case where the two-stage differential transistor circuits are used to constitute the comparator, the prior art requires $2(2^n - 1)$ differential transistor circuits and complex code conversion circuits when the digital signals of n bits are to be prepared. On the

other hand, the circuits shown in Figures 2, 4 and 6 simplify the circuit construction and reduce the power consumption since they consist of $(2^n - 1) + n$ differential transistor circuits when the digital signals of n bits are to be prepared. Moreover the number of the resistors can be reduced because many of the $2^n - 1$ differential transistors have their collector electrodes commonly connected with each other and with the load resistors, so that the code conversion circuit can make use of simple emitter-follower circuits.

Furthermore, in the case where the digital outputs of Gray code are to be generated, such a sampling as is employed to generate the digital outputs of binary code can be made unnecessary, so that high-speed operation can be realized.

It is also possible to reduce the chip size of the monolithic IC and to enlarge the allowability for dispersion in the input threshold at the comparators.

In a modified form, it should be possible to dispense with the amplification stage circuits in the case where steep switching characteristics are not required. Even in this case, the circuit construction can be simplified, so that the digital signals of predetermined code can be easily prepared, and also that the chip size

can be reduced for the manufacture of the monolithic IC.

Moreover, the common connection of the collector electrodes should not ^{be} ^{ed} limit_{ed} to that between the different comparators but can be effected between two or more comparators. In this modification, the collector junction capacity is increased so that the switching speed is lowered. Such modification is not required in the case where the quasi-decimal code or Gray code signals are to be generated.

The above described circuits can be further modified such that the constant current sources are replaced by resistors.

On the other hand, the A/D converter shown in Figures 6A and 6B can enjoy the following features because it has both the underflow detection output function and the function to set the output at a predetermined level in accordance with that detection output.

Since the A/D converter is formed as a monolithic or hybrid IC, and its circuit construction is therefore fixed, it is inconvenient to extend the output bits. Nevertheless, the A/D converter can perform the output extension with remarkable ease.

Referring now to a second embodiment of the A/D

converter shown in Figure 8, it will be noted that the parts enclosed within broken lines are constructed into either a monolithic semiconductor integrated circuit or a hybrid integrated circuit. Reference letters enclosed by circles indicate the terminals of the integrated circuit.

The A/D converter includes a comparator 1 which is operative to compare the reference voltages prepared by uniformly dividing the lowest voltage V_L supplied to the terminal B and the highest voltage V_H supplied to the terminal F by means of series resistors R_0 to R_{16} with the analog voltage signal V_{IN} fed from the terminal A. This comparator is equipped with an underflow detecting comparator for detecting the analog input signal V_{IN} lower than the lowest voltage V_L .

The A/D converter further includes an output circuit 2 for supplying the output of the comparator 1 as a digital signal of Gray code; a master latch circuit 3 for receiving the digital signals of Gray code from the output circuit 2 in synchronism at a first time; a code conversion circuit 4 for converting the digital signals of Gray code received by the master latch circuit 3 into digital signals of binary code; a slave latch circuit 5 for receiving the digital signals of binary code

converted by the code conversion circuit 4 in synchronism at a second time; an underflow master latch circuit 6 for receiving the underflow detection signals UF of the comparator 1 in synchronism at the first time; a gate circuit 7 for controlling whether or not the underflow signal from the master latch circuit 6 is to be transmitted to a slave latch circuit 8 at the output side in accordance with the control signal (at 0 V or V_{CC}) from the terminal L and whether or not the output binary code to be performed at the code conversion circuit 4 is fixed in accordance with the underflow signal.

The slave latch circuit 8 receives the underflow signal in synchronism with the second timing and feeds the underflow signal UF out of the terminal M.

The A/D converter further includes a circuit 9 for shaping the waveforms of the clock pulses $\overline{CP}$ fed from the terminal K in order to supply the inverted clock pulses CP to the master latch circuits 3 and 6 and the slave latch circuits 5 and 8. The master latch circuits 3 and 6 receive the input signals by using the former half period of the clock pulses as the first timing, whereas the slave latch circuits 5 and 8 receive the input signals by using the latter half period of the clock pulses as the second timing.

A bias circuit 10 is provided for preparing the bias voltage which drives the constant current transistors constituting the comparator 1, the output circuit 2, the latch circuits, the conversion circuit 4 and so on.

A capacitor C connected between terminals H and G is used to stabilize the bias voltage.

The terminals C, D and E, which are connected with the respective intermediate points between the series resistors for preparing the reference voltages of the comparator 1, are used to measure whether or not the reference voltages are accurately prepared, and may be dispensed with .

Figures 9A and 9B are detailed circuit diagrams showing the four-bit A/D converter shown in Figure 8 in greater detail. The parts enclosed by broken lines are formed in the monolithic IC, and the circuit block numbers and the terminal symbols are made to correspond to those of the embodiment of Figures 6A and 6B.

The construction and operation of the circuit shown in Figures 9A and 9B are substantially the same as those of the circuit already described with reference to Figures 6A and 6B, and their detailed explanations are accordingly omitted.

Figure 10 is a block diagram showing one embodiment of an output extending system of the A/D converter.

Reference symbols IC_1 and IC_2 indicate two A/D converters having the same construction as that shown in Figures 9A and 9B.

The external terminal B of the A/D converter IC_1 is fed with the lowest voltage V_L . The external terminal F, which is the highest voltage terminal of the A/D converter IC_1 , is connected to the external terminal B which is the lowest voltage terminal of the other A/D converter IC_2 . The external terminal F of the A/D converter IC_2 is fed with the highest voltage V_H . As a result, the internal reference voltages of the A/D converters IC_1 and IC_2 are divided one thirty-second into the reference voltages, an intermediate voltage V_M is prepared at the connecting terminals F and B therebetween.

Therefore, the A/D converter IC_1 takes its share in the voltage range V_L to V_M , whereas the A/D converter IC_2 takes its share in the voltage range V_M to V_H .

The analog input voltage V_{IN} is commonly fed to the external terminals A of the A/D converters IC_1 and IC_2 .

On the other hand, the clock pulses $\overline{CP}$ are

commonly fed to the external terminals K of the A/D converters IC_1 and IC_2 .

5 The output terminals Q to N of the A/D converters IC_1 and IC_2 are commonly connected with their partners and with load resistors, respectively. In short, a wired AND circuit is constructed.

The external terminal L of the A/D converter IC_1 is at zero volts so that the underflow detecting operation is prohibited.

10 On the other hand, the external terminal L of the A/D converter IC_2 is fed with V_{CC} so that the underflow detecting operation is performed.

15 On the other hand, the external terminals I of the A/D converters IC_1 and IC_2 are supplied with the power source voltage V_{CC} , whereas the external terminals G and J of the same are earthed. Moreover, the external terminals H are connected to capacitors C, respectively.

20 The underflow signal, which is fed out of the external terminal M of the A/D converter IC_2 , is used as an extension bit signal 2^4 .

It should be noted that for the analog voltage V_{IN} within a range $V_L > V_{IN} > V_M$, the underflow detection circuit of the A/D converter IC_2 operates to lower its detected output UF to the low level, as shown in Figure 7,

and to raise the outputs 2^0 to 2^3 to the high level.

As a result, the output by the wired AND has its level depending upon the outputs 2^0 to 2^3 of the A/D converter IC_1 , and the underflow output UF at the low level is generated as the output 2^4 so that the output signals 2^0 to 2^4 of extended binary code can be generated.

For the analog voltage V_{IN} within a range $V_M > V_{IN} > V_H$, on the other hand, the outputs 2^0 to 2^3 of the A/D converter IC_1 automatically take the high level, as shown in Figure 7, whereas the outputs 2^0 to 2^3 by the wired AND are released from the high level of the output as the result of the underflow detection so that the level depending upon the outputs 2^0 to 2^3 of the A/D converter IC_2 is fed out. On the other hand, the underflow output of the A/D converter IC_2 is varied at the high level, as shown in Figure 7, so that the extended binary code output signals 2^0 to 2^4 can be generated.

The reason why the underflow detecting operation of the A/D converter IC_1 is prohibited will now be described. In the case where the lower voltage range is shared (or in the case where the A/D converter IC_1 is used as a single A/D converter), as has been described hereinbefore, the setting of the outputs 2^0 to 2^3 at the high level for $V_{IN} < V_L$ would invite erroneous operation

so that the outputs become "1", "1", "1" and "1" for the
 V_{IN} V_L .

Referring now to Figure 11, the A/D converters
 IC_1 and IC_2 have the function to raise the outputs 2^0 to
5 2^4 from the overflow detecting output circuit and the
external terminals L to the high level.

For example, the overflow detecting output
circuit feeds the high level out of the external terminals
M during the overflow and is constructed by equipping the
10 circuit shown in Figures 9A and 9B with the comparator,
which uses the voltage at the terminals F as the
reference voltage, and master and slave latch circuits.

On the other hand, the external terminal L
prohibits the operations of the code conversion circuit
15 of the circuit shown in Figures 9A and 9B, for example,
when it is at the low level, in order to raise the
outputs 2^0 to 2^3 to the high level.

The A/D converters IC_1 and IC_2 thus constructed
are connected in a similar manner to the one shown in
20 Figure 10. Incidentally, the overflow output terminal M
of the A/D converter IC_1 is connected to the external
terminal L of another A/D converter IC_2 so that the
overflow output of the A/D converter IC_1 is used at the
extension bit signal 2^4 . On the other hand, the external

terminal L of the A/D converter IC_1 is fixed at the high level in order to prohibit the high level operation of the outputs 2^0 to 2^3 .

5 It should be noted that if the analog voltage V_{IN} is lower than V_M , the overflow output of the A/D converter IC_1 is at the low level in order to set the extension output bit signal 2^4 at the low level and the external terminal L of the A/D converter IC_2 at the low level so that the outputs 2^0 to 2^3 of the A/D converter
10 IC_2 are raised to the high level.

As a result, the outputs 2^0 to 2^3 by the wired AND are set at the level depending upon the outputs 2^0 to 2^3 of the A/D converter IC_1 similarly to the one shown in Figure 10, so that the extended binary code signals
15 2^0 to 2^4 can be generated.

When the analog voltage V_{IN} is expressed by an inequality $V_M > V_{IN} > V_H$, on the other hand, the outputs 2^0 to 2^3 of the A/D converter IC_1 are automatically raised to the high level, and the overflow output is raised to
20 the high level. As a result, the output high level of the A/D converter IC_2 is released to effect the A/D conversion.

As a result, the outputs 2^0 to 2^3 by the wired AND are set at the level depending upon the outputs 2^0 to

2³ of an A/D converter IC₂ similarly to the one shown in Figure 10, so that the extended binary code signals 2⁰ to 2⁴ can be generated together with the overflow outputs at the high level.

5 The embodiment shown in Figure 12 corresponds to the case, in which the extensions of four times are performed by the use of the four A/D converters IC₁ to IC₄ shown in Figures 9A and 9B.

10 The connecting method of the A/D converters IC₁ and IC₂ in this embodiment is basically similar to that of the embodiment shown in Figure 11, and its repeated explanation is omitted here.

15 In order to prepare the extended output signals 2⁴ and 2⁵, the underflow signals of the A/D converters IC₂, IC₃ and IC₄ are consecutively raised to the high level such that $V_{IN} > \frac{1}{4}(V_H - V_L)$, $V_{IN} > V_M$ and $V_{IN} > \frac{3}{4}(V_H - V_L)$ so that the extended output 2⁴ is prepared by gate circuits G₁ and G₂. As the extended output 2⁵, on the other hand, the underflow output of the A/D converter IC₃, which is at the high level for $V_{IN} > V_M$, can be
20 utilized as it is.

 The gate circuits G₁ and G₂ raise the output 2⁴ to the high level for $\frac{1}{4}(V_H - V_L) < V_{IN} < V_M$ because the output of the A/D converter IC₂ is at the high level

(i.e., "1") whereas the others are at the low level (i.e., "0"). Next, for $V_M < V_{IN} < \frac{3}{4}(V_H - V_L)$, the output 2^4 is lowered to the low level because the outputs of the A/D converters IC_2 and IC_3 are at the high level whereas the others are at the low level.

For $V_{IN} > \frac{3}{4}(V_H - V_L)$, moreover, all the outputs of the A/D converters IC_2 to IC_4 are at the high level so that the output 2^4 can be raised again to the high level.

As a result, the extended binary code signals 2^0 to 2^5 can be generated.

As has been described above, the A/D converters constructed as integrated circuit devices are made to additionally have the underflow detecting output function and the function to forcibly set the outputs to a predetermined level in accordance with the underflow detection signals, or the overflow detecting output function and the function to forcibly set the outputs to a predetermined level in accordance with the signals from the external terminals, whereby the output bits can be easily extended. Especially, in the case where the output circuits comprise open-collector transistors and are forcibly turned off in accordance with the underflow detection signals or the signals from the outside in order to use the high level (i.e., the positive power source

voltage), the output bits can be extended by the use of the remarkably simple construction because the wired AND can be utilized.

Moreover, since the A/D converters described above have the underflow or overflow detecting output function, it can be used, too, for controlling the gain or D.C. voltage of a composite video signal amplifying circuit as the input analog signal source, in the case where the composite video signal in television broadcasting operation is subjected to an A/D conversion, such that the voltage level of a synchronizing signal may become coincident with the underflow or overflow detection output which is prepared by that A/D conversion.

Moreover, the above described A/D converters can have their differential and multi-emitter transistors formed in an identical device forming region when they are to be monolithically integrated, as shown in the embodiment of Figures 9A and 9B, because the differential transistors as the comparator have their collector electrodes commonly connected and because the multi-emitter transistors are used as the code conversion circuit.

As a result, a highly dense integration can be realized.

Still moreover, since the analog signals are converted by the comparator into the digital signals of the Gray code, the error at a switching intermediate point of the comparator is as small as ± 1 bit, and sampling is not required, as is different from the case in which the digital signals of binary code are to be directly prepared. As will be apparent from Figure 7, furthermore, the input threshold of the comparator becomes the alternate reference voltage under the lowest bit so that the allowability for dispersion can be enlarged. Furthermore, the frequency characteristics can be extended to twice the frequency range which is as high as the case in which the digital signals of binary code are to be directly generated.

Furthermore, since the comparators can prepare the signals $\bar{A}$ to $\bar{D}$ in opposite phases to those of the signals A to D in positive phase as the digital signals of the Gray code, it is possible to attain a large gain with the use of the simple circuit by amplifying the signals of opposite phases by means of the differential amplifying circuits.

Furthermore, upon the output extension, as shown in Figure 10 or 11, since no logic means is incorporated upon the interchange between the A/D converter for taking

its share in the lower voltage range and the A/D converter for taking its share in the higher voltage range, there arises no erroneous operation, and a high-speed operation can be realized.

5 The A/D converters may be constructed of hybrid ICs. On the other hand, the outputs of the comparators may be directly converted into the digital signals of binary code and may be fed out.

10 On the other hand, the output circuit may be constructed of the open-emitter transistors. In this modification, a wired OR may be used for the output extension. In this case in which the wired OR is used, it is convenient to forcibly render the output transistor non-conductive in accordance with the overflow detection
15 signal thereby to effect the low level.

 Furthermore, the output circuit may be constituted of a TTL circuit. In this case, it is necessary to provide an AND or OR circuit for the output extension.

Attention is drawn to our Divisional Application No. 83.25882 (Serial No. 2,126,815) in which there is claimed in claim 1, an integrated analog-to-digital (A/D) converter including:

- 5 (a) a comparator for comparing a plurality of reference voltages and an analog input signal and for producing a plurality of output signals as a result of the comparison;
- 10 (b) a code converter for converting the plural output signals of said comparator into digital signals of plural bits;
- 15 (c) a critical detecting comparator for comparing a critical reference voltage having a level outside the range of said plural reference voltages with the analog input signal thereby to feed out a detection output, which is separate from the plural bits, at a predetermined level in the case where said analog input signal exceeds said critical reference voltage;
- 20 (d) a control circuit for forcibly controlling the levels of said digital signals of the plural bits to a selected level, which is the same for all the plural bits, in the case where said detection output of said critical detecting comparator reaches said predetermined level;
- 25 (e) a first output circuit for feeding out said digital signals of the plural bits of said code converter to the plural output terminal of an integrated circuit; and
- 30 (f) a second output circuit for feeding out the detection output of said critical detecting comparator to another output terminal of said integrated circuit, wherein said control circuit has a control input terminal which is extracted as an external terminal from said integrated circuit so that the forced control operation is prohibited by supplying a control signal to said control input
- 35 terminal of said control circuit.



CLAIMS.

1. A parallel comparator including:

(a) a plurality of comparator portions each having first and second transistors differentially connected;

5 (b) an $(n-x)$ th comparator portion having first and second transistors differentially connected;

(c) an n th comparator portion having first and second transistors differentially connected; and

(d) an $(n+x)$ th comparator portion having first
10 and second transistors differentially connected; where n and x are positive integers, n is at least greater than $x+1$ and x is equal to 2 or greater than 2;

wherein said first transistors of said plurality of comparator portions, said $(n-x)$ th comparator portion, said
15 n th comparator portion and said $(n+x)$ th comparator portion have their base electrode supplied with an analog input signal whereas said second transistors of said above comparator portions have their base electrode supplied with reference voltage having different levels, wherein the
20 collector electrode of said second transistor of said $(n-x)$ th comparator portion and the collector electrode of said first transistor of said n th comparator portion are commonly connected $(n-x)$ load means, and wherein the collector electrode of said second transistor of said n
25 th comparator portion and the collector electrode of said first transistor of said $(n+x)$ th comparator portion are commonly connected to n th load means.



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2. A parallel comparator according to Claim 1, further including:

(e) an $(n-x)$ th amplifying transistor having its base electrode connected with said $(n-x)$ th load means;

5 (f) an n th amplifying transistor having its base electrode connected with said n th load means; and

(g) a constant current source commonly connected to the emitter electrode of said $(n-x)$ th amplifying transistor and the emitter electrode of said n th
10 amplifying transistor.

3. A parallel comparator according to claim 1, wherein $x=2$, wherein the collector electrode of said second transistor of said $(n-2)$ th comparator portion and the collector electrode of said first transistor of said
15 n th comparator portion are commonly connected with $(n-2)$ th load means, wherein the collector electrode of said second transistor of said $(n-1)$ th comparator portion and the collector electrode of said first transistor of said
20 $(n+1)$ th comparator portion are commonly connected with $(n-1)$ th load means; and wherein the collector electrode of said second transistor of said n th comparator portion and the collector electrode of said first transistor of said
 $(n+2)$ th comparator portion are commonly connected with
 n th load means.

25 4. A parallel comparator according to claim 3, further including:

(h) $(n+2)$ th load means connected with the collector electrode of said second transistor of said
 $(n+2)$ th comparator portion;



(i) an (n-2)th emitter-follower transistor having its base electrode connected with said (n-2)th load means;

(j) an (n+2)th emitter-follower transistor having its base electrode connected with said (n+2)th load means; and

(k) emitter load means commonly connected with the emitter electrode of said (n-2)th emitter-follower transistor and the emitter electrode of said (n+2)th emitter-follower transistor.

5. A parallel comparator having (n+x) comparator portions constructed and arranged to operate substantially as herein described with reference to and as illustrated in Figure 4; or Figures 6A and 6B; or Figures 9A and 9B of the accompanying drawings.
