aluminum or copper). The second chip passivation layer 65 may be formed of, for example, a silicon nitride layer or a polyimide layer. The second chip conductive pads 63 may be electrically connected through third internal connection terminals 44 to corresponding ones of the second substrate upper conductive patterns 33. The third internal connection terminals 44 may be solder balls, conductive bumps, conductive pillars, or any combination thereof. The third internal connection terminals 44 may include one or more of copper, tin, or lead. A third under-fill layer 46 may be interposed between the second semiconductor chip 60 and the second substrate 30. The second semiconductor chip 60 may include a second chip left-side wall 60sl adjacent to the first semiconductor chip 50 and a second chip right-side wall 60sr opposite to the second chip left-side wall 60sl. As shown in FIG. 1, the second semiconductor chip 60 may further include a second chip front-side wall 60sf that connects the second chip right-side wall 60sr to the second chip left-side wall 60sl at a front side of the second semiconductor chip 60, and a second chip back-side wall 60sb that is opposite to the second chip front-side wall 60sf and connects the second chip right-side wall 60sr to the second chip left-side wall 60sl at a back (or rear) side of the second semiconductor chip 60. The second semiconductor chip 60 may have a top

WHAT IS CLAIMED IS:

1. A semiconductor package, comprising:

a first substrate;

a first semiconductor structure mounted on the first substrate, the first semiconductor structure including a first sidewall and a second sidewall opposite to the first sidewall;

a second semiconductor structure mounted on the first substrate and spaced apart from the first semiconductor structure, the second semiconductor structure including a third sidewall adjacent to the first sidewall of the first semiconductor structure;

a heat sink covering at least portions of the first semiconductor structure, the second semiconductor structure, and the first substrate; and

a thermal interface material layer between the first semiconductor structure and the heat sink and between the second semiconductor structure and the heat sink, the thermal interface material layer including a first thermal interface material segment which is interposed between the first sidewall of the first semiconductor

structure and the third sidewall of the second semiconductor structure and a second thermal interface material segment that protrudes beyond the second sidewall, a first distance from a top surface of the first substrate to a lowest point of a bottom surface of the first thermal interface material segment being less than a second distance from the top surface of the first substrate to a lowest point of a bottom surface of the second thermal interface material segment;

a first under-fill layer between the first substrate and the first semiconductor structure,

wherein the first under-fill layer includes a first under-fill protrusion that protrudes beyond the first sidewall, and

wherein the first thermal interface material segment is spaced apart from the first under-fill protrusion; and

a second under-fill layer between the first substrate and the second semiconductor structure,

wherein the second under-fill layer includes a second under-fill protrusion that protrudes beyond the third sidewall, and

wherein the first thermal interface material segment is spaced apart from the second under-fill protrusion.

2. The semiconductor package of claim 1, wherein a third distance from the top surface of the first substrate to a highest point of an upper surface of the first under-fill protrusion is equal to or less than about 50% of a fourth distance from the top surface of the first substrate to a top surface of the first semiconductor structure.

3. The semiconductor package of claim 1 or claim 2, wherein

the second semiconductor structure includes,

a fourth sidewall opposite to the third sidewall,

the thermal interface material layer further includes a third thermal interface material segment that protrudes beyond the fourth sidewall, and

a fifth distance from the top surface of the first substrate to a lowest point of a bottom surface of the third thermal interface material segment is greater than the first distance.

4. The semiconductor package of claim 3, wherein the second under-fill protrusion is in contact with the first under-fill protrusion.

5. The semiconductor package of claim 3 or claim 4, wherein a sixth distance from the top surface of the first substrate to a highest point of an upper surface of the second under-fill protrusion is equal to or less than about 50% of a seventh distance from the top surface of the first substrate to a top surface of the second semiconductor structure.

6. The semiconductor package of any one of claims 3 to 5, wherein

the first and second semiconductor structures defines a gap region therebetween,

an upper end of the gap region corresponds to a lower one from among heights of top surfaces of the first and second semiconductor structures,

a lower end of the gap region corresponds to the top surface of the first substrate,

a first side of the gap region corresponds to the first sidewall,

a second side of the gap region, which is opposite to the first side of the gap region, corresponds to the third sidewall, and

a sum of volumes of the first thermal interface material segment, the first under-fill protrusion, and the second under-fill protrusion that are positioned in the gap region is equal to or less than about 90% of a total volume of the gap region.

7. The semiconductor package of claim 6, wherein

the gap region includes an empty space that is not occupied by the first thermal interface material segment, the first under-fill protrusion, and the second under-fill protrusion, and

a volume of the empty space is equal to or greater than about 10% of the total volume of the gap region.

8. The semiconductor package of any one of claims 1 to 7, further comprising:

a second substrate under the first substrate,

wherein the heat sink is attached to the second substrate.

9. The semiconductor package of claim 8, further comprising:

an adhesive layer between the heat sink and the second substrate,

wherein the adhesive layer includes a same material as the thermal interface material layer.

10. The semiconductor package of any one of claims 1 to 9, wherein each of the first and second semiconductor structures is one of a semiconductor chip or a sub-semiconductor package.

11. The semiconductor package of any one of claims 1 to 10, wherein a cross-section of the first thermal interface material segment has a profile having an inflection point at a lower surface thereof.

12. The semiconductor package of claim 11, wherein:

a top surface of the first semiconductor structure is lower than a top surface of the second semiconductor structure, and

the inflection point is nearer to the first semiconductor structure than to the second semiconductor structure.

13. The semiconductor package of any one of claims 1 to 9, wherein one of the first semiconductor structure or the second semiconductor structure includes a sub-package substrate and at least one semiconductor chip mounted on the sub-package substrate,

wherein the thermal interface material layer is in contact with a top surface of the semiconductor chip.

14. A semiconductor package, comprising:

a first substrate;

a first semiconductor structure mounted on the first substrate, the first semiconductor structure including a first sidewall and a second sidewall opposite to the first sidewall;

a second semiconductor structure mounted on the first substrate and spaced apart from the first semiconductor structure, the second semiconductor structure

including a third sidewall adjacent to the first sidewall of the first semiconductor structure;

a heat sink covering at least portions of the first semiconductor structure, the second semiconductor structure, and the first substrate; and

a thermal interface material layer between the first semiconductor structure and the heat sink and between the second semiconductor structure and the heat sink, the thermal interface material layer including a first thermal interface material segment which is interposed between the first sidewall of the first semiconductor structure and the third sidewall of the second semiconductor structure, a second thermal interface material segment adjacent to the second sidewall, and a fourth thermal interface material segment which is interposed vertically between the first thermal interface material segment and the heat sink, and a sum of the first thermal interface material segment and the fourth thermal interface material segment being thicker than the second thermal interface material segment;

a first under-fill layer between the first substrate and the first semiconductor structure, the first under-fill layer including a first under-fill protrusion that protrudes beyond the first sidewall,

wherein the first thermal interface material segment is spaced apart from the first under-fill protrusion; and

a second under-fill layer between the first substrate and the second semiconductor structure, the second under-fill layer including a second under-fill protrusion protruding beyond the third sidewall,

wherein the first thermal interface material segment is spaced apart from the second under-fill protrusion.

15. A semiconductor package, comprising:

a package substrate;

a first semiconductor structure and a second semiconductor structure mounted on the package substrate and spaced apart from each other in a direction parallel to a top surface of the package substrate;

a heat sink covering at least portions of the first semiconductor structure, the second semiconductor structure, and the package substrate; and

a thermal interface material layer between the first semiconductor structure and the heat sink and between the second semiconductor structure and the heat sink,

the thermal interface material layer having different thicknesses according to positions thereof, the thermal interface material layer having a greatest thickness at a position having a portion interposed between a first sidewall of the first semiconductor structure and a third sidewall of the second semiconductor structure, and the third sidewall being adjacent to the first sidewall; and

an interposer substrate between the package substrate and the first semiconductor structure and between the package substrate and the second semiconductor structure;

a first under-fill layer between the interposer substrate and the first semiconductor structure, the first under-fill layer protruding beyond the first sidewall of the first semiconductor structure; and

a second under-fill layer between the interposer substrate and the second semiconductor structure, the second under-fill layer protruding beyond the third sidewall of the second semiconductor structure,

wherein the thermal interface material layer is spaced apart from both the first and second under-fill layers.