

ABSTRACT

An information processing device according to an embodiment controls access from n (n being an integer equal to or greater than 2) MPUs to a shared memory. A control unit analyzes an access pattern to the shared memory based on access requests to the shared memory received in parallel from the n MPUs in a same access phase and sequentially processes, in the access phase, the received m (m being a natural number equal to or less than n) access requests in order based on the analyzed access pattern. Thus, irrespective of an increase in the number of master MPUs transmitting and receiving input/output data via a shared memory of an intelligent input/output device, the master MPUs can transmit and receive data without a decrease in effective processing speed.