ABSTRACT

Methods, systems, and apparatuses for redundancy in a memory array are described. A memory array may include some memory cells that are redundant to other memory cells of the array. Such redundant memory cells may be used if another memory cell is discovered to be defective in some way; for example, after the array is fabricated and before deployment, defects in portions of the array that affect certain memory cells may be identified. Memory cells may be designated as redundant cells for numerous other memory cells of the array so that a total number of redundant cells in the array is relatively small fraction of the total number of cells of the array. A configuration of switching components may allow redundant cells to be operated in a manner that supports redundancy for numerous other cells and may limit or disturbances to neighboring cells when accessing redundancy cells.