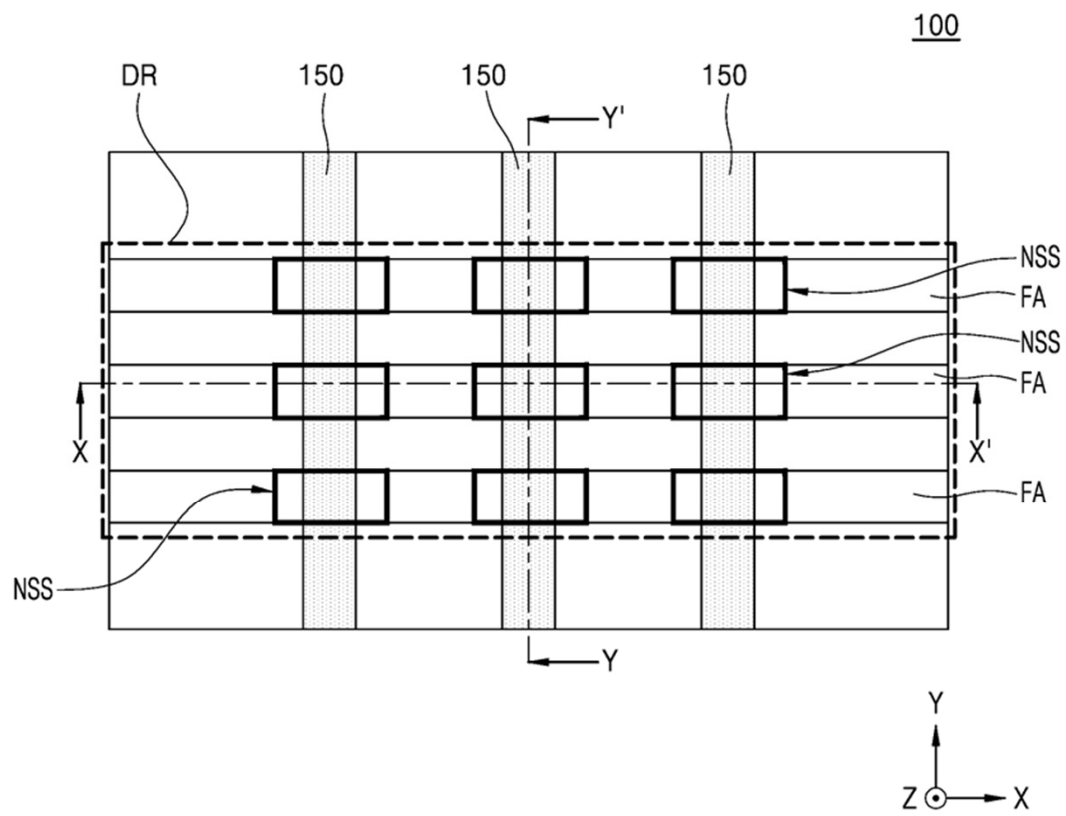


FIG. 1



[illegible]

FIG. 3

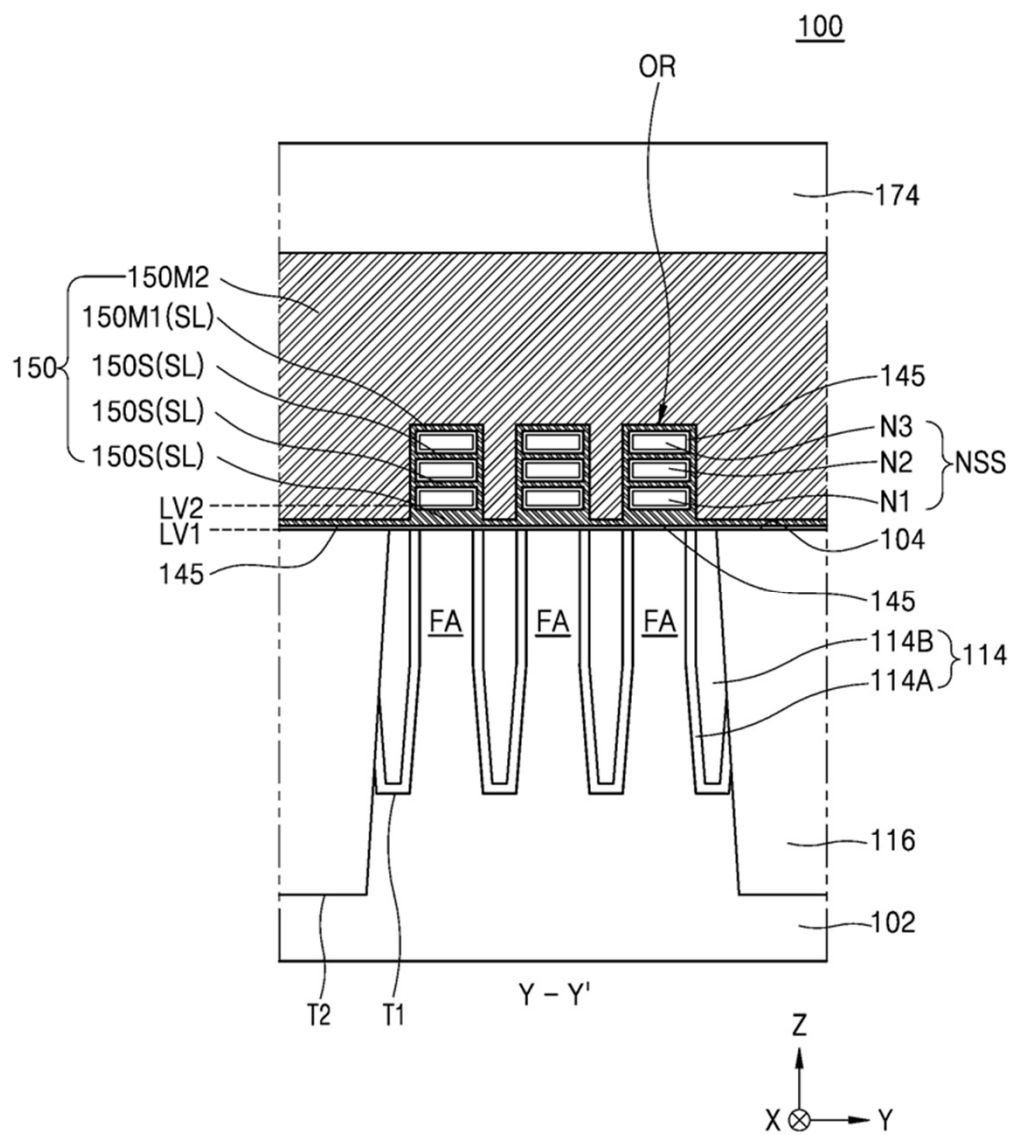


FIG. 4

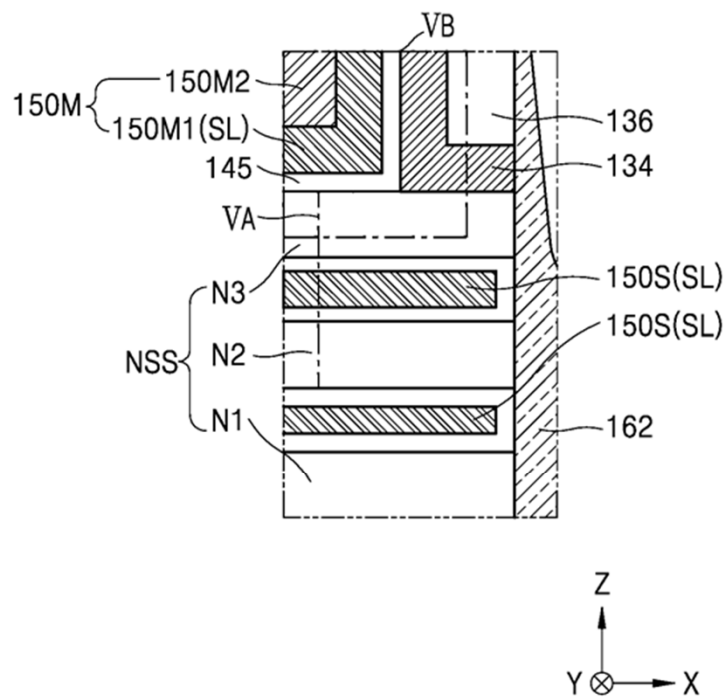


FIG. 5A

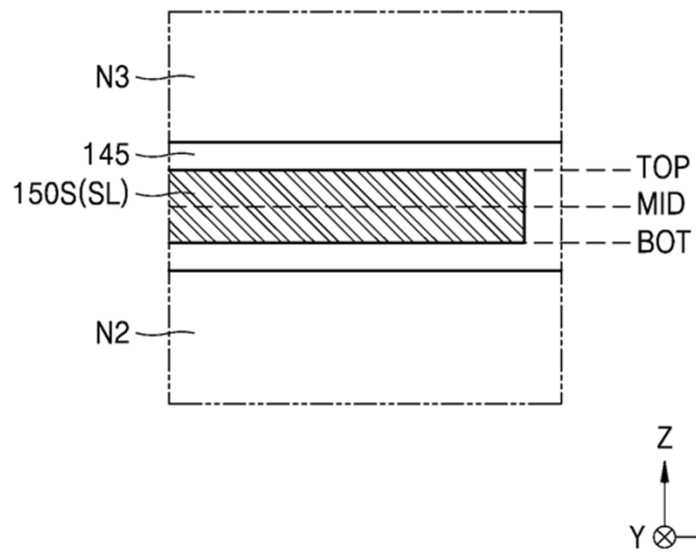


FIG. 5B

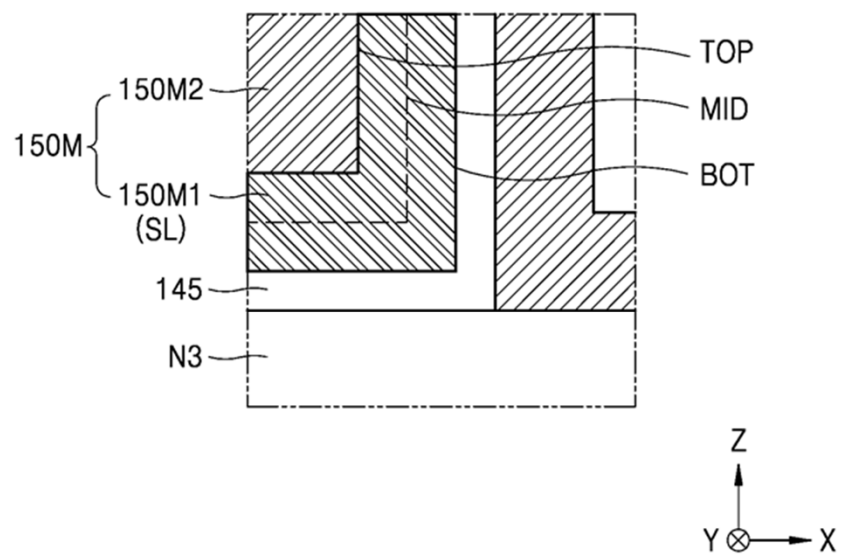


FIG. 6

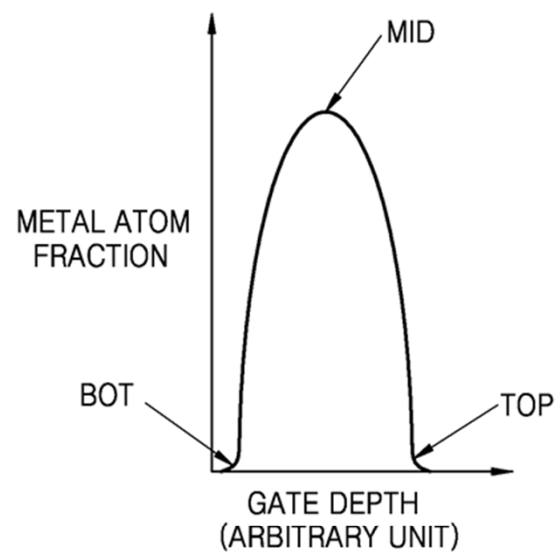


FIG. 7A

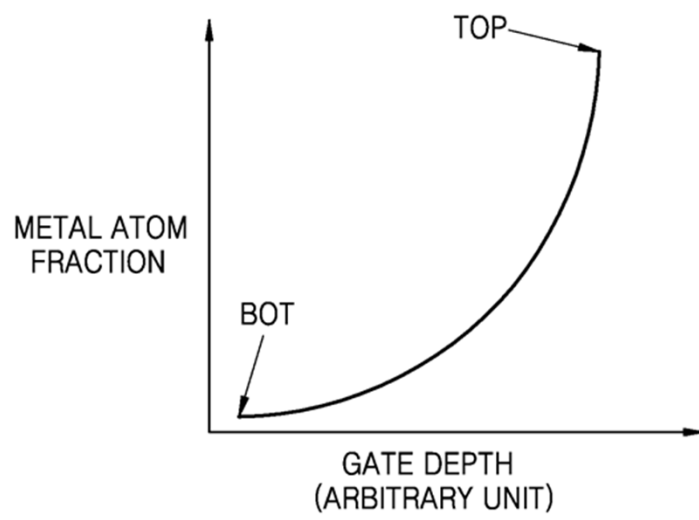


FIG. 7B

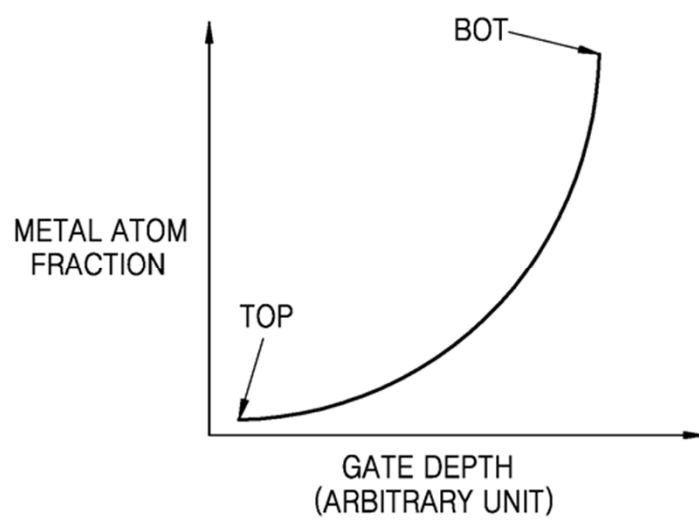


FIG. 8

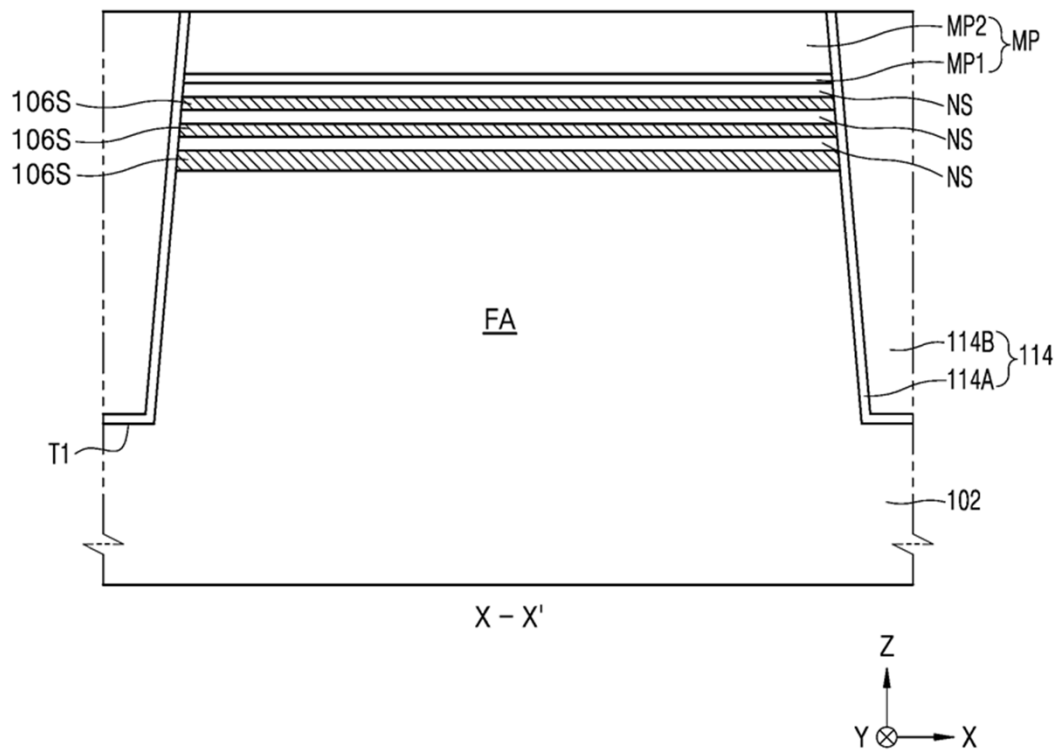


FIG. 9

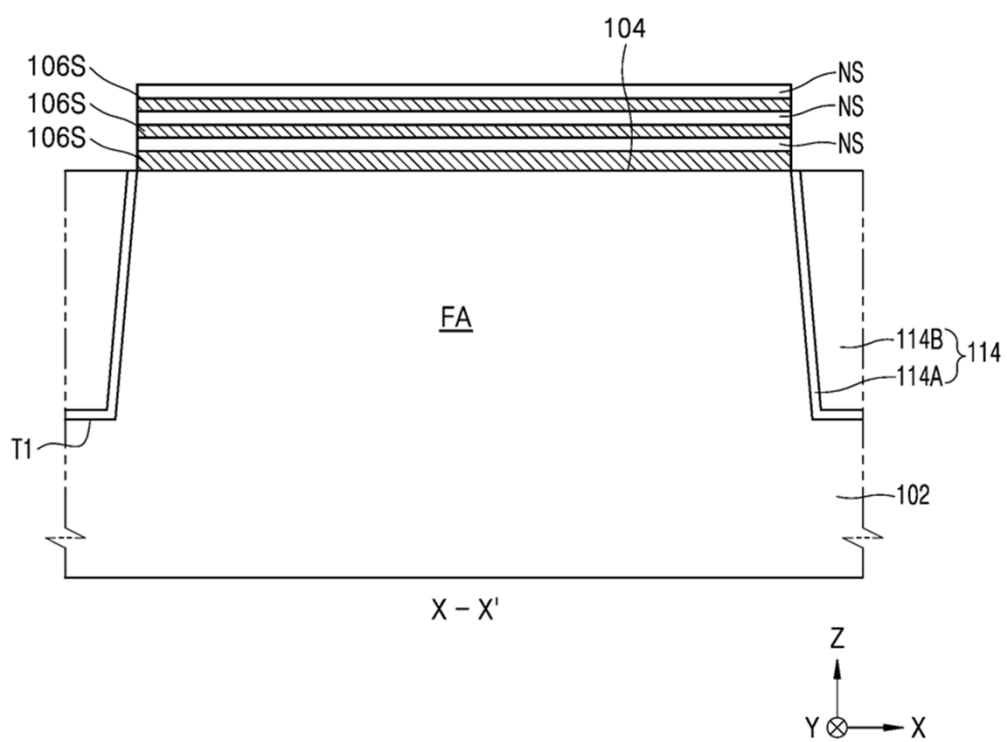


FIG. 10

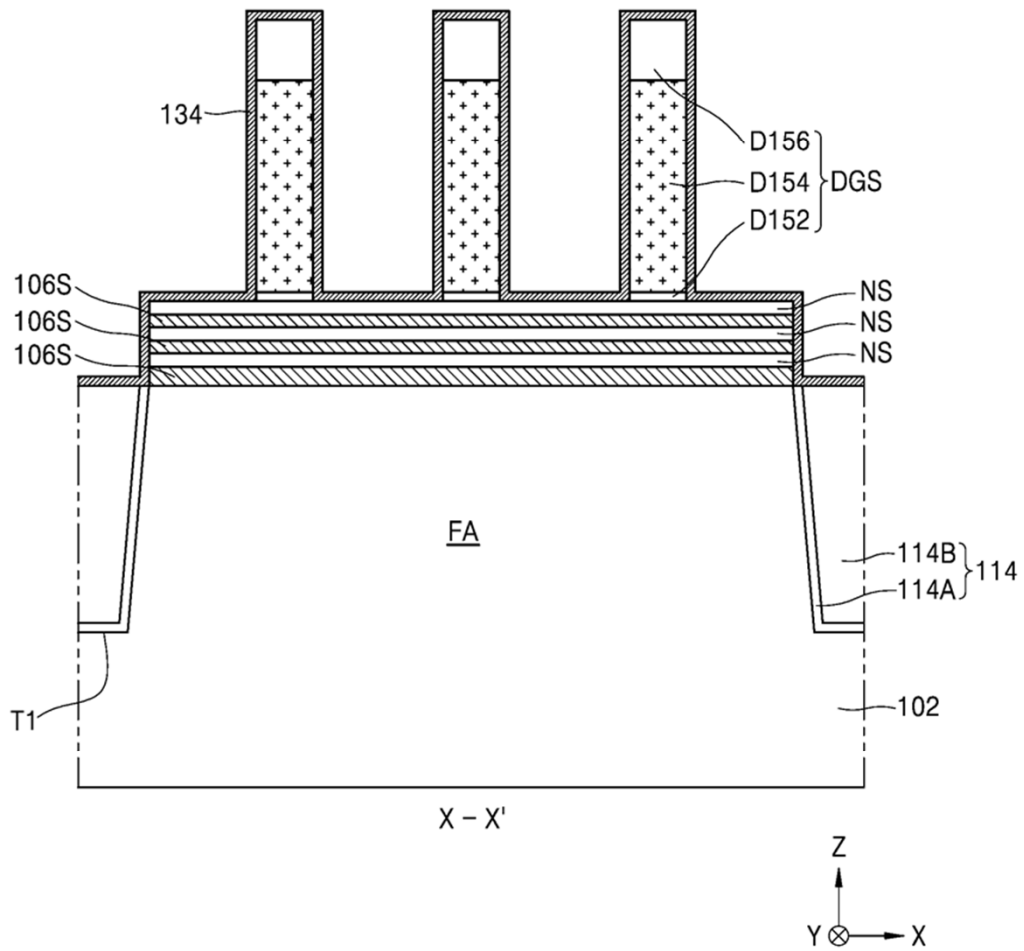


FIG. 11

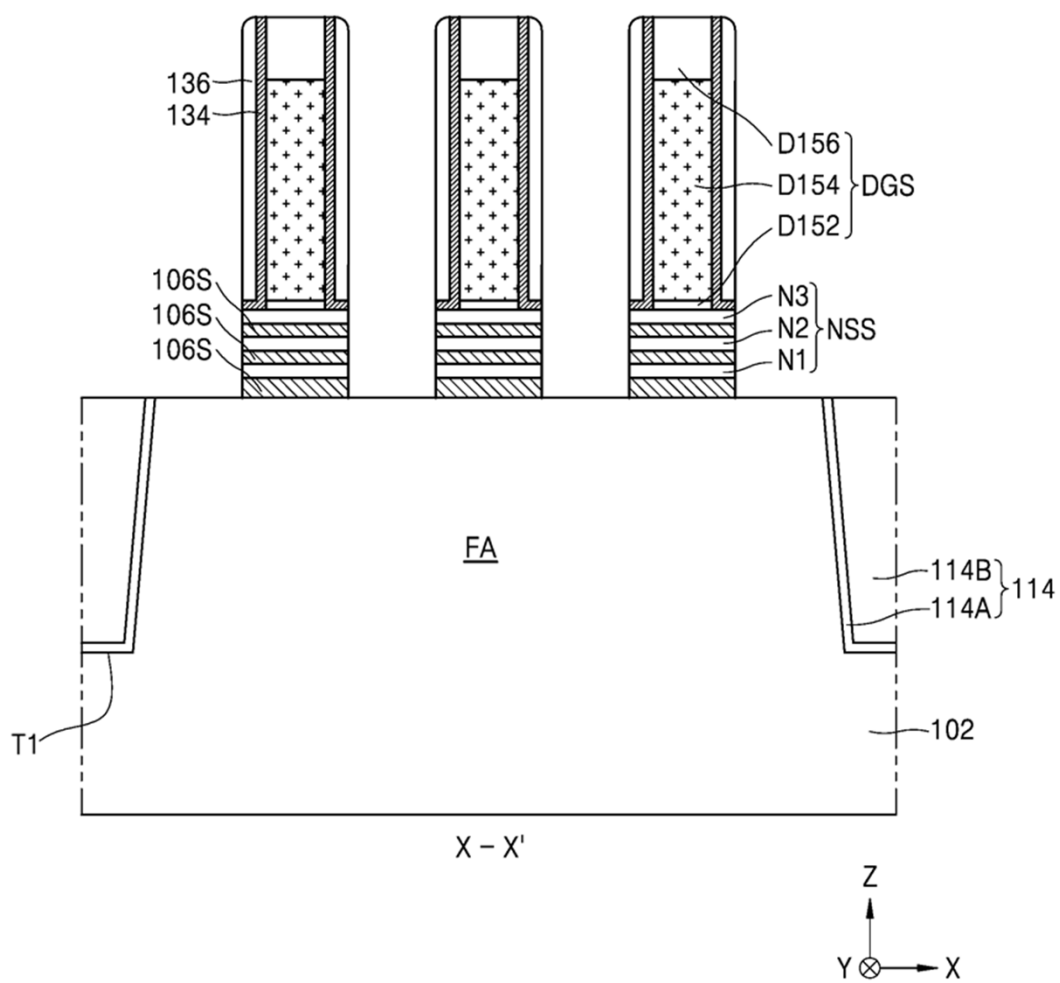


FIG. 12

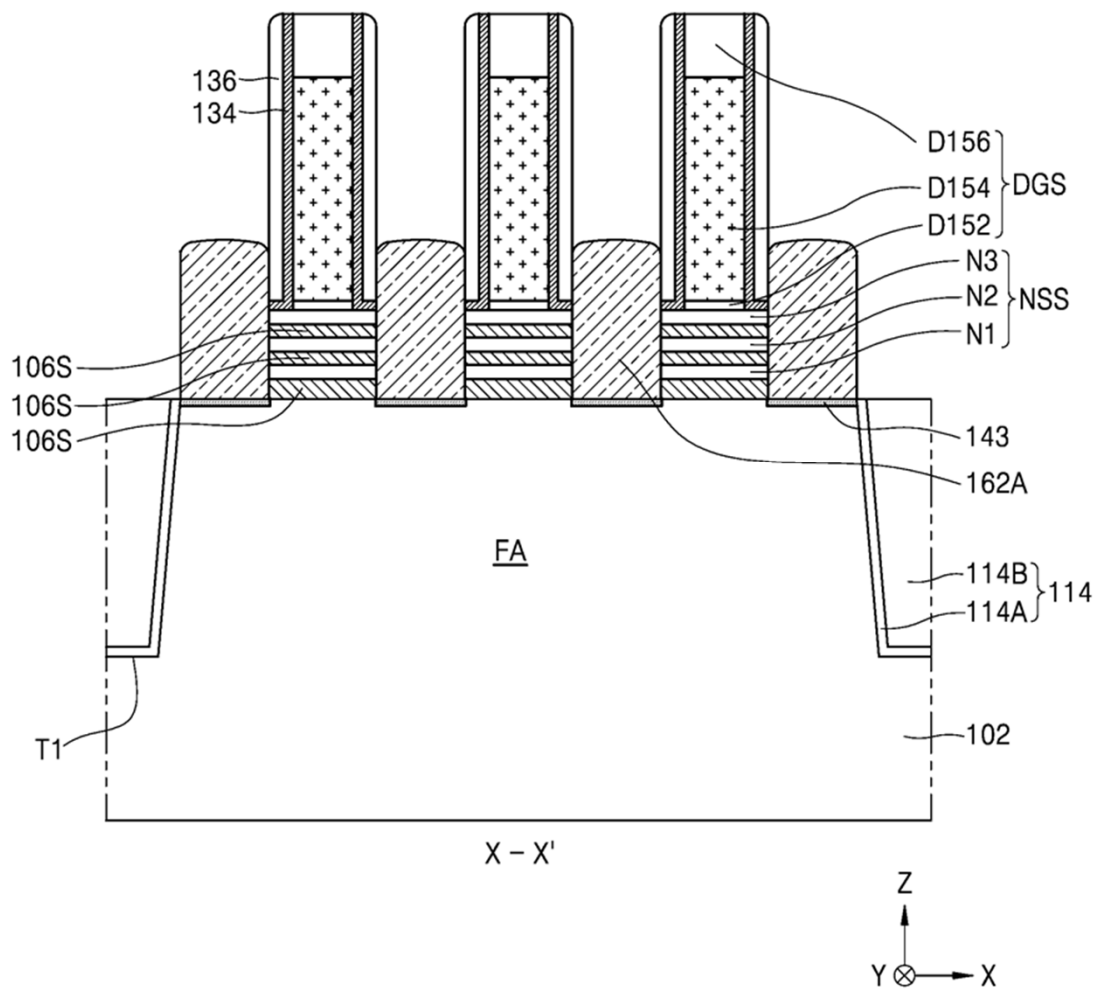


FIG. 13

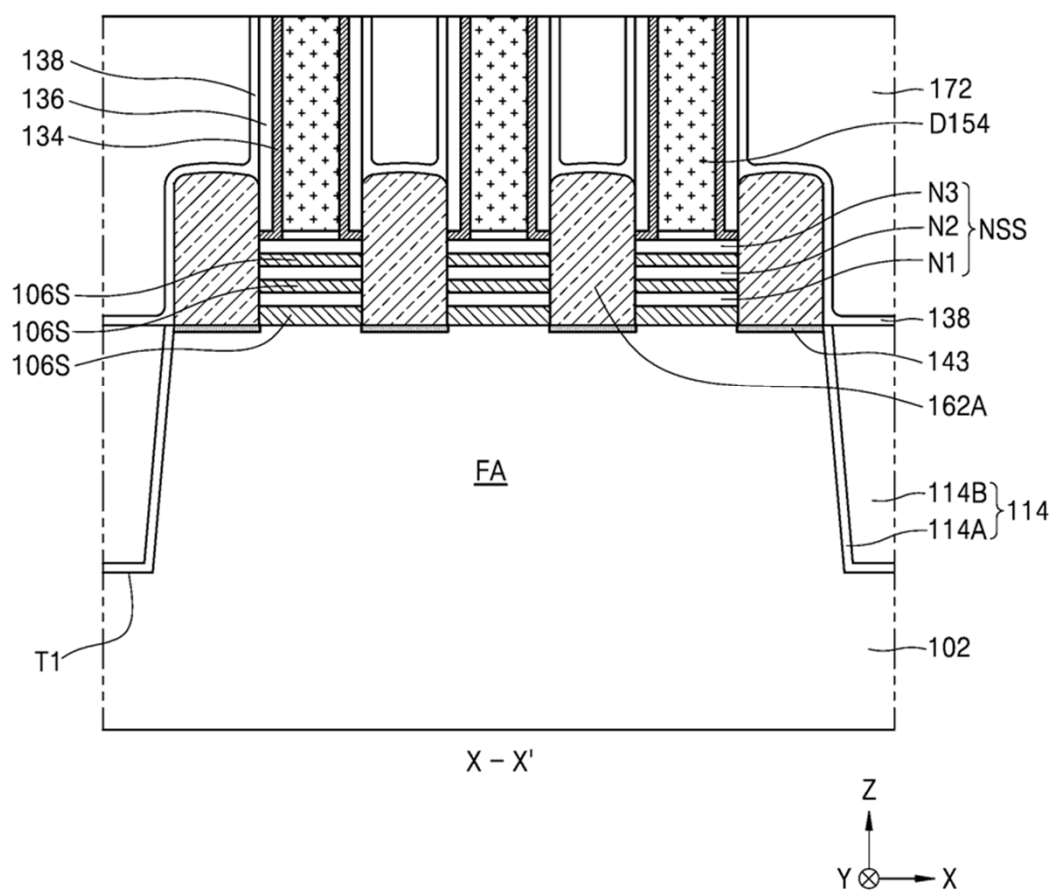


FIG. 14

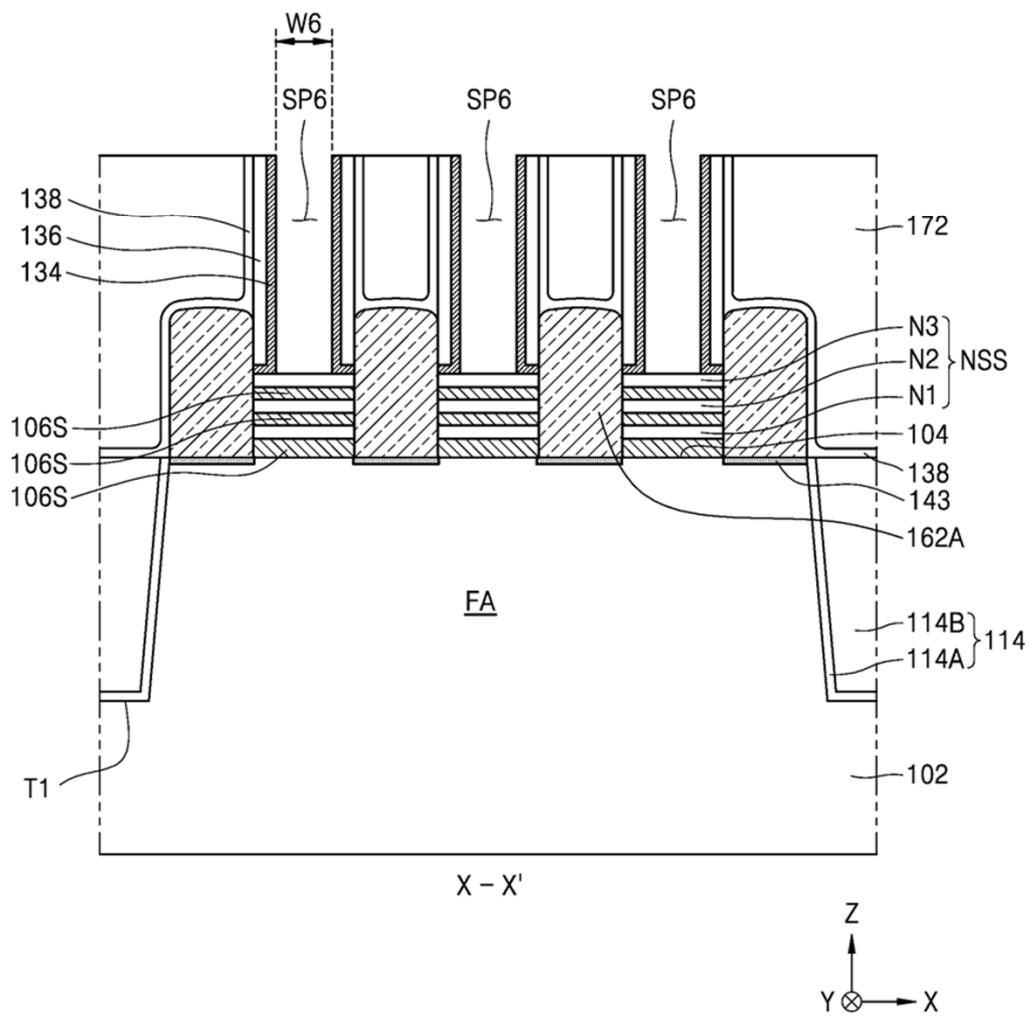


FIG. 15

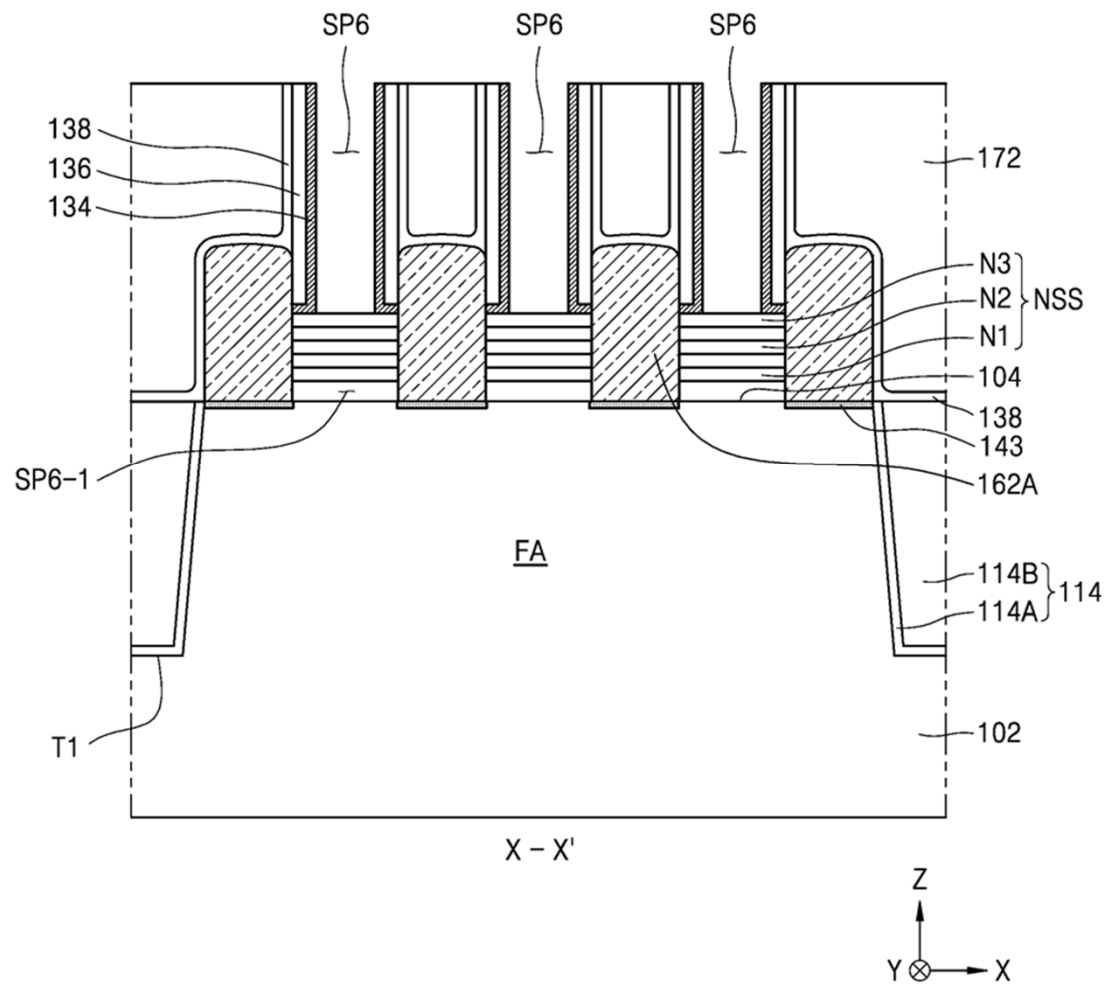


FIG. 16

This cross-sectional view shows a semiconductor device with a substrate 102. A gate stack 104 is formed on the substrate, consisting of a gate dielectric 138, a gate electrode 143, and a gate cap 162A. The gate stack is divided into three regions labeled N1, N2, and N3, collectively designated as NSS. On the left side, a series of layers are shown: 150M (comprising 150M1, 150M2, and 150M3), 150S(SL), 150S(SL), 150S(SL), 136, and 138. The central region is labeled 150. On the right side, a series of layers are shown: 114A, 114B, 114, 145, and 172. A dashed line X-X' indicates the plane of the cross-section. A coordinate system is shown in the bottom right corner with X, Y, and Z axes.

FIG. 17

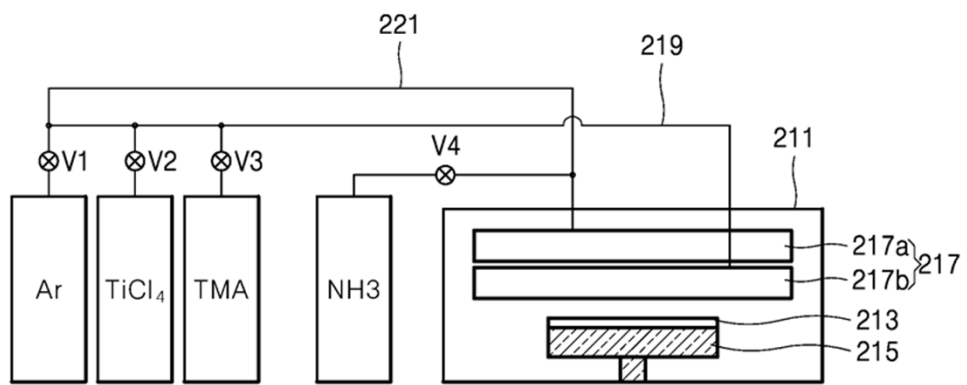


FIG. 18

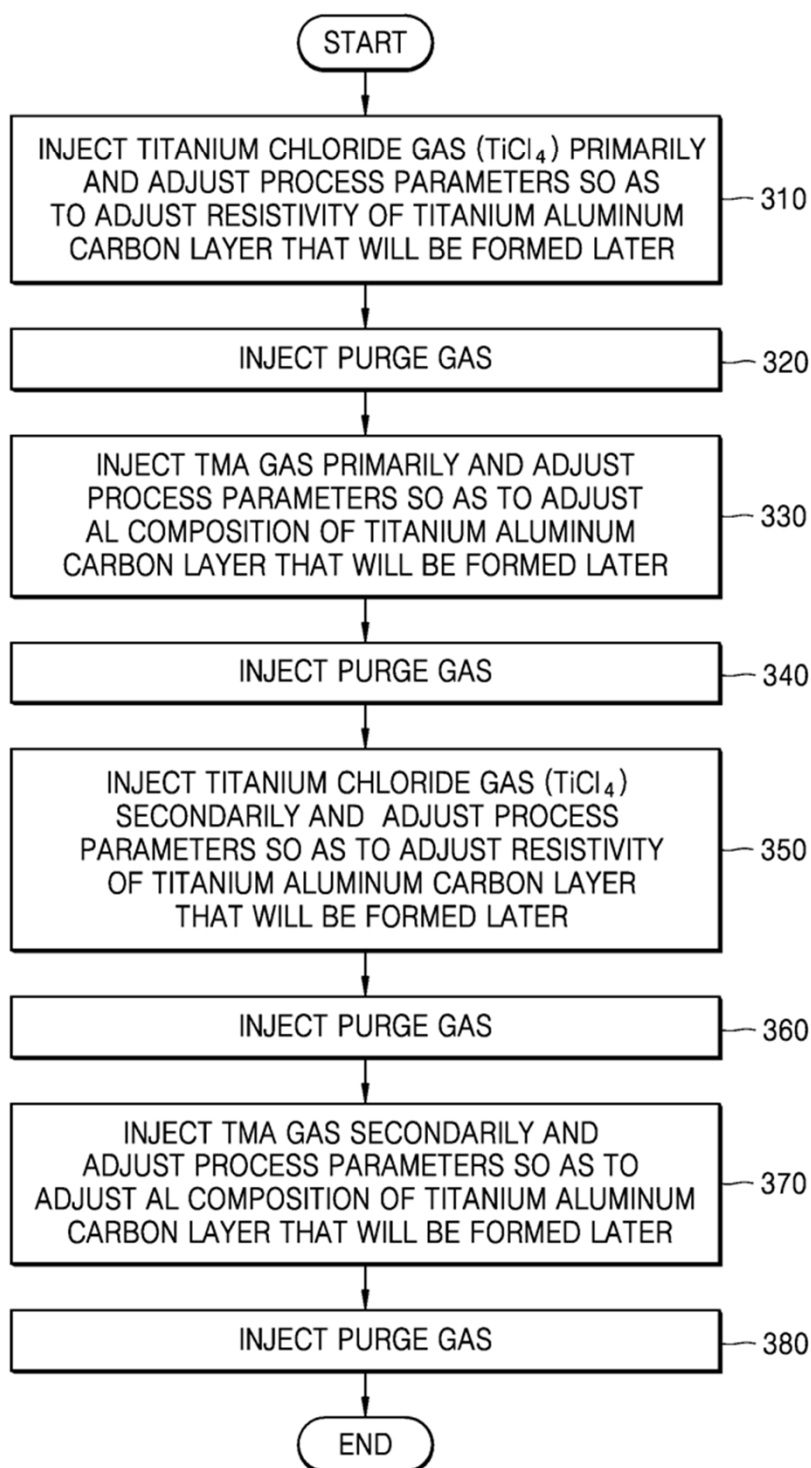


FIG. 19

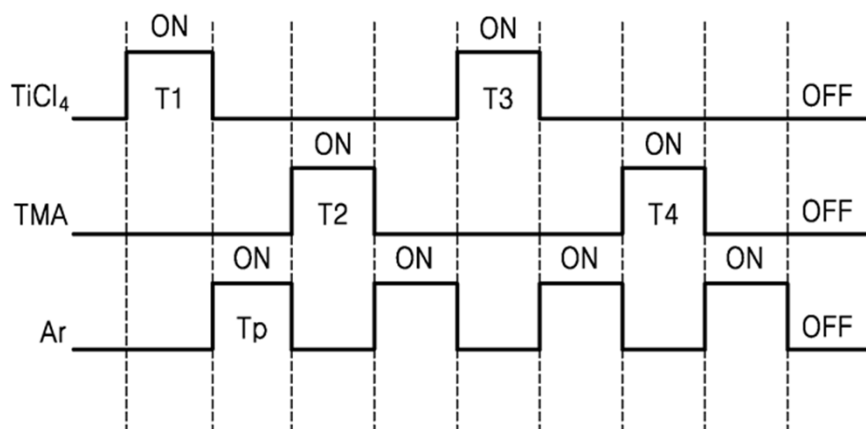


FIG. 20

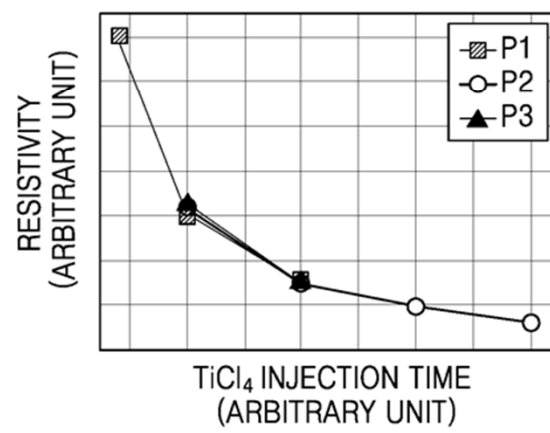


FIG. 21

