

DESCRIPTION

Title of Invention: METHOD FOR PRODUCING SEMICONDUCTOR
DEVICE AND SEMICONDUCTOR DEVICE

Technical Field

[0001]

The present invention relates to a method for producing
a semiconductor device and a semiconductor device.

Background Art

[0002]

The degree of integration of semiconductor integrated
circuits, in particular, integrated circuits using MOS
transistors has been increasing. With the increasing degree
of integration, the size of MOS transistors used in
integrated circuits has been decreased to nano-scale
dimensions. Such a decrease in the size of MOS transistors
causes difficulty in suppressing leak currents, which poses
a problem in that it is hard to reduce the area occupied by
the circuits because of the requirements of the secure
retention of necessary currents. To address the problem, a
surrounding gate transistor (hereinafter referred to as
"SGT") having a structure in which a source, a gate, and a
drain are disposed so as to be perpendicular to a substrate
and a gate electrode surrounds a pillar-shaped semiconductor
layer has been proposed (e.g., refer to PTL 1, PTL 2, and
PTL 3).

[0003]

In an existing method for producing an SGT, a silicon pillar on which a nitride film hard mask is formed in a pillar shape is formed, a diffusion layer is formed in a lower portion of the silicon pillar, a gate material is then deposited, the gate material is then planarized and etched back, and an insulating film sidewall is formed on the side wall of the silicon pillar and the nitride film hard mask. Subsequently, a resist pattern for forming a gate line is formed, the gate material is etched, the nitride film hard mask is then removed, and a diffusion layer is formed in an upper portion of the silicon pillar (e.g., refer to PTL 4).

[0004]

In such a method, when the distance between the silicon pillars is decreased, a thick gate material needs to be deposited between the silicon pillars and thus holes called voids may be formed between the silicon pillars. If voids are formed, holes are made in the gate material after the etching back. When an insulating film is then deposited to form an insulating film sidewall, the insulating film is deposited in the voids. This causes difficulty in gate material processing.

[0005]

In view of the foregoing, it has been disclosed that a silicon pillar is formed, a gate oxide film is then formed,

a thin polysilicon is deposited, a resist that covers an upper portion of the silicon pillar and is used to form a gate line is then formed, a gate line is etched, a thick oxide film is then deposited, the upper portion of the silicon pillar is caused to be exposed, the thin polysilicon on the upper portion of the silicon pillar is removed, and the thick oxide film is removed by wet etching (e.g., refer to NPL 1).

[0006]

However, a method in which a metal is used for gate electrodes is not described. In addition, a resist that covers an upper portion of the silicon pillar and is used to form a gate line needs to be formed. Therefore, the upper portion of the silicon pillar needs to be covered and thus such a method is not a self-aligned process.

Citation List

Patent Literature

[0007]

PTL 1: Japanese Unexamined Patent Application
Publication No. 2-71556

PTL 2: Japanese Unexamined Patent Application
Publication No. 2-188966

PTL 3: Japanese Unexamined Patent Application
Publication No. 3-145761

PTL 4: Japanese Unexamined Patent Application

Publication No. 2009-182317

Non Patent Literature

[0008]

NPL 1: B. Yang, K. D. Buddharaju, S. H. G. Teo, N. Singh, G. D. Lo, and D. L. Kwong, "Vertical Silicon-Nanowire Formation and Gate-All-Around MOSFET", IEEE Electron Device Letters, VOL. 29, No. 7, July 2008, pp 791-794.

Summary of Invention

Technical Problem

[0009]

It is an object of the present invention to provide a method for producing an SGT in which a thin gate material is used, a metal gate is employed, and a self-aligned process is performed and an SGT structure obtained by the method.

Solution to Problem

[0010]

A method for producing a semiconductor device according to the present invention includes a first step including forming a planar silicon layer on a silicon substrate and forming a first pillar-shaped silicon layer and a second pillar-shaped silicon layer on the planar silicon layer; a second step including, after the first step, forming an oxide film hard mask on the first pillar-shaped silicon layer and the second pillar-shaped silicon layer, and forming a second oxide film on the planar silicon layer, the

second oxide film being thicker than a gate insulating film; and a third step including, after the second step, forming the gate insulating film around each of the first pillar-shaped silicon layer and the second pillar-shaped silicon layer, forming a metal film and a polysilicon film around the gate insulating film, the polysilicon film having a thickness that is smaller than half of a distance between the first pillar-shaped silicon layer and the second pillar-shaped silicon layer, forming a third resist for forming a gate line, and performing anisotropic etching to form the gate line.

[0011]

The method includes, after the third step, a fourth step including depositing a fourth resist, exposing a portion of the polysilicon film on an upper side wall of each of the first pillar-shaped silicon layer and the second pillar-shaped silicon layer, removing the exposed portion of the polysilicon film by etching, stripping the fourth resist, and removing the metal film by etching to form a first gate electrode and a second gate electrode that are connected to the gate line.

[0012]

A thick oxide film is deposited on the first pillar-shaped silicon layer, the second pillar-shaped silicon layer, and the planar silicon layer, a thin oxide film is deposited

on side walls of the pillar-shaped silicon layer and the second pillar-shaped silicon layer; and the oxide films are removed by isotropic etching to form the oxide film hard mask on the first pillar-shaped silicon layer and the second pillar-shaped silicon layer and to form the second oxide film on the planar silicon layer, the second oxide film being thicker than the gate insulating film.

[0013]

The method further includes a fifth step including forming a first n-type diffusion layer in an upper portion of the first pillar-shaped silicon layer, forming a second n-type diffusion layer in a lower portion of the first pillar-shaped silicon layer and in an upper portion of the planar silicon layer, forming a first p-type diffusion layer in an upper portion of the second pillar-shaped silicon layer, and forming a second p-type diffusion layer in a lower portion of the second pillar-shaped silicon layer and in an upper portion of the planar silicon layer.

[0014]

The method further includes a sixth step including forming silicides on the first n-type diffusion layer, the second n-type diffusion layer, the first p-type diffusion layer, the second p-type diffusion layer, and the gate line.

[0015]

A semiconductor device according to the present

invention includes a planar silicon layer formed on a silicon substrate; first and second pillar-shaped silicon layers formed on the planar silicon layer; a gate insulating film formed around the first pillar-shaped silicon layer; a first gate electrode having a laminated structure of a metal film and a polysilicon film and formed around the gate insulating film; a gate insulating film formed around the second pillar-shaped silicon layer; a second gate electrode having a laminated structure of a metal film and a polysilicon film and formed around the gate insulating film, the polysilicon film having a thickness that is smaller than half of a distance between the first pillar-shaped silicon layer and the second pillar-shaped silicon layer; a gate line connected to the first and second gate electrodes, the gate line having an upper surface located lower than upper surfaces of the first and second gate electrodes; a second oxide film formed between the gate line and the planar silicon layer, the second oxide film being thicker than the gate insulating films; a first n-type diffusion layer formed in an upper portion of the first pillar-shaped silicon layer; a second n-type diffusion layer formed in a lower portion of the first pillar-shaped silicon layer and in an upper portion of the planar silicon layer; a first p-type diffusion layer formed in an upper portion of the second pillar-shaped silicon layer; and a second p-type diffusion

layer formed in a lower portion of the second pillar-shaped silicon layer and in an upper portion of the planar silicon layer.

[0016]

The gate line has a laminated structure of the metal film and a silicide.

[0017]

A center line of the gate line is displaced from a line that connects a center point of the first pillar-shaped silicon layer to a center point of the second pillar-shaped silicon layer by a first predetermined distance.

[0018]

The semiconductor device includes silicides formed on the first and second n-type diffusion layers and the first and second p-type diffusion layers.

Advantageous Effects of Invention

[0019]

According to the present invention, there can be provided a method for producing an SGT in which a thin gate material is used, a metal gate is employed, and a self-aligned process is performed and an SGT structure obtained by the method.

[0020]

The self-aligned process is achieved by, after the first step, forming an oxide film hard mask on the first

pillar-shaped silicon layer and the second pillar-shaped silicon layer; a third step including forming a gate insulating film around each of the first pillar-shaped silicon layer and the second pillar-shaped silicon layer, forming a metal film and a polysilicon film around the gate insulating film, the polysilicon film having a thickness that is smaller than half of a distance between the first pillar-shaped silicon layer and the second pillar-shaped silicon layer, forming a third resist for forming a gate line, and performing anisotropic etching to form the gate line; and, after the third step, a fourth step including depositing a fourth resist, exposing a portion of the polysilicon film on an upper side wall of each of the first pillar-shaped silicon layer and the second pillar-shaped silicon layer, removing the exposed portion of the polysilicon film by etching, stripping the fourth resist, and removing the metal film by etching to form a first gate electrode and a second gate electrode that are connected to the gate line. Such a self-aligned process allows high degree of integration.

[0021]

In particular, the oxide film hard mask protects the upper portions of silicon pillars during formation of the gate line to thereby achieve the self-aligned process.

[0022]

By forming a second oxide film between the gate line and the planar silicon layer, the second oxide film being thicker than the gate insulating films, capacitance between the gate line and the substrate can be decreased. In addition, insulation between the gate line and the substrate can be ensured with more certainty.

[0023]

The gate line has a laminated structure of the metal film and a silicide. A direct contact between the silicide and the metal film allows a decrease in the resistance.

[0024]

A center line of the gate line is displaced from a line that connects a center point of the first pillar-shaped silicon layer to a center point of the second pillar-shaped silicon layer by a first predetermined distance. A silicide that connects the second n-type diffusion layer to the second p-type diffusion layer is easily formed, which allows high degree of integration.

Brief Description of Drawings

[0025]

[Fig. 1] Fig. 1(A) is a plan view of a semiconductor device according to an embodiment of the present invention. Fig. 1(B) is a sectional view taken along line X-X' of Fig. 1(A). Fig. 1(C) is a sectional view taken along line Y-Y' of Fig. 1(A).

[Fig. 2] Fig. 2(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 2(B) is a sectional view taken along line X-X' of Fig. 2(A). Fig. 2(C) is a sectional view taken along line Y-Y' of Fig. 2(A).

[Fig. 3] Fig. 3(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 3(B) is a sectional view taken along line X-X' of Fig. 3(A). Fig. 3(C) is a sectional view taken along line Y-Y' of Fig. 3(A).

[Fig. 4] Fig. 4(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 4(B) is a sectional view taken along line X-X' of Fig. 4(A). Fig. 4(C) is a sectional view taken along line Y-Y' of Fig. 4(A).

[Fig. 5] Fig. 5(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 5(B) is a sectional view taken along line X-X' of Fig. 5(A). Fig. 5(C) is a sectional view taken along line Y-Y' of Fig. 5(A).

[Fig. 6] Fig. 6(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 6(B) is a sectional view taken along line X-X' of Fig. 6(A). Fig. 6(C) is a sectional view taken along line Y-Y' of Fig. 6(A).

[Fig. 7] Fig. 7(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 7(B) is a sectional view taken along line X-X' of Fig. 7(A). Fig. 7(C) is a sectional view taken along line Y-Y' of Fig. 7(A).

[Fig. 8] Fig. 8(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 8(B) is a sectional view taken along line X-X' of Fig. 8(A). Fig. 8(C) is a sectional view taken along line Y-Y' of Fig. 8(A).

[Fig. 9] Fig. 9(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 9(B) is a sectional view taken along line X-X' of Fig. 9(A). Fig. 9(C) is a sectional view taken along line Y-Y' of Fig. 9(A).

[Fig. 10] Fig. 10(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 10(B) is a sectional view taken along line X-X' of Fig. 10(A). Fig. 10(C) is a sectional view taken along line Y-Y' of Fig. 10(A).

[Fig. 11] Fig. 11(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 11(B) is a sectional view taken along line X-X' of Fig. 11(A). Fig. 11(C) is a sectional view taken along line Y-Y' of Fig. 11(A).

[Fig. 12] Fig. 12(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 12(B) is a sectional view taken along line X-X' of Fig. 12(A). Fig. 12(C) is a sectional view taken along line Y-Y' of Fig. 12(A).

[Fig. 13] Fig. 13(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 13(B) is a sectional view taken along line X-X' of Fig. 13(A). Fig. 13(C) is a sectional view taken along line Y-Y' of Fig. 13(A).

[Fig. 14] Fig. 14(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 14(B) is a sectional view taken along line X-X' of Fig. 14(A). Fig. 14(C) is a sectional view taken along line Y-Y' of Fig. 14(A).

[Fig. 15] Fig. 15(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 15(B) is a sectional view taken along line X-X' of Fig. 15(A). Fig. 15(C) is a sectional view taken along line Y-Y' of Fig. 15(A).

[Fig. 16] Fig. 16(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 16(B) is a sectional view taken along line X-X' of Fig. 16(A). Fig. 16(C) is a sectional view taken along line Y-Y' of Fig. 16(A).

[Fig. 17] Fig. 17(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 17(B) is a sectional view taken along line X-X' of Fig. 17(A). Fig. 17(C) is a sectional view taken along line Y-Y' of Fig. 17(A).

[Fig. 18] Fig. 18(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 18(B) is a sectional view taken along line X-X' of Fig. 18(A). Fig. 18(C) is a sectional view taken along line Y-Y' of Fig. 18(A).

[Fig. 19] Fig. 19(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 19(B) is a sectional view taken along line X-X' of Fig. 19(A). Fig. 19(C) is a sectional view taken along line Y-Y' of Fig. 19(A).

[Fig. 20] Fig. 20(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 20(B) is a sectional view taken along line X-X' of Fig. 20(A). Fig. 20(C) is a sectional view taken along line Y-Y' of Fig. 20(A).

[Fig. 21] Fig. 21(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 21(B) is a sectional view taken along line X-X' of Fig. 21(A). Fig. 21(C) is a sectional view taken along line Y-Y' of Fig. 21(A).

[Fig. 22] Fig. 22(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 22(B) is a sectional view taken along line X-X' of Fig. 22(A). Fig. 22(C) is a sectional view taken along line Y-Y' of Fig. 22(A).

[Fig. 23] Fig. 23(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 23(B) is a sectional view taken along line X-X' of Fig. 23(A). Fig. 23(C) is a sectional view taken along line Y-Y' of Fig. 23(A).

[Fig. 24] Fig. 24(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 24(B) is a sectional view taken along line X-X' of Fig. 24(A). Fig. 24(C) is a sectional view taken along line Y-Y' of Fig. 24(A).

[Fig. 25] Fig. 25(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 25(B) is a sectional view taken along line X-X' of Fig. 25(A). Fig. 25(C) is a sectional view taken along line Y-Y' of Fig. 25(A).

[Fig. 26] Fig. 26(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 26(B) is a sectional view taken along line X-X' of Fig. 26(A). Fig. 26(C) is a sectional view taken along line Y-Y' of Fig. 26(A).

[Fig. 27] Fig. 27(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 27(B) is a sectional view taken along line X-X' of Fig. 27(A). Fig. 27(C) is a sectional view taken along line Y-Y' of Fig. 27(A).

[Fig. 28] Fig. 28(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 28(B) is a sectional view taken along line X-X' of Fig. 28(A). Fig. 28(C) is a sectional view taken along line Y-Y' of Fig. 28(A).

[Fig. 29] Fig. 29(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 29(B) is a sectional view taken along line X-X' of Fig. 29(A). Fig. 29(C) is a sectional view taken along line Y-Y' of Fig. 29(A).

[Fig. 30] Fig. 30(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 30(B) is a sectional view taken along line X-X' of Fig. 30(A). Fig. 30(C) is a sectional view taken along line Y-Y' of Fig. 30(A).

[Fig. 31] Fig. 31(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 31(B) is a sectional view taken along line X-X' of Fig. 31(A). Fig. 31(C) is a sectional view taken along line Y-Y' of Fig. 31(A).

[Fig. 32] Fig. 32(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 32(B) is a sectional view taken along line X-X' of Fig. 32(A). Fig. 32(C) is a sectional view taken along line Y-Y' of Fig. 32(A).

[Fig. 33] Fig. 33(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 33(B) is a sectional view taken along line X-X' of Fig. 33(A). Fig. 33(C) is a sectional view taken along line Y-Y' of Fig. 33(A).

[Fig. 34] Fig. 34(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 34(B) is a sectional view taken along line X-X' of Fig. 34(A). Fig. 34(C) is a sectional view taken along line Y-Y' of Fig. 34(A).

[Fig. 35] Fig. 35(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 35(B) is a sectional view taken along line X-X' of Fig. 35(A). Fig. 35(C) is a sectional view taken along line Y-Y' of Fig. 35(A).

[Fig. 36] Fig. 36(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 36(B) is a sectional view taken along line X-X' of Fig. 36(A). Fig. 36(C) is a sectional view taken along line Y-Y' of Fig. 36(A).

[Fig. 37] Fig. 37(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 37(B) is a sectional view taken along line X-X' of Fig. 37(A). Fig. 37(C) is a sectional view taken along line Y-Y' of Fig. 37(A).

[Fig. 38] Fig. 38(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 38(B) is a sectional view taken along line X-X' of Fig. 38(A). Fig. 38(C) is a sectional view taken along line Y-Y' of Fig. 38(A).

[Fig. 39] Fig. 39(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 39(B) is a sectional view taken along line X-X' of Fig. 39(A). Fig. 39(C) is a sectional view taken along line Y-Y' of Fig. 39(A).

[Fig. 40] Fig. 40(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 40(B) is a sectional view taken along line X-X' of Fig. 40(A). Fig. 40(C) is a sectional view taken along line Y-Y' of Fig. 40(A).

[Fig. 41] Fig. 41(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 41(B) is a sectional view taken along line X-X' of Fig. 41(A). Fig. 41(C) is a sectional view taken along line Y-Y' of Fig. 41(A).

[Fig. 42] Fig. 42(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 42(B) is a sectional view taken along line X-X' of Fig. 42(A). Fig. 42(C) is a sectional view taken along line Y-Y' of Fig. 42(A).

[Fig. 43] Fig. 43(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 43(B) is a sectional view taken along line X-X' of Fig. 43(A). Fig. 43(C) is a sectional view taken along line Y-Y' of Fig. 43(A).

Description of Embodiments

[0026]

Hereinafter, referring to Figs. 2 to 43, a production process of a semiconductor device having an SGT structure according to an embodiment of the present invention will be described.

[0027]

Hereafter, a first step will be described that includes forming a planar silicon layer on a silicon substrate and forming a first pillar-shaped silicon layer and a second pillar-shaped silicon layer on the planar silicon layer.

[0028]

As illustrated in Fig. 2, on a silicon substrate 101, first resists 102 and 103 for forming a first pillar-shaped silicon layer 104 and a second pillar-shaped silicon layer

105 are formed.

[0029]

As illustrated in Fig. 3, the silicon substrate 101 is etched to form the first pillar-shaped silicon layer 104 and the second pillar-shaped silicon layer 105. Since the resists are used to form the pillar-shaped silicon layers, the number of steps can be decreased, compared with a process using a hard mask.

[0030]

As illustrated in Fig. 4, the first resists 102 and 103 are stripped.

[0031]

As illustrated in Fig. 5, a second resist 106 for forming a planar silicon layer 107 is formed.

[0032]

As illustrated in Fig. 6, the silicon substrate 101 is etched to form the planar silicon layer 107.

[0033]

As illustrated in Fig. 7, the second resist 106 is stripped.

[0034]

As illustrated in Fig. 8, an element separation film 108 is formed around the planar silicon layer 107.

Thus, the first step has been described that includes forming the planar silicon layer 107 on the silicon

substrate 101 and forming the first pillar-shaped silicon layer 104 and the second pillar-shaped silicon layer 105 on the planar silicon layer 107.

[0035]

Hereafter, a second step will be described that includes forming an oxide film hard mask on the first pillar-shaped silicon layer and the second pillar-shaped silicon layer, and forming a second oxide film on the planar silicon layer, the second oxide film being thicker than a gate insulating film.

[0036]

As illustrated in Fig. 9, an oxide film 109 is deposited so as to cover the first pillar-shaped silicon layer 104, the second pillar-shaped silicon layer 105, and the planar silicon layer 107. This deposition is preferably performed by atmospheric pressure CVD (chemical vapor deposition). Employment of deposition by atmospheric pressure CVD allows deposition of a thick oxide film on the first pillar-shaped silicon layer 104, the second pillar-shaped silicon layer 105, and the planar silicon layer 107, and deposition of a thin oxide film on the side walls of the pillar-shaped silicon layer 104 and the second pillar-shaped silicon layer 105. In addition, the oxide film on the first pillar-shaped silicon layer 104 and the second pillar-shaped silicon layer 105 can be deposited so as to be thicker than

the oxide film deposited on the planar silicon layer 107.

[0037]

As illustrated in Fig. 10, the oxide film 109 is removed by isotropic etching to form oxide film hard masks 111 and 112 on the first pillar-shaped silicon layer 104 and the second pillar-shaped silicon layer 105 and to form a second oxide film 110 on the planar silicon layer 107, the second oxide film 110 being thicker than the gate insulating film.

[0038]

Thus, the second step has been described that includes forming an oxide film hard mask on the first pillar-shaped silicon layer and the second pillar-shaped silicon layer, and forming a second oxide film on the planar silicon layer, the second oxide film being thicker than a gate insulating film.

[0039]

Hereafter, a third step will be described that includes forming the gate insulating film around each of the first pillar-shaped silicon layer and the second pillar-shaped silicon layer, forming a metal film and a polysilicon film around the gate insulating film, the polysilicon film having a thickness that is smaller than half of a distance between the first pillar-shaped silicon layer and the second pillar-shaped silicon layer, forming a third resist for forming a

gate line, and performing anisotropic etching to form the gate line.

[0040]

As illustrated in Fig. 11, gate insulating films 113 and 114 are formed around the first pillar-shaped silicon layer 104 and the second pillar-shaped silicon layer 105; and a metal film 115 and a polysilicon film 116 are formed around the gate insulating films 113 and 114. Accordingly, formation of voids in the polysilicon film 116 can be suppressed. The metal film 115 may be formed of any metal that is used in a semiconductor process and sets the threshold voltage of a transistor, such as titanium nitride. The gate insulating films 113 and 114 may be any films that are used in a semiconductor process, such as, oxide films, oxynitride films, and high-dielectric films.

[0041]

As illustrated in Fig. 12, a third resist 117 for forming a gate line is formed. In this embodiment, the resist is illustrated such that its top is located lower than the pillar-shaped silicon layers. This is because, when the pillar-shaped silicon layers have a large height, the thickness of the resist on upper portions of the pillar-shaped silicon layers may be small or the polysilicon on upper portions of the pillar-shaped silicon layers may be exposed. The narrower the gate-line width, the higher the

probability of exposure of the polysilicon on the upper portions of the pillar-shaped silicon layers. The resist may be formed such that its top is located higher than the pillar-shaped silicon layers.

[0042]

In addition, in this case, the third resist 117 is preferably formed such that the center line of the third resist 117 for the gate line is displaced from a line that connects the center point of the first pillar-shaped silicon layer 104 to the center point of the second pillar-shaped silicon layer 105. This is because a silicide that connects a second n-type diffusion layer to a second p-type diffusion layer is easily formed.

[0043]

As illustrated in Fig. 13, the polysilicon film 116 and the metal film 115 are etched to form gate electrodes 118a and 118b and a gate line 118c. In this case, even when the thickness of the resist on upper portions of the pillar-shaped silicon layers is small or the polysilicon on upper portions of the pillar-shaped silicon layers is exposed, the upper portions of the pillar-shaped silicon layers are protected by the oxide film hard masks 111 and 112.

[0044]

As illustrated in Fig. 14, the second oxide film 110 is etched. At this time, the oxide film hard masks 111 and 112

are also etched. However, since the thickness of the oxide films deposited on the first pillar-shaped silicon layer 104 and the second pillar-shaped silicon layer 105 is larger than the thickness of the oxide film deposited on the planar silicon layer 107, the oxide film hard masks 111 and 112 are left. When the oxide film hard masks 111 and 112 are not left, in a subsequent step, the silicon pillars will be etched during removal of the polysilicon film. In this case, the height of the polysilicon film exposed is preferably increased by the height of the silicon pillars that is decreased by etching. Alternatively, the second oxide film 110 may be etched after the fourth step.

[0045]

As illustrated in Fig. 15, the third resist 117 is stripped.

[0046]

Thus, the third step has been described that includes forming a gate insulating film around each of the first pillar-shaped silicon layer and the second pillar-shaped silicon layer, forming a metal film and a polysilicon film around the gate insulating film, the polysilicon film having a thickness that is smaller than half of a distance between the first pillar-shaped silicon layer and the second pillar-shaped silicon layer, forming a third resist for forming a gate line, and performing anisotropic etching to form the

gate line.

[0047]

Hereafter, a fourth step will be described that includes depositing a fourth resist, exposing a portion of the polysilicon film on an upper side wall of each of the first pillar-shaped silicon layer and the second pillar-shaped silicon layer, removing the exposed portion of the polysilicon film by etching, stripping the fourth resist, and removing the metal film by etching to form a first gate electrode and a second gate electrode that are connected to the gate line.

[0048]

As illustrated in Fig. 16, a fourth resist 119 is deposited; and portions of the polysilicon film 116 on upper side walls of the first pillar-shaped silicon layer 104 and the second pillar-shaped silicon layer 105 are exposed, which is preferably achieved by resist etch back. Alternatively, a spin-on-glass coating film may be used.

[0049]

As illustrated in Fig. 17, the exposed portions of the polysilicon film 116 are removed by etching, which is preferably performed by isotropic dry etching.

[0050]

As illustrated in Fig. 18, the fourth resist 119 is stripped.

[0051]

As illustrated in Fig. 19, an oxide film 160 is deposited.

[0052]

As illustrated in Fig. 20, a fifth resist 161 is deposited; and portions of the oxide film 160 on upper side walls of the first pillar-shaped silicon layer 104 and the second pillar-shaped silicon layer 105 are exposed, which is preferably achieved by resist etch back. Alternatively, a spin-on-glass coating film may be used.

[0053]

As illustrated in Fig. 21, the exposed portions of the oxide film 160 are removed by etching, which is preferably performed by isotropic etching.

[0054]

As illustrated in Fig. 22, the fifth resist 161 is stripped.

[0055]

As illustrated in Fig. 23, the metal film 115 is removed by etching to form the first gate electrode 118b and the second gate electrode 118a that are connected to the gate line 118c. Thus, a self-aligned process is performed.

[0056]

As illustrated in Fig. 24, the oxide film hard masks 111 and 112 and the oxide film 160 are removed by etching.

[0057]

Thus, the fourth step has been described that includes depositing a fourth resist, exposing a portion of the polysilicon film on an upper side wall of each of the first pillar-shaped silicon layer and the second pillar-shaped silicon layer, removing the exposed portion of the polysilicon film by etching, stripping the fourth resist, and removing the metal film by etching to form a first gate electrode and a second gate electrode that are connected to the gate line.

[0058]

Hereafter, a fifth step will be described that includes forming a first n-type diffusion layer in an upper portion of the first pillar-shaped silicon layer, forming a second n-type diffusion layer in a lower portion of the first pillar-shaped silicon layer and in an upper portion of the planar silicon layer, forming a first p-type diffusion layer in an upper portion of the second pillar-shaped silicon layer, and forming a second p-type diffusion layer in a lower portion of the second pillar-shaped silicon layer and in an upper portion of the planar silicon layer.

[0059]

As illustrated in Fig. 25, a sixth resist 120 is formed for the purpose of forming a first n-type diffusion layer and a second n-type diffusion layer. Before the sixth

resist 120 is formed, a thin oxide film may be deposited.

[0060]

As illustrated in Fig. 26, arsenic is implanted to form a first n-type diffusion layer 121 and a second n-type diffusion layer 122.

[0061]

As illustrated in Fig. 27, the sixth resist 120 is stripped.

[0062]

As illustrated in Fig. 28, a seventh resist 123 is formed for forming a first p-type diffusion layer and a second p-type diffusion layer.

[0063]

As illustrated in Fig. 29, boron or boron fluoride is implanted to form a first p-type diffusion layer 124 and a second p-type diffusion layer 125.

[0064]

As illustrated in Fig. 30, the seventh resist 123 is stripped, a nitride film 126 is deposited, and a heat treatment is performed.

[0065]

Thus, the fifth step has been described that includes forming a first n-type diffusion layer in an upper portion of the first pillar-shaped silicon layer, forming a second n-type diffusion layer in a lower portion of the first

pillar-shaped silicon layer and in an upper portion of the planar silicon layer, forming a first p-type diffusion layer in an upper portion of the second pillar-shaped silicon layer, and forming a second p-type diffusion layer in a lower portion of the second pillar-shaped silicon layer and in an upper portion of the planar silicon layer.

[0066]

Hereafter, a sixth step will be described that includes forming silicides on the first n-type diffusion layer, the second n-type diffusion layer, the first p-type diffusion layer, the second p-type diffusion layer, and the gate line.

[0067]

As illustrated in Fig. 31, the nitride film 126 is etched to form nitride film side walls; and a metal is deposited, a heat treatment is performed, and unreacted metal is removed. As a result, silicides 128, 130, 132, 134, 127, 131, 129, and 133 are formed on the first n-type diffusion layer 121, the second n-type diffusion layer 122, the first p-type diffusion layer 124, the second p-type diffusion layer 125, the gate line 118c, the first gate electrode 118b and the second gate electrode 118a. The nitride film side walls may have a laminated structure of an oxide film and a nitride film.

[0068]

The connection between the second n-type diffusion

layer 122 and the second p-type diffusion layer 125 is achieved by the silicide 130. Since the center line of the gate line 118c is displaced from a line that connects the center point of the first pillar-shaped silicon layer 104 to the center point of the second pillar-shaped silicon layer 105, the silicide 130 is easily formed, which allows high degree of integration.

[0069]

In addition, since the polysilicon film 116 is thin, the gate line 118c tends to have a laminated structure of the metal film 115 and the silicide 127. The direct contact between the silicide 127 and the metal film 115 allows a decrease in the resistance.

[0070]

Thus, the sixth step has been described that includes forming silicides on the first n-type diffusion layer, the second n-type diffusion layer, the first p-type diffusion layer, the second p-type diffusion layer, and the gate line.

[0071]

As illustrated in Fig. 32, a contact stopper 137 such as a nitride film is formed; and an interlayer insulating film 138 is formed.

[0072]

As illustrated in Fig. 33, an eighth resist 139 for forming contact holes is formed.

[0073]

As illustrated in Fig. 34, the interlayer insulating film 138 is etched to form contact holes 140 and 141.

[0074]

As illustrated in Fig. 35, the eighth resist 139 is stripped.

[0075]

As illustrated in Fig. 36, a ninth resist 142 for forming contact holes is formed. The interlayer insulating film 138 is etched to form contact holes 143 and 144.

[0076]

As illustrated in Fig. 37, the ninth resist 142 is stripped.

[0077]

As illustrated in Fig. 38, the contact stopper 137 is etched to remove portions of the contact stopper 137 below the contact holes 140 and 141 and the contact holes 143 and 144.

[0078]

As illustrated in Fig. 39, a metal is deposited to form contacts 145, 146, 147, and 148.

[0079]

As illustrated in Fig. 40, a metal 149 for metal wirings is deposited.

[0080]

As illustrated in Fig. 41, tenth resists 150, 151, 152, and 153 for forming metal wirings are formed.

[0081]

As illustrated in Fig. 42, the metal 149 is etched to form metal wirings 154, 155, 156, and 157.

[0082]

Next, as illustrated in Fig. 43, the tenth resists 150, 151, 152, and 153 are stripped. Thus, a method for producing an SGT in which a thin gate material is used, a metal gate is employed, and a self-aligned process is performed has been described.

[0083]

The structure of a semiconductor device obtained by the above-described production method is illustrated in Fig. 1. As illustrated in Fig. 1, the semiconductor device includes the planar silicon layer 107 formed on the silicon substrate 101; the first and second pillar-shaped silicon layers 104 and 105 formed on the planar silicon layer 107; the gate insulating film 113 formed around the first pillar-shaped silicon layer 104; the first gate electrode 118b having a laminated structure of the metal film 115 and the polysilicon film 116 and formed around the gate insulating film 113; the gate insulating film 114 formed around the second pillar-shaped silicon layer 105; the second gate electrode 118a having a laminated structure of the metal

film 115 and the polysilicon film 116 and formed around the gate insulating film 114, the polysilicon film 116 having a thickness that is smaller than half of a distance between the first pillar-shaped silicon layer 104 and the second pillar-shaped silicon layer 105; the gate line 118c connected to the first and second gate electrodes 118b and 118a, the gate line 118c having an upper surface located lower than upper surfaces of the first and second gate electrodes 118b and 118a; the second oxide film 110 formed between the gate line 118c and the planar silicon layer 107, the second oxide film 110 being thicker than the gate insulating films 113 and 114; the first n-type diffusion layer 121 formed in an upper portion of the first pillar-shaped silicon layer 104; the second n-type diffusion layer 112 formed in a lower portion of the first pillar-shaped silicon layer 104 and in an upper portion of the planar silicon layer 107; the first p-type diffusion layer 124 formed in an upper portion of the second pillar-shaped silicon layer 105; and the second p-type diffusion layer 125 formed in a lower portion of the second pillar-shaped silicon layer 105 and in an upper portion of the planar silicon layer 107.

[0084]

The second oxide film 110 is formed between the gate line 118c and the planar silicon layer 107, the second oxide

film 110 being thicker than the gate insulating films 113 and 114. Accordingly, capacitance between the gate line and the substrate can be decreased and insulation between the gate line and the substrate can be ensured.

[0085]

In addition, the gate line 118c has a laminated structure of the metal film 115 and the silicide 127. The direct contact between the silicide 127 and the metal film 115 allows a decrease in the resistance.

[0086]

The center line of the gate line 118c is displaced from a line that connects the center point of the first pillar-shaped silicon layer 104 to the center point of the second pillar-shaped silicon layer 105 by a first predetermined distance. The silicide 130 that connects the second n-type diffusion layer 122 to the second p-type diffusion layer 125 is easily formed, which allows high degree of integration.

[0087]

In the present invention, various embodiments and modifications can be made without departing from the broad spirit and scope of the present invention. Furthermore, the above-described embodiment is provided to describe one embodiment of the present invention, and the scope of the present invention is not limited thereto.

[0088]

For example, a method for producing a semiconductor device in which the p-type (including the p⁺-type) and the n-type (including the n⁺-type) are each changed to the opposite conductivity type in the above embodiment, and a semiconductor device produced by the method are also obviously included in the technical scope of the present invention.

Reference Signs List

[0089]

- 101. silicon substrate
- 102. first resist
- 103. first resist
- 104. first pillar-shaped silicon layer
- 105. first pillar-shaped silicon layer
- 106. second resist
- 107. planar silicon layer
- 108. element separation film
- 109. oxide film
- 110. second oxide film
- 111. oxide film hard mask
- 112. oxide film hard mask
- 113. gate insulating film
- 114. gate insulating film
- 115. metal film
- 116. polysilicon film

- 117. third resist
- 118a. gate electrode
- 118b. gate electrode
- 118c. gate line
- 119. fourth resist
- 120. sixth resist
- 121. first n-type diffusion layer
- 122. second n-type diffusion layer
- 123. seventh resist
- 124. first p-type diffusion layer
- 125. second p-type diffusion layer
- 126. nitride film
- 127. silicide
- 128. silicide
- 129. silicide
- 130. silicide
- 131. silicide
- 132. silicide
- 133. silicide
- 134. silicide
- 137. contact stopper
- 138. interlayer insulating film
- 139. eighth resist
- 140. contact hole
- 141. contact hole

- 142. ninth resist
- 143. contact hole
- 144. contact hole
- 145. contact
- 146. contact
- 147. contact
- 148. contact
- 149. metal
- 150. tenth resist
- 151. tenth resist
- 152. tenth resist
- 153. tenth resist
- 154. metal wiring
- 155. metal wiring
- 156. metal wiring
- 157. metal wiring
- 160. oxide film
- 161. fifth resist

CLAIMS

1. A method for producing a semiconductor device having a structure in which a source, a gate, and a drain are disposed so as to have a pillar shape perpendicular to a silicon substrate and a gate electrode surrounds a pillar-shaped semiconductor layer, the method comprising:

a first step including forming a planar silicon layer on the silicon substrate and forming a first pillar-shaped silicon layer and a second pillar-shaped silicon layer on the planar silicon layer;

a second step following the first step, including forming an oxide film hard mask on the first pillar-shaped silicon layer and the second pillar-shaped silicon layer, and forming a second oxide film on the planar silicon layer, the second oxide film being thicker than a gate insulating film; and

a third step following the second step, including forming the gate insulating film on each of the first pillar-shaped silicon layer and the second pillar-shaped silicon layer, forming a metal film and a polysilicon film on the gate insulating film, forming a third resist for forming a gate line such that the metal film and the polysilicon film formed on the first pillar-shaped silicon layer are connected to the metal film and the polysilicon film formed on the second

pillar-shaped silicon layer, and performing anisotropic etching on the polysilicon film and the metal film to form the gate line, the polysilicon film having a thickness that is smaller than half a distance between the first pillar-shaped silicon layer and the second pillar-shaped silicon layer, and

after the third step, a fourth step including depositing a fourth resist, exposing a portion of the polysilicon film on an upper side wall of each of the first pillar-shaped silicon layer and the second pillar-shaped silicon layer, removing the exposed portion of the polysilicon film by etching, stripping the fourth resist, and removing the metal film by etching to form a first gate electrode and a second gate electrode that are connected to the gate line.

2. The method for producing a semiconductor device according to Claim 1, wherein a thick oxide film is deposited on the first pillar-shaped silicon layer, the second pillar-shaped silicon layer, and the planar silicon layer, a thin oxide film is deposited on side walls of the first pillar-shaped silicon layer and the second pillar-shaped silicon layer; and the thick oxide film and the thin oxide film are removed by isotropic etching to form the oxide film hard mask on the first pillar-shaped silicon layer and the second pillar-shaped silicon layer and to form the second

oxide film on the planar silicon layer, the second oxide film being thicker than the gate insulating film.

3. The method for producing a semiconductor device according to Claim 1, further comprising a fifth step including

forming a first n-type diffusion layer in an upper portion of the first pillar-shaped silicon layer,

forming a second n-type diffusion layer in a lower portion of the first pillar-shaped silicon layer and in an upper portion of the planar silicon layer,

forming a first p-type diffusion layer in an upper portion of the second pillar-shaped silicon layer, and

forming a second p-type diffusion layer in a lower portion of the second pillar-shaped silicon layer and in an upper portion of the planar silicon layer.

4. The method for producing a semiconductor device according to Claim 3, further comprising a sixth step including forming silicides on the first n-type diffusion layer, the second n-type diffusion layer, the first p-type diffusion layer, the second p-type diffusion layer, and the gate line.