What is claimed is:

1. A nonvolatile memory device comprising:

a memory cell array including a plurality of pages, each of the plurality of pages including a plurality of memory cells, each of the plurality of memory cells storing a plurality of data bits, each of the plurality of data bits being selectable by a different threshold voltage;

a page buffer circuit coupled to the memory cell array through a plurality of bit-lines, the page buffer circuit including a plurality of page buffers configured to

sense data from selected memory cells among the plurality of memory cells through the plurality of bit-lines, and

perform a first read operation and a second read operation, each including two sequential sensing operations to determine one data state, and each of the plurality of page buffers including a latch, among a plurality of latches, the latch configured to sequentially store results of the two sequential sensing operations; and

a control circuit configured to

control the plurality of page buffers to store a result of the first read operation,

reset the plurality of latches after completion of the first read operation, and

control the plurality of page buffers to perform the second read operation based on a valley determined based on the result of the first read operation.

2. The nonvolatile memory device of claim 1, wherein

the page buffer circuit includes a first group of page buffers coupled to a first group of bit-lines among the plurality of bit-lines and a second group of page buffers coupled to a second group of bit-lines among the plurality of bit-lines,

the first group of page buffers is configured to perform the first read operation with

respect to the selected memory cells during a first develop period, and

the second group of page buffers is configured to perform the first read operation with respect to the selected memory cells during a second develop period different from the first develop period.

3. The nonvolatile memory device of claim 2, wherein

the control circuit is configured to cause a first read voltage to be applied to one or more word-lines coupled to the selected memory cells during performance of the first read operation,

the first group of page buffers is configured to sequentially perform a first sensing operation and a second sensing operation on the first group of bit-lines, and

the second group of page buffers is configured to sequentially perform a third sensing operation and a fourth sensing operation on the second group of bit-lines.

4. The nonvolatile memory device of claim 3, wherein

the first group of page buffers is configured to perform the first read operation on the selected memory cells during the first develop period which starts at a first time point, and

the second group of page buffers is configured to perform the first read operation on the selected memory cells during the second develop period which starts at a second time point posterior to the first time point.

5. The nonvolatile memory device of claim 3 or claim 4, wherein the control circuit is configured to control the first group of page buffers and the second group of page buffers such that the first group of page buffers and the second group of page buffers

respectively perform the first sensing operation and the third sensing operation contemporaneously, and the first group of page buffers and the second group of page buffers respectively perform the second sensing operation and the fourth sensing operation contemporaneously.

6. The nonvolatile memory device of any one of claims 3 to 5, wherein

the control circuit is configured to

count a first number of on cells stored in each of a first group of latches among the plurality of latches included in the first group of page buffers based on a result of the second sensing operation,

count a second number of on cells stored in each of a second group of latches among the plurality of latches included in the second group of page buffers based on a result of the fourth sensing operation, and

determine a position of the valley based on the first number of on cells and the second number of on cells.

7. The nonvolatile memory device of claim 6, wherein the control circuit is configured to control the plurality of page buffers to perform the second read operation based on the first read voltage if a difference between the first number of on cells and the second number of on cells is equal to or smaller than a reference value.

8. The nonvolatile memory device of claim 6, wherein the control circuit is configured to control the plurality of page buffers to perform the second read operation based on a second read voltage greater than the first read voltage if (i) a difference between the first number of on cells and the second number of on cells is greater than a reference value,

and (ii) the first number of on cells is smaller than the second number of on cells.

9. The nonvolatile memory device of claim 6, wherein the control circuit is configured to control the plurality of page buffers to perform the second read operation based on a third read voltage smaller than the first read voltage if (i) a difference between the first number of on cells and the second number of on cells is greater than a reference value, and (ii) the first number of on cells is greater than the second number of on cells.

10. The nonvolatile memory device of claim 1, wherein each of the plurality of page buffers includes:

a pre-charge circuit including a first p-channel metal-oxide semiconductor (PMOS) transistor and a second PMOS transistor connected in series between a pre-charge voltage source and a sensing node;

a switch circuit coupled between a respective bit-line among the plurality of bit-lines and the sensing node; and

a sense and latch circuit coupled between the sensing node and a ground voltage source, the sense and latch circuit including,

a respective latch among the plurality of latches,

a first n-channel metal-oxide semiconductor (NMOS) transistor,

a second NMOS transistor connected in series with the first NMOS transistor between a first node of the respective latch and the ground voltage source,

a third NMOS transistor, and

a fourth NMOS transistor connected in series with the third NMOS transistor between a second node of the respective latch and the ground voltage source, a gate of the fourth NMOS transistor being connected to the sensing node,

wherein the control circuit is configured to

apply a load signal to a gate of the first PMOS transistor,

apply a bit-line set-up signal to a gate of the second PMOS transistor,

apply a reset signal to the third NMOS transistor such that the sense and latch circuit performs a first sensing operation of the first read operation, and

apply a set signal to the first NMOS transistor such that the sense and latch circuit performs a second sensing operation of the first read operation.

11. The nonvolatile memory device of claim 10, wherein after the plurality of bit-lines are pre-charged, the control circuit is configured to:

apply a first bit-line set-up signal with a logic high level to the second PMOS transistor of each of a first group of page buffers among the plurality of page buffers at a first time point such that each of the first group of page buffers sequentially performs the first sensing operation and the second sensing operation on the sensing node; and

apply a second bit-line set-up signal with a logic high level to the second PMOS transistor of each of a second group of pages buffers among the plurality of page buffers at a second time point posterior to the first time point such that each of the second group of page buffers sequentially performs a third sensing operation and a fourth sensing operation on the sensing node.

12. The nonvolatile memory device of claim 11, wherein the control circuit is configured to control the first group of page buffers and the second group of page buffers such that the first group of page buffers and the second group of page buffers respectively perform the first sensing operation and the third sensing operation contemporaneously, and the first group of page buffers and the second group of page buffers respectively perform the

second sensing operation and the fourth sensing operation contemporaneously.

13. The nonvolatile memory device of claim 11 or claim 12, wherein the control circuit is configured to:

count a first number of on cells stored in each of a first group of latches among the plurality of latches included in the first group of page buffers based on a result of the first sensing operation and the second sensing operation,

count a second number of on cells stored in each of a second group of latches among the plurality of latches included in the second group of page buffers based on a result of the third sensing operation and the fourth sensing operation,

determine the valley based on the first number of on cells and the second number of on cells, and

reset one or more values stored in the plurality of latches by applying a refresh signal to a gate of the second NMOS transistor after the determination of the valley.

14. The nonvolatile memory device of any one of claims 1 to 13, wherein the memory cell array includes:

first memory cells coupled to a first word-line, the first memory cells corresponding to the selected memory cells; and

second memory cells coupled to a second word-line, the second memory cells being stacked on the first memory cells.

15. A method of operating a nonvolatile memory device including a memory cell array, the memory cell array including a plurality of pages, each of the plurality of pages including a plurality of memory cells, each of the plurality of memory cells storing a

plurality of data bits, each of the plurality of data bits being selectable by a different threshold voltage, the method comprising:

performing a first read operation including two sensing operations through a plurality of bit-lines to determine one data state from selected memory cells among the plurality of memory cells; and

performing a second read operation to determine one data state based on a valley determined based on a result of the first read operation,

wherein results of the two sensing operations are sequentially stored in a plurality of latches, each latch among the plurality of latches being included in a corresponding page buffer among a plurality of page buffers, the plurality of page buffers being coupled to the plurality of bit-lines, and the plurality of latches being reset after completion of the first read operation.

16. The method of claim 15, wherein

the plurality of page buffers includes a first group of page buffers coupled to a first group of bit-lines among the plurality of bit-lines and a second group of page buffers coupled to a second group of bit-lines among the plurality of bit-lines, and

the performing the first read operation includes,

sequentially performing, in each of the first group of page buffers, a first sensing operation and a second sensing operation on a sensing node coupled to the first group of bit-lines during a first develop period, the first develop period starting from a first time period, and

sequentially performing, in each of the second group of page buffers, a third sensing operation and a fourth sensing operation on a sensing node coupled to the second group of bit-lines during a second develop period, the second develop period

starting from a second time period posterior to the first time period.

17. The method of claim 16, wherein the first sensing operation and the third sensing operation are performed contemporaneously and the second sensing operation and the fourth sensing operation are performed contemporaneously.

18. The method of claim 16 or claim 17, further comprising:

counting a first number of on cells stored in each of a first group of latches among the plurality of latches included in the first group of page buffers based on a result of the second sensing operation;

counting a second number of on cells stored in each of a second group of latches among the plurality of latches included in the second group of page buffers based on a result of the fourth sensing operation; and

determining a position of the valley based on the first number of on cells and the second number of on cells.

19. A method of operating a nonvolatile memory device including a memory cell array, the memory cell array including a plurality of pages, each of the plurality of pages including a plurality of nonvolatile memory cells, each of the plurality of nonvolatile memory cells storing a plurality of data bits, each of the plurality of data bits being selectable by a plurality of different threshold voltages, the method comprising:

determining, in a control circuit of the nonvolatile memory device, a read setting of the nonvolatile memory device based on a command and an address, the command and the address being received from a memory controller configured to control the nonvolatile memory device;

sensing one or more data bits stored in selected memory cells among the plurality of nonvolatile memory cells based on a normal read condition in response to determining the read setting designates a normal read operation; and

performing an on-chip valley search read operation on the selected memory cells in response to determining the read setting designates a valley search read operation,

wherein the on-chip valley search read operation is performed by

determining a valley of the plurality of different threshold voltages, and

sensing the one or more data bits stored in the selected memory cells based on the valley, and

wherein the performing the on-chip valley search read operation includes:

performing a first read operation including two sensing operations through a plurality of bit-lines to determine one data state from the selected memory cells; and

performing a second read operation to determine one data state based on the valley determined based on a result of the first read operation,

wherein results of the two sensing operations are sequentially stored in a plurality of latches, each latch among the plurality of latches being included in a corresponding page buffer among a plurality of page buffers, the plurality of page buffers being coupled to the plurality of bit-lines, and the plurality of latches being reset after completion of the first read operation.