WHAT IS CLAIMED IS:

1. A method of fabricating a semiconductor device, comprising:

providing a substrate;

forming a plurality of line elements on the substrate including a first line element having a first region with a first width and a biased region with a second width, the second width different than the first width;

forming spacer elements abutting sidewalls of each of the plurality of line elements;

after forming the spacer elements, removing the plurality of line elements from the substrate; and

etching an underlying layer using the spacer elements after removing the plurality of line elements.

2. The method of claim 1, wherein the forming the spacer elements includes forming a conformal layer of material on the substrate and etching the conformal layer to form the spacer elements.

3. The method of claim 1, wherein the second width is less than the first width.

4. The method of claim 1, further comprising:

forming a contact element on etched underlying layer.

5. The method of claim 1, further comprising:

using the etched underlying layer as a masking element to form a gate structure; and

forming a contact element on the gate structure.

6. The method of claim 5, wherein the contact element is formed on a shifted region of the gate structure, the shifted region being defined by the spacer element abutting a sidewall of the biased region of the first line element.

7. The method of claim 6, wherein the gate structure is formed on a fin extending from the substrate.

8. The method of claim 1, wherein the forming spacer elements includes forming a first spacer element abutting the first line element, wherein a first region of the first spacer element abutting the biased region of the first line element is noncollinear with a second region the first spacer element abutting the first region of the first line element.

9. The method of claim 8, further comprising:

using the first spacer element as a masking element to form a gate structure on the substrate, wherein the gate structure includes a first region that is noncollinear with a second region, the first region of the gate structure defined by the first region of the first spacer element and the second region of the gate structure defined by the second region of the first spacer element; and

forming a contact element on the first region on the gate structure.

10. The method of claim 1, wherein the forming spacer elements includes forming a first spacer element abutting the first line element, wherein a first region of the first spacer element abutting the biased region of the first line element is offset from a second region of the first spacer element abutting the first region of the first line element, wherein the offset is less than approximately 10 nm.

11. The method of claim 10, further comprising:

using the first region and the second region of the first spacer element as masking elements to etch the underlying layer disposed on the substrate.

12. A finFET transistor, comprising:

a substrate having a fin extending from the substrate;

a gate structure formed on the fin, wherein the gate structure includes:

a first portion and a second portion, wherein the first and second portions each have a first edge and an opposing second edge, and wherein the first edges are substantially collinear and the second edges are substantially collinear; and

an offset portion interposing the first portion and the second portion, the offset portion having a first edge and a second edge, wherein the first edge and the second edge are noncollinear with the first and second edges of the first and second portions of the gate structure; and

a contact element connected to the offset portion of the gate structure.

13. The finFET element of claim 12, wherein the offset portion directly overlies the fin.

14. The finFET element of claim 12, wherein the first portion includes a sidewall, and wherein the first portion sidewall interfaces a lateral sidewall of the fin.

15. The finFET element of claim 12, wherein the gate structure includes a metal gate electrode.

16. A semiconductor device, comprising:

a gate structure formed on a semiconductor substrate, wherein the gate structure includes:

a first portion and a second portion, wherein the first and second portions each have a first edge and an opposing second edge, and wherein the first edges are substantially collinear and the second edges are substantially collinear; and

an offset portion interposing the first portion and the second portion, the offset portion having a first edge and a second edge, wherein the first edge and the second edge

are noncollinear with the first and second edges of the first and second portions of the gate structure.

17. The semiconductor device of claim 16, wherein the gate structure includes a metal gate electrode.

18. The semiconductor device of claim 16, further comprising:

a contact element connected to the offset portion of the gate structure.

19. The semiconductor device of claim 16, wherein gate structure interfaces a single, planar surface of the semiconductor substrate.

20. The semiconductor device of claim 16, wherein gate structure is a contiguous structure.

Claims

1. A method of fabricating a semiconductor device, comprising:

providing a substrate;

forming a plurality of line elements on the substrate, wherein the plurality of line elements includes:

a first contiguous line element having a first region with a first width and wherein the first contiguous line element includes a biased region with a second width, the second width different than the first width;

forming spacer elements abutting sidewalls of each of the plurality of line elements including abutting sidewalls of the first continuous line element at the first region and the biased region;

after forming the spacer elements, removing the plurality of line elements from the substrate; and

etching an underlying layer using the spacer elements after removing the plurality of line elements.

2. The method of claim 1, wherein the forming the spacer elements includes forming a conformal layer of material on the substrate and etching the conformal layer to form the spacer elements.

3. The method of claim 1, wherein the second width is less than the first width.

4. The method of claim 1, further comprising:

forming a contact element on etched underlying layer.

5. The method of claim 1, further comprising:

using the etched underlying layer as a masking element to form a gate structure; and

forming a contact element on the gate structure.

6. The method of claim 5, wherein the contact element is formed on a shifted region of the gate structure, the shifted region being defined by the spacer element abutting a sidewall of the biased region of the first line element.

7. The method of claim 6, wherein the gate structure is formed on a fin extending from the substrate.

8. The method of claim 1, wherein the forming spacer elements includes forming a first spacer element abutting the first line element, wherein a first region of the first spacer element abutting the biased region of the first line element is noncollinear with a second region the first spacer element abutting the first region of the first line element.

9. The method of claim 8, further comprising:

using the first spacer element as a masking element to form a gate structure on the substrate, wherein the gate structure includes a first region that is noncollinear with a second region, the first region of the gate structure defined by the first region of the first spacer element and the second region of the gate structure defined by the second region of the first spacer element; and

forming a contact element on the first region on the gate structure.

10. The method of claim 1, wherein the forming spacer elements includes forming a first spacer element abutting the first line element, wherein a first region of the first spacer element abutting the biased region of the first line element is offset from a second region of the first spacer element abutting the first region of the first line element, wherein the offset is less than approximately 10 nm.

11. The method of claim 10, further comprising:

using the first region and the second region of the first spacer element as masking elements to etch the underlying layer disposed on the substrate.

12. A method of fabricating a semiconductor device, comprising:

forming a plurality of line elements on a substrate including a first line element having a first region with a first width and a biased region with a second width, the second width different than the first width;

forming spacer elements abutting sidewalls of each of the plurality of line elements;

after forming the spacer elements, removing the plurality of line elements from the substrate;

etching an underlying layer using the spacer elements after removing the plurality of line elements;

using the etched underlying layer as a masking element to form a gate structure; and

forming a contact element on the gate structure, wherein the contact element is formed on a shifted region of the gate structure, the shifted region being defined by the spacer element abutting a sidewall of the biased region of the first line element.

13. The method of claim 12, wherein the gate structure is disposed on a fin element extending from the substrate.

14. The method of claim 12, wherein the second width is less than the first width.

15. The method of claim 12, wherein the first width and the second width are defined by patterning using a photolithography process.

16. The method of claim 12, wherein the forming the plurality of line elements includes forming a plurality of photoresist features including a first photoresist feature having element having a first region of photoresist with the first width and a biased region of photoresist with the second width; and

using the plurality of photoresist features as masking elements to etch the plurality of line elements.

17. The method of claim 12, wherein the forming the plurality of line elements includes forming the plurality of line elements of polysilicon.

18. The method of claim 12, wherein the forming spacer elements includes depositing an oxide layer and etching the deposited oxide layer.

19. The method of claim 12, further comprising:

forming the underlying layer comprising hard mask material on the substrate.

20. A method of fabricating a semiconductor device, comprising:

forming a contiguous line element having a first region with a first width and wherein the contiguous line element includes a biased region with a second width, the second width different than the first width;

forming spacer elements abutting sidewalls of the continuous line element at the first region and the biased region;

after forming the spacer elements, removing the contiguous line element; and

using the formed spacer elements as a masking element during an etching process, wherein the etching process etches an underlying layer, and wherein the underlying layer is a layer of a gate structure.