DEVICE HAVING A CONTACT BETWEEN SEMICONDUCTOR REGIONS THROUGH A BURIED INSULATING LAYER, AND PROCESS FOR FABRICATING SAID DEVICE

FIELD OF THE INVENTION

The field of the invention is that of semiconductor devices produced on a semiconductor-on-insulator (SeOI) substrate.

BACKGROUND OF THE INVENTION

Such an SeOI substrate comprises a thin layer of semiconductor material separated from a base substrate by means of a buried insulating layer.

A semiconductor device produced on such a substrate generally has a conducting region produced in the thin layer above the insulating layer, for example a drain region or a source region of an FET transistor, or else an emitter region of a bipolar transistor associated with an FET transistor in order to inject charge into the channel of the FET transistor.

A semiconductor device on an SeOI substrate may also include a conducting region produced in the base substrate beneath the insulating layer, for example a buried back control gate region facing the channel of an FET transistor.

Connections have to be made in order to supply these various types of conducting region. In general, these connections are produced on the front face side of the semiconductor substrate. Thus, there would typically be, for an FET transistor, a word line WL, a bit line BL and a source line SL which are connected to the front control gate region, the drain region and the source region respectively by means of metal connections produced on the front face side.

In general it is desirable to limit the number of metal connections so as to simplify the fabrication of the semiconductor device, especially as regards the lithography operations.

Moreover, it is in general desirable to limit the footprint of the semiconductor device (i.e. the area occupied by the latter). Now, making a

connection via the front face inevitably increases the footprint.

Even more generally, it is desirable to simplify as far as possible the production of these connections.

BRIEF DESCRIPTION OF THE INVENTION

A first aspect of the invention provides a semiconductor device produced on a semiconductor-on-insulator substrate comprising a thin layer of semiconductor material separated from a base substrate by means of a buried insulating layer, a source region and a channel region of a field effect transistor being arranged in the thin layer, wherein the device comprises:

- a first conducting region in the thin layer constituting the emitter of a bipolar transistor, the base of the bipolar transistor being formed by the source region and the collector of the bipolar transistor being formed by the channel region of the field effect transistor,
- a second conducting region in the base substrate constituting a buried injection line, and
- a contact connecting the first region to the second region through the insulating layer.

Certain preferred, but non-limiting, features of this device are the following:

- the first region, the second region and the contact have a conductivity of the same type;
- the contact is formed from a metallic interconnect material; and
- the first region and the second region have a conductivity of opposite type and the contact has an upper region, the conductivity of which is of the same type as that of the first region, and a lower region, the conductivity of which is of the same type as that of the second region.

According to another aspect, the invention provides a process for fabricating a semiconductor device on a semiconductor-on-insulator substrate comprising a thin layer of semiconductor material separated from a base substrate by means of an insulating layer, the device comprising a source region and a channel region of a field effect transistor in the thin layer, the process comprising the formation:

- of an injection line buried in the base substrate,
- of an emitter of a bipolar transistor in the thin layer, the base of the bipolar transistor being formed by the source region and the collector of the bipolar transistor being formed by the channel region of the field effect transistor,
- of a contact connecting the emitter to the buried injection line through the insulating layer.

Certain preferred, but non-limiting, features of this process are the following;

- to form the contact, the following steps are carried out:
  - etching of the semiconductor substrate in order to form therein a trench extending beyond the buried insulating layer, through the emitter, until reaching the buried injection line; and
  - filling of the trench with an interconnect material;
- the interconnect material is a semiconductor material;
- the interconnect material is predoped;
- it further includes a step of doping the semiconductor material in the trench;
- an upper region and a lower region of the trench are oppositely doped;
- the boundary between the upper region and the lower region is located level with the insulating layer;
- the boundary between the upper region and the lower region is located level with the thin layer above the first region; and
- the interconnect material is metallic.

BRIEF DESCRIPTION OF THE DRAWINGS

Other features, objects and advantages of the present invention will become more clearly apparent on reading the following detailed description of preferred embodiments thereof, given by way of non-limiting example and with reference to the appended drawings in which:

- Figure 1 shows one possible embodiment of a buried bit line beneath the insulating layer and connected to a drain region of an FET transistor by means of a contact through the insulating layer;
- Figure 2 shows one possible embodiment of a buried source line beneath the insulating layer and connected to a source region SL by means of a contact through the insulating layer;
- Figure 3 shows one possible embodiment of a buried injection line beneath the insulating layer and connected to an emitter region of a bipolar transistor by means of a contact through the insulating layer;
- Figure 4 shows two conducting regions of a semiconductor device, a first region being placed in the thin layer, whereas the second region is placed in the base substrate;
- Figure 5 shows the production of a trench extending beyond the buried insulating layer, through the first region, right into the second region;
- Figure 6 shows the filling of the trench with an interconnect material;
- Figures 7a and 7b show two alternative ways of etching the interconnect material, carried out with and without a lithography mask respectively;
- Figure 8 illustrates an embodiment in which the first conducting region does not contact the front face of the SeOI substrate; and
- Figure 9 illustrates an embodiment in which the first region and the second region have conductivities of opposite type.

DETAILED DESCRIPTION OF THE INVENTION

The object of the invention is to provide, in a simple manner, a line for connection to a semiconductor region of a semiconductor device on an SeOI substrate.

More particularly, the aim of the invention is to limit the footprint of the device and to limit the use of metal connections.

To do this, the invention proposes to connect said semiconductor region to another semiconductor region placed in the SeOI substrate on the other side from the insulating layer by means of a contact through the insulating layer.

Thus, when considering a first semiconductor region placed in the thin layer of the SeOI substrate, this first region is connected, by means of a contact through the insulating layer, to an access line formed by a second semiconductor region in the base substrate beneath the buried insulating layer.

Conversely, when considering a first semiconductor region placed in the base substrate, this first region is connected, by means of a contact through the insulating layer, to an access line formed by a second semiconductor region in the thin layer above the buried insulating layer, by means of a contact through the insulating layer.

The first situation relates for example to a first region in the thin layer of the drain-region or source-region type of an FET transistor. The invention therefore makes it possible to bury the bit line BL or the source line SL in the base substrate beneath the insulating layer.

The first situation also relates to a first region in the thin layer of the emitter-region type of a bipolar transistor associated with an FET transistor in order to inject charge into the channel of the FET transistor. The invention therefore makes it possible to bury the injection line IL connected to the emitter region in the base substrate beneath the insulating layer.

The second situation relates for example to a first region in the base substrate of the back control gate region type, placed beneath the insulating

layer facing the channel of an FET transistor. The invention therefore makes it possible to access this buried back control gate via the front face of the SeOI substrate with a back control gate drive line.

In the context of the invention, the expression "connection between semiconductor regions" is understood to mean both an ohmic junction between semiconductor regions having a conductivity of the same type and a pn junction between semiconductor regions having conductivities of opposite type.

Figures 1 to 3 show a sectional view of a semiconductor device according to one possible embodiment of the first aspect of the invention produced on an SeOI (semiconductor-on-insulator) substrate, preferably an SOI (silicon-on-insulator) substrate, comprising a thin layer of semiconductor material separated from a base substrate by means of a buried insulating layer.

The insulating layer is for example a BOX (buried oxide) layer, typically an SiO_2 layer.

The semiconductor device here is a DRAM memory cell (DRAM standing for dynamic random access memory). The memory cell comprises an FET transistor having a source S, a drain D1 and a floating channel C1. A gate dielectric layer and a control gate electrode are deposited in sequence above the floating channel C1.

The drain D1 and the source S are preferably in contact with the buried oxide layer BOX so that the FET transistor is fully depleted.

The source S may thus be shared between two adjacent memory cells (it thus also serves as source region for the FET transistor having a drain D2 and a channel C2). Such sharing enables the footprint of a memory cell to be reduced.

The drain D1 is connected to a bit line BL, the source S is connected to a source line SL and the control gate is connected to a word line WL1.

In the context of the embodiment shown in Figure 1, the drain D1 constitutes a first semiconductor region (for example n^+-doped in the case of

an npn-FET transistor) in the thin layer, the drain D1 being connected, by means of a contact I1 through the insulating layer BOX, to a bit line BL buried in the base substrate beneath the insulating layer BOX. The bit line BL thus forms a second semiconductor region in the base substrate.

As shown in Figure 1, the bit line BL may especially be placed so as to connect the drain regions D1, D2 together along one row of a memory array, with a contact I1, I2 through the insulating layer provided for each of the drain regions.

In the context of the embodiment shown in Figure 2, the source S constitutes a first semiconductor region (for example n^+-doped in the case of an npn-FET transistor) in the thin layer, the source S being connected, by means of a contact I_N through the insulating layer BOX, to a source line SL buried in the base substrate beneath the insulating layer BOX. The bit line SL thus forms a second semiconductor region in the base substrate.

It should be pointed out that the source line SL may especially be placed so as to connect the source regions together along one row of a memory array, with a contact through the insulating layer provided for each of the source regions. The buried source line SL is thus parallel to the word lines WL1, WL2.

In the context of the embodiment shown in Figure 3, a bipoplar transistor, the base of which is formed by the source S of the FET transistor and the collector of which is formed by the channel C1 of the transistor, is associated with the FET transistor in order to inject charge into the channel C1. The bipolar transistor has an emitter E which constitutes a first semiconductor region (for example p^+-doped in the case of an npn-FET transistor) in the thin layer. The emitter E is connected, by means of a contact I_P through the insulating layer BOX, to an injection line IL buried in the base substrate beneath the insulating layer BOX. The injection line IL thus forms a second semiconductor region in the base substrate.

In the examples shown in Figures 1 to 3, the first regions and the second regions have a conductivity of the same type (n^+ in Figures 1 and 2,

p^+ in Figure 3) and the interconnects I1, I2, I_N, I_P are therefore produced by means of a semiconductor material having a conductivity of the same type.

It will be understood that producing access lines with a doped semiconductor material avoids having to use metal connections.

Furthermore, the fact of burying these lines frees up surface on the front face. This architecture is also relatively flexible in so far as a buried access line may extend beneath a plurality of memory cells, a single connection then being necessary for addressing the line and consequently said plurality of cells.

It will also be understood that the buried lines (bit line in Figure 1, source line in Figure 2, injection line in Figure 3) are preferably isolated from the base substrate by means of a well W of opposite conductivity, in order to create a diode serving as both lateral and underlining isolation.

However, the invention also extends to the case in which the first region and the second region are of opposite conductivity. In this situation, the contact enables a p-n junction to be produced.

The contact may therefore have an upper region of the same conductivity type as that of the first region and a lower region of the same conductivity type as that of second region.

In an alternative embodiment, the contact may be produced by means of a material of metallic nature, especially a silicide (for example $WSiO_2$).

It should be noted that although memory transistors have been shown in Figures 1, 2 and 3, it is however obvious that the invention applies to all types of connection between logic MOS transistors.

Various embodiments of a semiconductor device according to the first aspect of the invention will be described below with reference to Figures 4-9.

Figure 4 shows an SeOI substrate comprising a thin layer 1 separated from a base substrate 2 by means of a buried insulating layer 3. The thin layer 1 typically has a thickness of between a few nm and a few tens of nm depending on whether the device is fully depleted or partially depleted. The insulating layer 3 itself has a thickness typically between one nm and several

tens of nm.

A first semiconductor region 4 is placed in the thin layer 1 above the insulating layer, while a second semiconductor region 5 is placed in the base substrate beneath the insulating layer.

It will be understood that the first and second regions 4, 5 are not necessarily produced before the formation of the interconnect described below, but they may be produced during this formation, or even once the interconnect has been formed.

Referring to Figure 5, the semiconductor substrate is etched so as to form therein a trench 6 extending beyond the buried insulating layer, through the first region 4, until reaching the second region 5.

As shown in Figure 6, the trench 6 is then filled with an interconnect material 7.

The interconnect material may be metallic (for example a silicide: $WSiO_2$). Thus, an ohmic contact is made through the insulating layer between the first region 4 and the second region 5.

The interconnect material is preferably a semiconductor material, typically the same material as that of the thin layer of the SeOI substrate.

Taking for example an SOI substrate, amorphous or polycrystalline silicon is deposited on the surface of the SOI substrate in order to fill the trench.

Alternatively, an atomic layer of silicon may be deposited by ALD (atomic layer deposition).

Next, a lithography mask is positioned on the surface of SeOI substrate, the mask covering the regions that it is desired to retain. A material deposited in the regions not covered is then etched (cf. Figure 7a).

As a variant (cf. Figure 7b), a lithography mask is not used and a localized etching operation of the RIE (reactive ion etching) type is carried out so as to remove all of the material deposited on the surface of the substrate.

The deposited material is preferably doped. Thus, when the regions to

be connected are both of n^+-type conductivity (cf. Figures 1 and 2) or both of p^+-type conductivity (cf. Figure 3), the deposited material is of n^+-type or p^+-type conductivity respectively.

It should be noted that the method may therefore require two passes: one for filling certain trenches with n^+-Si and the other for filling other trenches with p^+-Si. It is then preferable to use a lithography mask in order to avoid any risk of a short circuit.

In this regard, it should be noted that making metallic interconnects requires only one filling pass.

As a variant, the material may be doped subsequently. When the two regions to be connected have the same conductivity type, the regions of the trench which are lying in the first region, in the insulating layer and in the second region are then doped with the same type.

In the case shown in Figure 8 in which the first region 4 is not in contact with the front face of the SeOI substrate, an upper region 8 and a lower region 9 of the trench have conductivities of opposite type, with the boundary between the upper region and the lower region located level with the thin layer 1 above the first region 4. Thus, when the regions to be connected are of p^+-type, the lower region of the trench is of p^+-type and the upper region of n^+-type above the first region 4, the junction being made in the thin single-crystal layer. These conductivities of opposite type may be obtained by implantation or by epitaxy, with n^+-type doping in the upper region and p^+-type doping in the lower region in the example shown.

The invention also extends to the case shown in Figure 9 of first and second regions to be connected that have conductivities of opposite type, with a contact of the p-n junction type. The procedure is then in the manner just described by forming, in the trench, an upper region 8 and a lower region 9 of opposite conductivity type (the upper region having a conductivity of the same type as that of the first region, for example n^+-type, the lower region having a conductivity of the same type as the second region, for example p^+-type). The boundary between the lower and upper regions of the trench

defines the location of the p-n junction. This junction is preferably chosen to be level with the insulating layer.

It should also be noted that if the trench is filled with undoped semiconductor material, it is also possible to carry out an annealing operation so that the dopants from the first region 4 and from the second region 5 diffuse back into the contact. The level of doping of the first region 4 and of the second region 5 must therefore be initially very high (of the order of 10^{20}) in order to take into account the dilution of this level of doping towards the contact. If the regions 4 and 5 have the same polarity, ohmic contact is created. In contrast, if the regions 4 and 5 are oppositely doped, a diode is created. It should be understood that the diode thus created makes it possible in particular to associate a bipolar transistor with a memory cell (cf. Figure 3 also) by forming a fourth drive electrode for the injection, thereby permitting the memory cell to be operated at a lower voltage for writing and for erasure.

CLAIMS

1. Semiconductor device produced on a semiconductor-on-insulator substrate comprising a thin layer of semiconductor material separated from a base substrate by means of a buried insulating layer, a source region and a channel region of a field effect transistor being arranged in the thin layer, wherein the device comprises:

- a first conducting region in the thin layer constituting the emitter of a bipolar transistor, the base of the bipolar transistor being formed by the source region and the collector of the bipolar transistor being formed by the channel region of the field effect transistor,
- a second conducting region in the base substrate constituting a buried injection line, and
- a contact connecting the first region to the second region through the insulating layer.

2. Device according to claim 1, wherein the contact is formed from a doped semiconductor interconnect material.

3. Device according to claim 1, in which the contact has a lower region the conductivity of which is of the same type as that of the first region, and an upper region of opposite conductivity.

4. Device according to claim 3, wherein the boundary between the upper region and the lower region is located level with the insulating layer.

5. Device according to claim 3, wherein the boundary between the upper region and the lower region is located level with the thin layer above the first region.

6. Process for fabricating a semiconductor device on a semiconductor-on-insulator substrate comprising a thin layer of semiconductor material separated from a base substrate by means of an insulating layer, the device comprising a source region and a channel region of a field effect transistor in the thin layer, the process comprising the formation:

- of an injection line buried in the base substrate,
- of an emitter of a bipolar transistor in the thin layer, the base of the bipolar transistor being formed by the source region and the collector of the bipolar transistor being formed by the channel region of the field effect transistor,
- of a contact connecting the emitter to the buried injection line through the insulating layer.

7. Process according to Claim 6, in which, to form the contact, the following steps are carried out:

- etching of the semiconductor substrate in order to form therein a trench extending beyond the buried insulating layer, through the emitter, until reaching the buried injection line; and
- filling of the trench with an interconnect material.

8. Process according to Claim 7, in which the interconnect material is a predoped semiconductor material.

9. Process according to Claim 7, in which the interconnect material is a semiconductor material and which further includes a step of doping the semiconductor material in the trench.

10. Process according to claim 9, in which doping the semiconductor

material in the trench is performed by an annealing operation that diffuse dopants in the trench.

11. Process according to one of claims 8-10, in which an upper region and a lower region of the trench are oppositely doped.

12. Process according to Claim 11, in which the boundary between the upper region and the lower region is located level with the insulating layer.

13. Process according to Claim 11, in which the boundary between the upper region and the lower region is located level with the thin layer above the first region.