1318770

PATENT SPECIFICATION (11) 1 318 770

DRAWINGS ATTACHED

(21) Application No. 58591/70 (22) Filed 10 Dec. 1970 (19)
(31) Convention Application No. 885 605 (32) Filed 16 Dec. 1969 in
(33) United States of America (US)
(44) Complete Specification published 31 May 1973
(51) International Classification B28D 5/06
(52) Index at acceptance
B6J 1 301 30Y 314 350 351 352 362 365 440 491 492 500 530 53Y 550 702 710 71X 750
H1K 217 288 312 341 345 34Y 351 54Y 551 552 553 55Y 573 578 579 57Y 581 583 591 59Y 611 615 616 619 61Y

(72) Inventor HERBERT ATKIN WAGGENER

(54) METHODS OF ETCHING SEMICONDUCTOR BODIES

(71) We, WESTERN ELECTRIC COMPANY, INCORPORATED, of 195 Broadway, New York City, New York State, United States of America, a Corporation organized and existing under the laws of the State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates generally to methods for making semiconductor devices including an etching step.

In the manufacture of semiconductor devices, it is often necessary to shape the starting semiconductor material in a desired manner. Since the devices are generally of very small size, mechanical shaping is generally not feasible and chemical methods, such as etching are used. Electrochemical methods have also been suggested but most of these have limitations, such as, for example, being suitable mainly for a particular material, for example, germanium, or material of a particular conductivity type or material of a particular range of resistivity. These previous methods in general are not suitable for dealing with silicon bodies, particularly of the integrated circuit type, where it is generally desired to remove the high resistivity portions from a relatively low resistivity epitaxial layer. More specifically, it is more commonly desired to remove a relatively high resistivity substrate or bulk portion from an overlying epitaxial or diffused layer of a relatively lower resistivity, without regard to the type of semiconductivity, so that the remaining layer contributes only a minimum parasitic resistance to devices fabricated therein or thereon.

According to the present invention a method of making a semiconductor device includes the steps of inserting a semiconductor body in an etchant of the kind hereinafter defined in spaced relation to a counter-electrode and establishing a potential distribution in the body such that the portions not to be etched are maintained at at least the passivating potential with respect to the counter electrode and so that the portions to be etched are maintained at a potential less than the passivating potential with respect to the counter-electrode.

Thus, the semiconductor body is etched in a solution which is a chemical etchant for the semiconductor irrespective of semiconductivity type. That is, the etchant solution is of a type which is defined as one which etches the semiconductor at an appreciable rate unless there is a voltage applied thereto with respect to a counter-electrode immersed in said etchant, the voltage being greater than a predetermined passivation potential, for example, a silicon body of either type semiconductivity which is doped to a concentration of less than about 10^{20} atoms per cubic centimeter is etched relatively rapidly if simply immersed in a potassium hydroxide solution. However, if a positive potential of greater than about 0.5 volts with respect to a platinum counter-electrode is applied to the silicon body, all those portions of the silicon which are at least about 0.5 volts positive are substantially passivated. That is, those portions at least about 0.5 volts positive are etched at a rate of at least 10 times slower (typically 200—10,000 times slower) than those portions which are at a voltage less than about the 0.5 volts. For this reason, the "passivation potential" of this silicon-potassium hydroxide-platinum system is considered to be about 0.5 volts.

In some embodiments of the invention the semiconductor body includes a PN junction over which a voltage drop is maintained so that some portions of the semiconductor on one side of the PN junction are at a more positive potential than the passivation poten-

tial and those semiconductor portions on the other side of the PN junctions are at a potential less than the passivation potential. With this potential distribution, those semiconductor portions at a voltage less than the passivation potential are etched until enough material is removed so that the junction is exposed. Once the junction is exposed, the semiconductor passivates with respect to the solution and the etching effectively stops, i.e., the etch rate is reduced by a factor of at least an order of magnitude and typically by as much as 200—10,000.

In other embodiments of the invention a potential distribution is established within a semiconductor body by suitable placement of electrodes and potentials and using resistive and field effect techniques. Once this potential distribution is established in whatever configuration desired, the semiconductor will be etched in all those portions exposed to the etchant solution which are at a potential of less than the passivation potential.

The invention will be better understood from the following more detailed description of embodiments thereof taken in conjunction with the accompanying drawing, in which:

Fig. 1 shows schematically an arrangement for accomplishing the selective removal of P-type semiconductor material from N-type, in accordance with the invention;

Fig. 2 shows schematically an arrangement for accomplishing the selective removal of N-type semiconductor material from P-type, in accordance with the invention;

Figs. 3 and 4 show a portion of cross sections of semiconductive wafers which are conveniently etched in accordance with the invention;

Fig. 5 shows a portion of a semiconductor wafer prepared for etching selectively a slot to a predetermined depth in a semiconductor surface, in accordance with the invention; and

Fig. 6 shows a cross section of a portion of a semiconductor wafer illustrating one of the many possible ways of connecting a potential to a portion of the semiconductor body for controlling the selective etching in accordance with the invention.

With more specific reference now to the drawing, in Figs. 1 and 2 there is shown schematically the basic apparatus for carrying out the invention. As shown, the apparatus comprises a suitable container 11 of a material resistant to the etchants 12 employed. A counter-electrode 13 is at least partially immersed in the etchant 12 and suitable means 14 for connecting the counter-electrode to external circuitry for the application of a controlling potential (+V) are provided. The counter-electrode advantageously is a material which does not dissolve and deleteriously contaminate the electrolyte, e.g., platinum or gold, or it may be of the same material as the body to be etched.

As shown in Fig. 1, a semiconductor body 15 includes a P-type portion which is to be etched and an N-type portion which is to remain after the etching ceases. Semiconductor 15 is immersed in the electrolyte in spaced relationship with the counter-electrode. Means 16 also are provided for connecting some portion of semiconductor 15 to the circuitry for providing the controlling potential (+V). It will be noted in Fig. 1 that the positive potential is connected only to the N-type portion of the semiconductor and that the P-type portion is separated from the N-type portion by a PN-junction 17.

It will be appreciated that means 16 are arranged such that the entirety of layer 17 is maintained at a potential greater than the passivation potential. Junction 17 provides a suitable voltage barrier so that the N-type portion can be maintained at a voltage greater than the passivation potential while the P-type portion is at a potential less than the passivation potential with respect to the counter-electrode 13.

As mentioned hereinabove, the etchant is selected from the class of chemical etchants which etch at an appreciable rate only those portions of the semiconductor which are at a potential less than some passivation potential with respect to the counter-electrode.

As the etching proceeds, the etching process is manifested by a visually observable evolution of hydrogen gas from the semiconductor surfaces being etched. Conversely, those surfaces which are not being attacked at an appreciable rate by the etchant evince no visually observable hydrogen evolution. Accordingly, the etching process can be conveniently monitored by observing the presence or absence of the hydrogen gas evolution.

However, once the P-type material is entirely removed so that the region around the position of metallurgical junction 17 is exposed to the etchant, all semiconductor surfaces exposed to the etchant are then at a potential greater than the passivation potential; and the etching substantially stops. This stoppage is evidenced by a sudden stopping of hydrogen gas evolution.

Once the hydrogen gas ceases to be evolved, the etch rate has been reduced by at least an order of magnitude and typically by as much as a factor of 200—10,000 compared with the etch rate during the time hydrogen gas is evolved.

Because of the considerable decrease in etching rate and because of the visually observable stoppage of hydrogen gas evolution, there is adequate time (which may be

of the order of hours) in which the remaining N-type semiconductor can be removed from the etchant before there has been appreciable attack thereon by the element. Of course the hydrogen gas evolution need not be detected visually and the semiconductor need not be removed from the etchant manually. It will be apparent that a hydrogen gas detector may be placed in or near the etchant and that electrical and mechanical means may be coupled to the gas detector so that the semiconductor is automatically withdrawn from the etchant when hydrogen gas has ceased to be evolved.

The illustration in Fig. 2 is substantially the same as that in Fig. 1 except that the semiconductor body 18 includes an N-type portion which is to be removed and a P-type portion which is to remain after the etching ceases. The N-type is removed by connecting P-type layer 19 to a voltage (+V) sufficient to maintain the entire P-type layer at a potential greater than the passivation potential.

Various modifications may be made to the aforementioned procedure. For example, the semiconductor body may be mounted with a wax or a resin to a premetallized conductive or dielectric carrier leaving only the surfaces to be etched exposed so that surfaces not to be etched are additionally protected from the etchant and so that handling of the semiconductor and application of controlling potentials thereby are facilitated.

The process in accordance with the invention can be practised with a variety of semiconductor materials, electrolytes, and counter-electrode materials. For the purpose of exposition only, the examples are directed to etching silicon.

Samples to be etched have included surface layers (either epitaxially formed or diffused, or both) over a bulk portion. Typically, the bulk has been doped to a concentration of less than about 10^{20} atoms per cubic centimeter. The thickness of the surface layer has been typically between about 1—15 microns; however, the thickness of the surface layer clearly is not critical. To facilitate handling in the electrolyte, the samples have been mounted using a resin or wax on a ceramic disc, and then immersed in the electrolyte which, for example, has been between about 1 and 7 normal potassium hydroxide. A platinum counter-electrode has been used, although any other material may be used provided it does not contaminate substantially the electrolyte used. Generally, the temperature of the electrolyte has been maintained at about 70 to 100 degrees Centigrade to produce an optimum etching rate. Although the rate is variable with applied bias, it has been found that P-type silicon doped to a concentration of about 10^{18} atoms per cubic centimeter etches at approximately 2—4 microns per minute in a 5 normal potassium hydroxide solution maintained at about 95 degrees Centigrade; and that when the junction is reached an oxide layer immediately grows upon the exposed surfaces. The etch rate of this oxide is about 200 times slower than the etch rate of the P-type material.

Although the aforementioned specific examples were described with respect to using potassium hydroxide as the etchant, the other alkali metal hydroxides may also be used. This group includes the hydroxides of sodium, rubidium, caesium, and lithium. Ammonium hydroxide and the alkyl substituted ammonium hydroxides, e.g., tetramethylammoniumhydroxide and tetraethylammonium-hydroxide, also may be used. Satisfactory results also may be had where aqueous mixtures of hydrofluoric acid and nitric acid are used as the etchant.

With more specific reference now to Figs. 3 and 4, there are shown cross sections of portions of semiconductor wafers having structures which are advantageously etched in accordance with the invention. In Fig. 3 there is shown a wafer portion *20* which includes a P-type substrate 21 over which there have been formed an N^+-type layer 22 and an N-type layer 23. A coating 24 of a material selected for its resistance to etching in the solution to be employed is shown over layer 23 for additional protection during the etching process. P-type layer 21 advantageously is of a relatively high resistivity, e.g., doped to an impurity concentration of less than of about 10^{18} acceptor atoms per cubic centimeter, so that spreading resistance within the bulk portion 21 itself would be sufficient to prevent a junction defect in the junction between layers 21 and 22 from providing enough current to cause the sample to passivate before the P-type 21 was completely removed. To perform the etching, an electrical connection is made to either the N^+-type layer 22 or to the N-type layer 23 or to both and then this electrical connection is supplied with a positive potential (+V), greater than the passivation potential with respect to the counter-electrode in the etching system. The structure shown in Fig. 3 is generally considered advantageous starting material for manufacturing air isolated monolithic circuits.

In Fig. 4 there is shown a similar structure to the one shown in Fig. 3, except that the conductivity types are reversed, i.e., a wafer portion *30* includes an N-type substrate 31 over which there has been formed a P^+ layer 32 and a less heavier doped P-type layer 33. Again, a coating 34 has been formed over the surface layers to provide additional protection from the etching solution during the etching process. To etch sample *30*, the P-type layer 33 or the P^+-type

layer 32 or both are connected to a potential positive with respect to the counter-electrode as in the aforementioned examples. However, it will be noted that there is a limit on the magnitude of positive potential which can be employed for this procedure since an excessive positive potential will forward bias the PN junction between layers 31 and substrate 32 and allow sufficient current to flow so that the N-type portion 31 will passivate rather than etch. Where wafer portion *30* includes silicon bulk portions and surface layers, and where the electrolyte used for etching is potassium hydroxide of about 7 normal and where the counter-electrode is platinum, a suitable potential to be applied to P^+ layer 32 is about 0.65 volts. This potential is sufficinetly high to cause P^+ layer 32 to passivate once the N-type substrate 31 has been etched away and yet is not sufficient to cause the PN-junction between layer 32 and N-type substrate 31 to become sufficiently forward biased to cause substrate 31 to passivate prior to its complete removal.

It should be noted at this point that with certain of the aforementioned etchant solutions, e.g., potassium hydroxide, there are different etch rates with respect to different crystallographic planes within the silicon semiconductor material. For example, using potassium hydroxide to etch silicon, it is well known that the etch rates as to planes parallel to the (100) crystallographic plane is considerably higher than the etch rate with respect to the planes parallel to the (III) crystallographic plane. In fact, the etch rate as to the (111) planes is so low that it may be difficult to determine when the etching has stopped when proceeding in accordance with the invention.

However, the aforemertioned etch rate limitation points toward another embodiment of the invention. There is shown in Fig. 5 a wafer portion prepared for selectively etching a surface slot therein. Wafter portion *40* includes a first semiconductor portion 41 contiguous with and forming a PN-junction with a layer 42 of opposite conductivity type. Over the surface of layer 42 there has been formed an apertured mask of a material which is resistant to the etchant solution to be employed. As in Figs. 3 and 4, the surface which is not to be etched at all, i.e., the surface of portion 41, is coated with an etch-resistant material 45 to provide additional protection during the etching process.

In accordance with this embodiment, the surface of layer portion 42 is made substantially parallel to the (100) plane of the semiconductor. The sample is placed in a potassium hydroxide solution, and the bulk portion 41 is connected to a source of positive potential equal to or greater than the passivation potential. Under these conditions, the exposed portion of layer 42 will be etched until the PN-junction between layers 42 and 41 is exposed at which time the etching will stop. The etching will only proceed laterally as far as the broken line side-lines 46A and 46B because of the preferential etch rates with respect to crystallographic planes, as described above. The technique of Fig. 5 may, of course, be used for forming voids of arbitrary shape and in particular for forming slots as are often used in dielectrical isolated integrated circuits. The depth of the void is, of course, controlled by the metallurgical position of the first PN-junction beneath the surface.

Referring now to Fig. 6, there is shown a portion *50* of a cross section of a semiconductor wafer illustrating one of the many possible ways of connecting a potential to a portion of a semiconductor body for controlling selective etching in accordance with the invention.

More specifically, wafer *50* has been prefabricated in accordance with the objective of producing an air isolated or dielectric isolated semiconductor integrated circuit. As shown, there is a relatively high resistivity P-type substrate 51 over which N^+-type layer 52 and less heavily doped N-type layer 53 have been formed, for example, by epitaxial deposition or by diffusion or by ion implantation or by any of the variety of other techniques well known in the art for altering the semiconductivity of a semiconductor body. Into layer 53 there have been formed localized zones 54A and 54B of P-type semiconductivity to provide resistors or base regions of transistors within the integrated circuit. Nested within P-type zones 54A and 54B are a plurality of N^+-type zones 55A and 55B for providing, for example, emitter zones of transistors within the integrated circuit. N^+-type zone 55C has been formed to enable easy fabrication of a low resistance contact to the collector of the transistor via an electrode 59 on the surface. A passivating dielectric layer 56 overlies the semiconductor surface in all portions except where metallic electrodes 57, 58, 60 and 61 extend through the dielectric layer to form a low resistance connection to the respective semiconductive zones therebeneath. Over the passivating dielectric layer 56 and over the aforementioned electrodes there has been formed a continuous and relatively uniform conductive layer 62, for example, of an inert metal such as platinum or gold.

To remove the P-type substrate 51 prior to etching slots from the bottom of layer 52 into the rest of the semiconductor to provide air isolation or dielectric isolation, the entire wafer *50* is immersed in an arrangement such as shown in Fig. 1; and the positive potential is applied to the conduc-

tive overlayer 62 which serves to distribute the potential and to protect the surface of the semiconductor from etching during the etch procedure. The potential is distributed through the conductive overlayer 62 and is applied substantially uniformly through a zone, such as zone 55C, to the N^+-type layer 52. In this manner the P-type material 51 is completely removed until the junction between P-type substrate 51 and N^+-type layer 52 is exposed. Once the junction is exposed, a current flows and an oxide layer grows on the then-exposed bottom of layer 52 and the semiconductor passivates.

The foregoing disclosure has been primarily in terms of monocrystalline silicon semiconductor material etched in a hot (70—100 degrees Centigrade) aqueous alkaline solution with a positive potential applied. It is to be understood that the upper limit (100°C) specified for the temperature range is not critical. Temperatures up to and including the boiling temperature may also be used.

It will be apparent to those skilled in the art that these procedures are generally applicable to other crystalline semiconductor materials, including germanium and the well-known III—V and II—VI compound semiconductors. The primary criterion is that the semiconductor be able to form an adherent passivating coating in the etching solution employed so as to achieve a substantial difference in etch rate for all those semiconductor portions to which there is applied a potential greater than the passivation potential.

WHAT WE CLAIM IS:—

1. Method of making a semiconductor device including the steps of inserting a semiconductor body in an etchant of the kind hereinbefore defined in spaced relation to a counter-electrode and establishing a potential distribution in the body such that the portions not to be etched are maintained at at least the passivating potential with respect to the counter-electrode and so that the portions to be etched are maintained at a potential less than the passivating potential with respect to the counter-electrode.

2. Method according to claim 1 including the step of maintaining the body in the etchant at least until all visible etching activity has ceased.

3. Method according to claim 1 or 2 wherein the body includes a rectifying barrier which is utilised in conjunction with potential establishing means so that the barrier separates the portions below passivating potential and those above passivating potential.

4. Method according to any preceding claim wherein the etchant is a hydroxide of an alkali metal or ammonium hydroxide or an alkyl-substituted ammonium hydroxide or an aqueous mixture of hydrofluoric acid and nitric acid.

5. Method according to claim 4 wherein the semiconductor is silicon and the etchant is an alkali metal hydroxide, the counter-electrode is of platinum or gold or silicon and the applied voltage is 0.5 volts or greater.

6. Method according to claim 5 wherein the etchant is potassium hydroxide and the voltage is 0.65 volts.

7. Method according to any preceding claim including the step of applying an etch-resistant coating to a portion of the semiconductor surface.

8. Method according to any preceding claim wherein the body is in the form of a thin layer of one conductivity type on a bulk portion of opposite conductivity type and forming a junction therewith, and etching is carried out so that the bulk portion or parts thereof are removed, until the junction is reached.

9. Method according to any preceding claim including the step of mounting the semiconductor body to be treated on to conductive or dielectric carrier.

10. Method according to any preceding claim including the step of heating the etchant.

11. Method according to any preceding claim including the steps of detecting the emission of hydrogen from the etching semiconductor by means of a hydrogen detector and actuating means for removing the semiconductor from the etchant in response to the cessation of hydrogen generation.

12. A method of making a semiconductor device by etching substantially as herein described with reference to any one of the Figures of the accompanying drawing.

13. A semiconductor device produced in accordance with the method of any one of the preceding claims.

P. S. BROWN,
Chartered Patent Agent,
5, Mornington Road,
Woodford Green, Essex.
Agent for the Applicants.

Printed for Her Majesty's Stationery Office by Burgess & Son (Aingdon), Ltd.—1973.
Published at The Patent Office, 25 Southampton Buildings, London, WC2A 1AY,
from which copies may be obtained.

tive overlayer 62 which serves to distribute the potential and to protect the surface of the semiconductor from etching during the etch procedure. The potential is distributed through the conductive overlayer 62 and is applied substantially uniformly through a zone, such as zone 55C, to the N^+-type layer 52. In this manner the P-type material 51 is completely removed until the junction between P-type substrate 51 and N^+-type layer 52 is exposed. Once the junction is exposed, a current flows and an oxide layer grows on the then-exposed bottom of layer 52 and the semiconductor passivates.

The foregoing disclosure has been primarily in terms of monocrystalline silicon semiconductor material etched in a hot (70—100 degrees Centigrade) aqueous alkaline solution with a positive potential applied. It is to be understood that the upper limit (100°C) specified for the temperature range is not critical. Temperatures up to and including the boiling temperature may also be used.

It will be apparent to those skilled in the art that these procedures are generally applicable to other crystalline semiconductor materials, including germanium and the well-known III—V and II—VI compound semiconductors. The primary criterion is that the semiconductor be able to form an adherent passivating coating in the etching solution employed so as to achieve a substantial difference in etch rate for all those semiconductor portions to which there is applied a potential greater than the passivation potential.

WHAT WE CLAIM IS:—

1. Method of making a semiconductor device including the steps of inserting a semiconductor body in an etchant of the kind hereinbefore defined in spaced relation to a counter-electrode and establishing a potential distribution in the body such that the portions not to be etched are maintained at at least the passivating potential with respect to the counter-electrode and so that the portions to be etched are maintained at a potential less than the passivating potential with respect to the counter-electrode.

2. Method according to claim 1 including the step of maintaining the body in the etchant at least until all visible etching activity has ceased.

3. Method according to claim 1 or 2 wherein the body includes a rectifying barrier which is utilised in conjunction with potential establishing means so that the barrier separates the portions below passivating potential and those above passivating potential.

4. Method according to any preceding claim wherein the etchant is a hydroxide of an alkali metal or ammonium hydroxide or an alkyl-substituted ammonium hydroxide or an aqueous mixture of hydrofluoric acid and nitric acid.

5. Method according to claim 4 wherein the semiconductor is silicon and the etchant is an alkali metal hydroxide, the counter-electrode is of platinum or gold or silicon and the applied voltage is 0.5 volts or greater.

6. Method according to claim 5 wherein the etchant is potassium hydroxide and the voltage is 0.65 volts.

7. Method according to any preceding claim including the step of applying an etch-resistant coating to a portion of the semiconductor surface.

8. Method according to any preceding claim wherein the body is in the form of a thin layer of one conductivity type on a bulk portion of opposite conductivity type and forming a junction therewith, and etching is carried out so that the bulk portion or parts thereof are removed, until the junction is reached.

9. Method according to any preceding claim including the step of mounting the semiconductor body to be treated on to conductive or dielectric carrier.

10. Method according to any preceding claim including the step of heating the etchant.

11. Method according to any preceding claim including the steps of detecting the emission of hydrogen from the etching semiconductor by means of a hydrogen detector and actuating means for removing the semiconductor from the etchant in response to the cessation of hydrogen generation.

12. A method of making a semiconductor device by etching substantially as herein described with reference to any one of the Figures of the accompanying drawing.

13. A semiconductor device produced in accordance with the method of any one of the preceding claims.

P. S. BROWN,
Chartered Patent Agent,
5, Mornington Road,
Woodford Green, Essex.
Agent for the Applicants.

Printed for Her Majesty's Stationery Office by Burgess & Son (Aingdon), Ltd.—1973.
Published at The Patent Office, 25 Southampton Buildings, London, WC2A 1AY,
from which copies may be obtained.

