Claims

1. A method used during fabrication of a semiconductor device, comprising:

providing a layer to be etched;

forming a sacrificial patterning layer over the layer to be etched, wherein the sacrificial patterning layer comprises a plurality of segmented portions having at least first and second cross sectional sidewalls;

forming a plurality of sacrificial first spacers, with one spacer formed on each sidewall of each segmented portion of the sacrificial patterning layer;

removing the sacrificial patterning layer;

forming a conformal second spacer layer over the plurality of sacrificial first spacers;

removing a portion of the conformal second spacer layer to form a plurality of second spacers on the sacrificial first spacers;

subsequent to forming the second spacers, removing the sacrificial first spacers; and

etching the layer to be etched using the second spacers as a pattern.

2. The method of claim 1 wherein each portion of the sacrificial patterning layer comprises a first width, and the method further comprises:

trimming the first width of each sacrificial patterning layer to have a second width which is about 25% narrower than the first width;

forming each of the plurality of first spacers to have a width which is about 25% of the first width; and

etching the conformal second spacer layer such that the second spacers each have a width which is about 25% of the first width.

3. The method of claim 2 further comprising etching the layer to be etched to form features from the layer to be etched, wherein each feature formed from the layer to be etched comprises a width which is about 25% of the first width.

4. The method of claim 3 further comprising:

forming the plurality of segmented portions of the sacrificial layer to have a pretrimmed pitch of about twice the first width; and

etching the layer to be etched to form the features to have a pitch which is about 25% of the pretrimmed pitch of the segmented portions of the sacrificial layer.

5. The method of claim 1 further comprising:

forming the sacrificial patterning layer such that the plurality of segmented portions have a first density; and

etching the layer to be etched using the second spacers as a pattern to form a plurality of features, wherein the plurality of features have a second density which is about four times the first density.

6. The method of claim 1 wherein each portion of the sacrificial patterning layer comprises a first width, and the method further comprises:

forming each of the plurality of first spacers to have a width which is about 33% of the first width;

etching the conformal second spacer layer such that the second spacers each have a width which is about 33% of the first width.

7. The method of claim 6 further comprising etching the layer to be etched to form features from the layer to be etched, wherein each feature formed from the layer to be etched comprises a width which is about 33% of the first width.

8. The method of claim 7 further comprising:

forming the plurality of segmented portions of the sacrificial layer to have a predetermined pitch of about twice the first width; and

etching the layer to be etched to form the features to have a pitch which is about 33% of the predetermined pitch of the segmented portions of the sacrificial layer.

9. The method of claim 1 further comprising:

forming the sacrificial patterning layer such that the plurality of segmented portions have a first density; and

etching the layer to be etched using the second spacers as a pattern to form a plurality of features, wherein the plurality of features have a second density which is about three times the first density.

10. The method of claim 1 further comprising forming the sacrificial patterning layer from photoresist.

11. The method of claim 1 further comprising forming the sacrificial patterning layer from a material selected from the group consisting of transparent carbon, multilayer resist, and bilayer resist.

12. A method used during fabrication of a semiconductor device, comprising:

providing a layer to be etched;

forming a sacrificial patterning layer over the layer to be etched, wherein the sacrificial patterning layer comprises a plurality of segmented portions each having a starting width which is about the same, an original pitch which is about twice the starting width, first and second cross sectional sidewalls, and a starting feature density;

selecting a desired feature reduction using the relationship *1/2m*, where "*m*" is an integer greater than or equal to 2 and the completed feature density will be about 2m times the starting feature density and the completed feature pitch will be about *1/2m* times the original pitch;

trimming the width of each segmented portion of the sacrificial first patterned layer by an amount about *1/2m* times the starting width;

forming a plurality of first spacers, with one spacer formed on each of the first and second sidewalls and each spacer having a target width about equal to *1/2m* times the starting width;

removing the sacrificial patterning layer;

forming a conformal second spacer layer on the plurality of first spacers;

removing a portion of the conformal second spacer layer to form a plurality of second spacers on the first spacers;

subsequent to removing the portion of the conformal second spacer layer:

if "*m*" is an even number, removing the first spacers such that the second spacers remain; or

if "*m*" is an odd number, removing the second spacers such that the first spacers remain; and

etching the layer to be etched using the remaining spacers as a pattern.

13. The method of claim 12 further comprising:

selecting "*m*" to be an even number;

removing the first spacers such that the second spacers remain; and

etching the layer to be etched using at least the second spacers as a pattern.

14. The method of claim 13 further comprising:

selecting the desired feature reduction to be *1/2m*, where "*m*" is 2 such that the completed feature density is about 4 times the starting feature density and the completed feature pitch is about ¼ times the original pitch;

removing the first spacers such that the second spacers remain; and

etching the layer to be etched using only the second spacers as a pattern.

15. The method of claim 13 further comprising:

selecting the desired feature reduction to be *1/2m* where "*m*" is an even number greater than or equal to 4;

forming a conformal third spacer layer over the first spacers and on the second spacers;

removing a portion of the conformal third spacer layer to form third spacers;

forming a conformal fourth spacer layer over the first and second spacers and on the third spacers;

removing a portion of the conformal fourth spacer layer to form fourth spacers;

removing the third and first spacers and leaving the second and fourth spacers; and

etching the layer to be etched using the second and fourth spacers as a pattern.

16. The method of claim 12 further comprising:

selecting the desired feature reduction to be an odd number;

forming a third spacer layer over the first spacers and on the second spacers;

removing a portion of the third spacer layer to form third spacers;

removing the second spacers and leaving the first and third spacers; and

etching the layer to be etched using at least the first and third spacers as a pattern.

17. The method of claim 15 further comprising:

selecting the desired feature reduction to be *1/2m*, where "*m*" is 3 such that the completed feature density is about 6 times the starting feature density and the completed feature pitch is about 1/6 times the original pitch; and

etching the layer to be etched using only the first and third spacers as a pattern.

18. A method used during fabrication of a semiconductor device, comprising:

providing a layer to be etched;

forming a sacrificial patterning layer over the layer to be etched, wherein the sacrificial patterning layer comprises a plurality of segmented portions each having a starting width which is about the same, an original pitch which is about twice the starting width, first and second cross sectional sidewalls, and a starting feature density;

selecting a desired feature reduction using the formula *1/(2m-1)*, where "*m*" is an integer greater than or equal to 2 and the completed

feature density will be about (2m-1) times the starting feature density and the completed feature pitch will be about *1/(2m-1)* times the original pitch;

forming a plurality of first spacers, with one first spacer formed on each of the first and second sidewalls and each first spacer having a target width about equal to 1/(2m-1) times the starting width;

removing the sacrificial patterning layer;

forming a conformal second spacer layer on the plurality of first spacers;

removing a portion of the conformal second spacer layer to form a plurality of second spacers on the first spacers;

subsequent to forming the plurality of second spacers on the first spacers:

if "*m*" is an even number, removing the first spacers such that the second spacers remain; or

if "*m*" is an odd number, removing the second spacers such that the first spacers remain; and

etching the layer to be etched using the remaining spacers as a pattern.

19. The method of claim 18 further comprising:

selecting "*m*" to be an even number;

removing the first spacers such that the second spacers remain; and

etching the layer to be etched using at least the second spacers as a pattern.

20. The method of claim 19 further comprising:

selecting the desired feature reduction to be *1/(2m-1)*, where "*m*" is 2 such that the completed feature density is about 3 times the starting feature density and the completed feature pitch is about 1/3 times the original pitch;

removing the first spacers such that the second spacers remain; and

etching the layer to be etched using only the second spacers as a pattern.

21. The method of claim 19 further comprising:

selecting the desired feature reduction to be *1/(2m-1)*, where "*m*" is an even number greater than or equal to 4;

forming a conformal third spacer layer over the first spacers and on the second spacers;

removing a portion of the conformal third spacer layer to form third spacers;

forming a conformal fourth spacer layer over the first and second spacers and on the third spacers;

removing a portion of the conformal fourth spacer layer to form fourth spacers;

removing the third and first spacers and leaving the second and fourth spacers; and

etching the layer to be etched using the second and fourth spacers as a pattern.

22. The method of claim 18 further comprising:

selecting the desired feature reduction to be an odd number;

forming a third spacer layer over the first spacers and on the second spacers;

removing a portion of the third spacer layer to form third spacers;

removing the second spacers and leaving the first and third spacers; and

etching the layer to be etched using at least the first and third spacers as a pattern.

23. A method used during fabrication of an electronic system, comprising:

fabricating a semiconductor device using a method comprising:

providing a layer to be etched;

forming a sacrificial patterning layer over the layer to be etched, wherein the sacrificial patterning layer comprises a plurality of segmented portions having at least first and second cross sectional sidewalls;

forming a plurality of sacrificial first spacers, with one spacer formed on each sidewall of each segmented portion of the sacrificial patterning layer;

removing the sacrificial patterning layer;

forming a conformal second spacer layer over the plurality of sacrificial first spacers;

removing a portion of the conformal second spacer layer to form a plurality of second spacers on the sacrificial first spacers;

subsequent to forming the second spacers, removing the sacrificial first spacers; and

etching the layer to be etched using the second spacers as a pattern;

providing a microprocessor; and

providing an electrical pathway between the semiconductor device and the microprocessor to facilitate electrical communication therebetween.

24. An in-process semiconductor device, comprising:

a layer to be etched; and

an etch mask comprising a plurality of planarized spacers, at least two of the spacers of the plurality comprising different materials, the spacers of the plurality having coplanar upper surfaces overlying the layer to be etched.

25. A semiconductor device, comprising:

an etched feature comprising a dimension which is *1/n* times a critical dimension of photolithography, where "*n*" is an integer greater than 2.

26. The semiconductor device of claim 25, further comprising:

the etched feature comprising the dimension which is *1/n* times a critical dimension of photolithography, where "*n*" is an odd integer greater than or equal to 3.

27. An in-process semiconductor device comprising:

a layer to be etched; and

a mask layer overlying the layer to be etched comprising a cross section having a plurality of separate, alternating first and second mask layer portions, wherein:

the first mask layer portions each comprise a single, vertically oriented pillar; and

the second mask layer portions each comprise a pair of vertically oriented pillars connected by a horizontally oriented segment.

28. The in-process semiconductor device of claim 27, further comprising a plurality of sacrificial spacers, with one of the plurality of sacrificial spacers interposed between each first and second mask layer portion.

The invention claimed is:

1. A method used during fabrication of a semiconductor device, the method comprising:

providing a layer to be etched, the layer to be etched having a substantially planar elevationally outermost surface; forming a plurality of sacrificial first spacers on the outermost surface;

forming a second spacer layer over the plurality of sacrificial first spacers;

removing a portion of the second spacer layer to form a plurality of triads of spacers on the outermost surface, the triads comprising the first spacer bracketed by second spacers on the surface with each of the spacers within the triad having a different elevational thickness and the second spacers contacting the first spacer;

forming a conformal layer over the triad;

removing a portion of the conformal layer to form groups of five adjacent spacers, the individual groups comprising the triad bracketed by third spacers; removing the second spacers;

and etching the layer to be etched using the first and third spacers as a pattern to form a plurality of substantially similar features within the layer to be etched.

2. The method of claim 1 wherein the etching forms recesses aligned substantially equidistant along the outermost surface of the layer to be etched.

3. The method of claim 1 wherein the surfaces of all of the spacers are non-planar.

4. The method of claim 1 wherein the forming the second spacer layer on the plurality of sacrificial first spacers comprises providing a spacing layer to fill between some of the first spacers but not filling between all of the first spacers.

5. The method of claim 4 wherein the spacing layer alternates between filled and unfilled between first spacers in one cross section of the device.

6. The method of claim 1 wherein each spacer within the group of five spacers has a different elevational thickness.

7. The method of claim 1 wherein the groups of five spacers are spaced apart from one another.

8. The method of claim 1 wherein individual spacers within the groups of five spacers contact one another.

9. The method of claim 1 wherein the groups of five spacers are spaced apart from one another a distance that is substantially the same as the width of the second spacers.

10. The method of claim 1 wherein upon removal of the second spacers, the remaining spacers are substantially equally spaced along the surface to be etched.