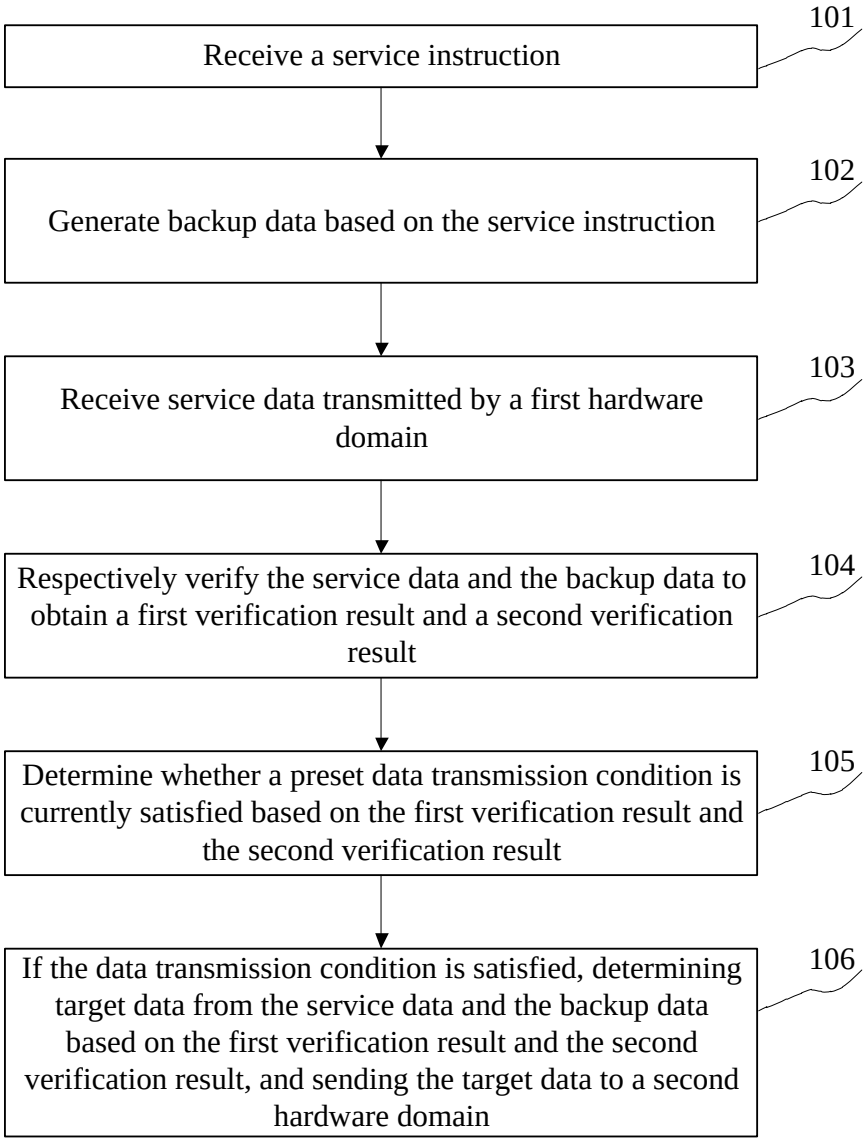

101
Receive a service instruction
102
Generate backup data based on the service instruction
103
Receive service data transmitted by a first hardware domain
104
Respectively verify the service data and the backup data to obtain a first verification result and a second verification result
105
Determine whether a preset data transmission condition is currently satisfied based on the first verification result and the second verification result
106
If the data transmission condition is satisfied, determining target data from the service data and the backup data based on the first verification result and the second verification result, and sending the target data to a second hardware domain

FIG. 1

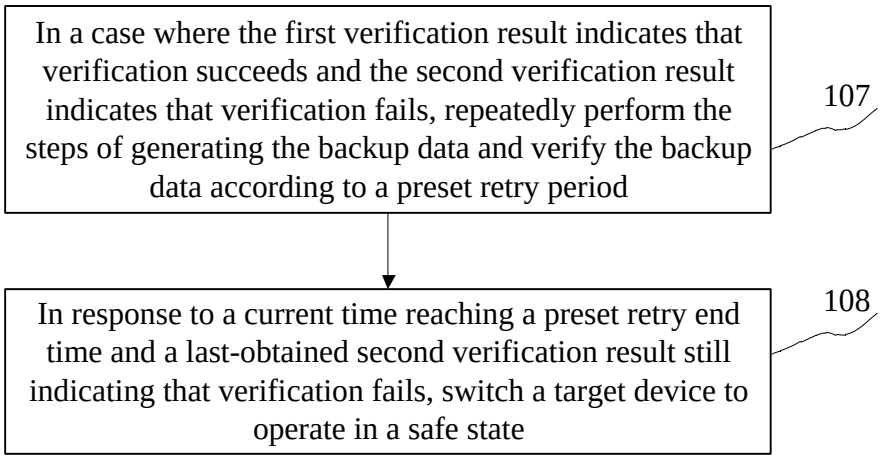

In a case where the first verification result indicates that verification succeeds and the second verification result indicates that verification fails, repeatedly perform the steps of generating the backup data and verify the backup data according to a preset retry period
107
In response to a current time reaching a preset retry end time and a last-obtained second verification result still indicating that verification fails, switch a target device to operate in a safe state
108

FIG. 2

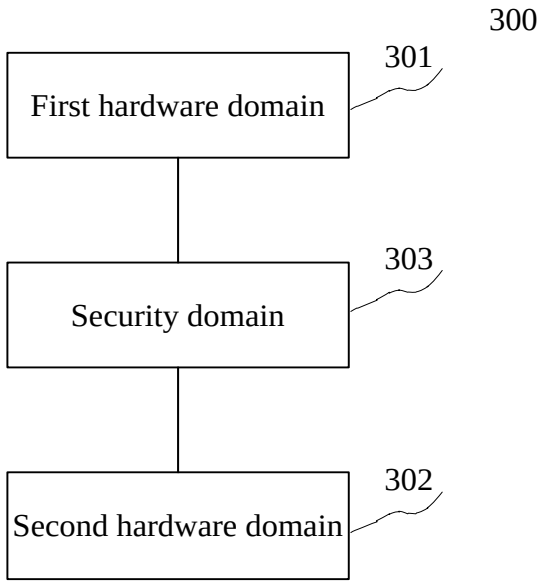

300
First hardware domain
301
Security domain
303
Second hardware domain
302

FIG. 3

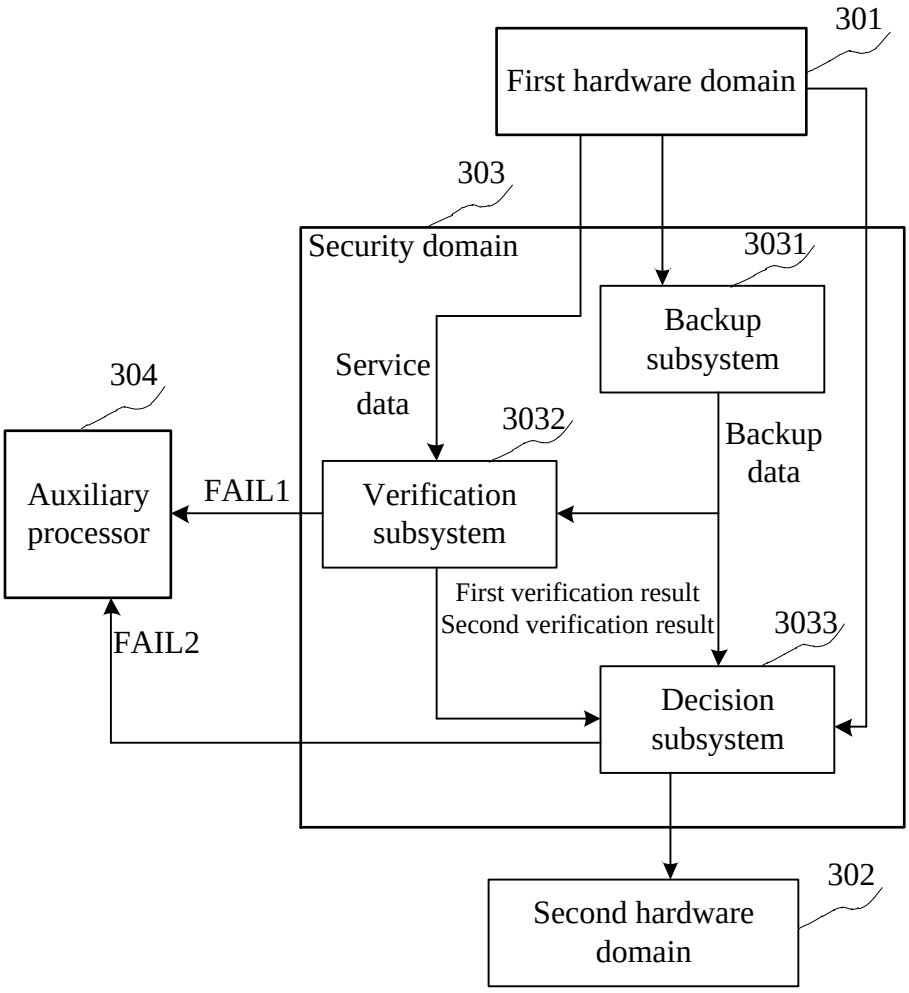

301
First hardware domain
303
Security domain
3031
Backup subsystem
Service data
304
3032
Backup data
Auxiliary processor
FAIL1
Verification subsystem
First verification result
Second verification result
3033
FAIL2
Decision subsystem
302
Second hardware domain

FIG. 4

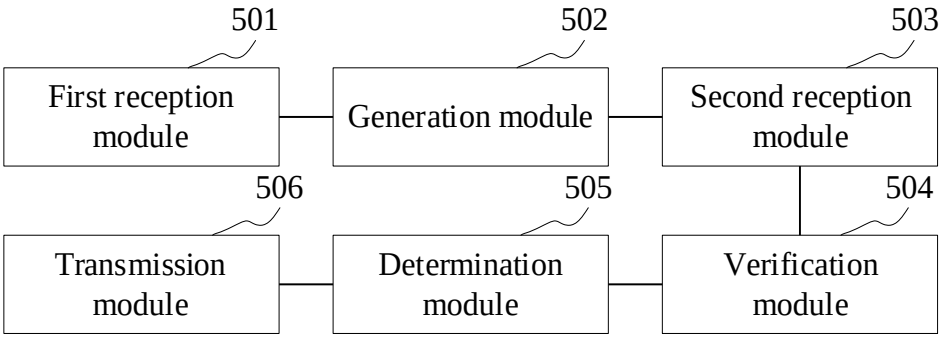

501
First reception module
502
Generation module
503
Second reception module
506
Transmission module
505
Determination module
504
Verification module

FIG. 5

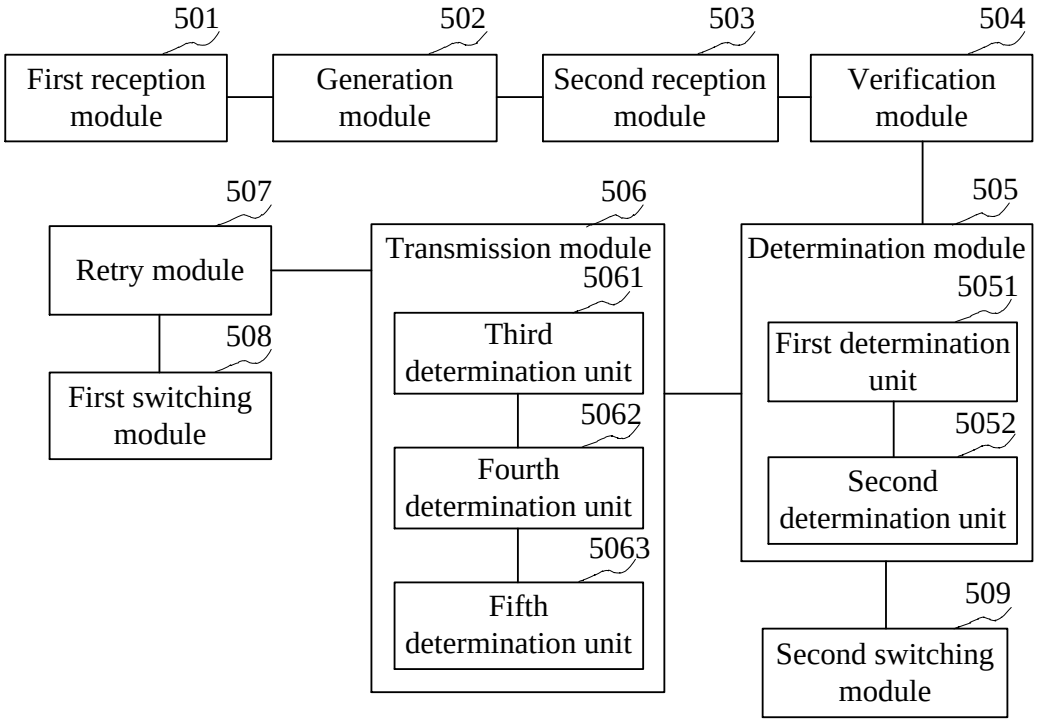

501
First reception module
502
Generation module
503
Second reception module
504
Verification module
505
Determination module
5051
First determination unit
5052
Second determination unit
506
Transmission module
5061
Third determination unit
5062
Fourth determination unit
5063
Fifth determination unit
507
Retry module
508
First switching module
509
Second switching module

FIG. 6

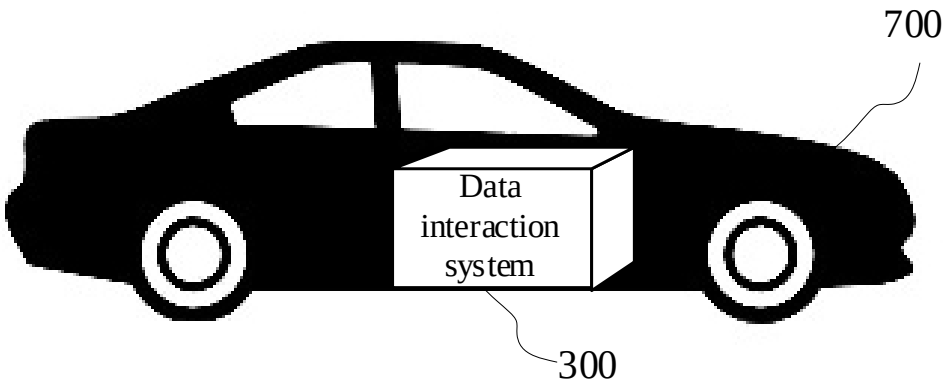

700
Data interaction system
300

FIG. 7

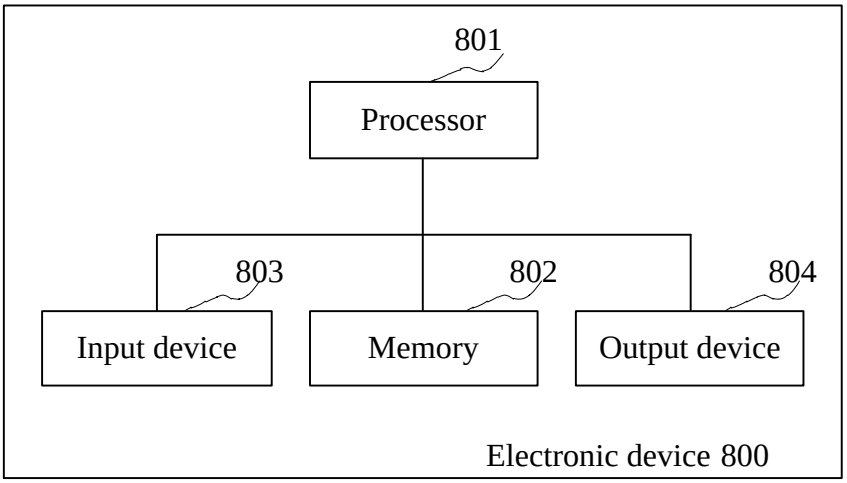

801
Processor
803
802
804
Input device
Memory
Output device
Electronic device 800

FIG. 8