

**DESCRIPTION**

**TITLE: Double Superlattices Obtained By Layer Transfer,  
Structure And Fabrication Process**

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**TECHNICAL FIELD OF THE INVENTION**

The invention generally relates to superlattices formed from at least one periodic stack of thin layers, and particularly to superlattices including semiconductor layers.  
10 More particularly, the invention relates to double superlattices.

**TECHNOLOGICAL BACKGROUND**

15 Superlattices have attracted attention because of their mechanical and semiconducting properties and also because they may be used to form quantum dots.

They have also been employed to develop what are known as nanosheet transistors or gate-all-around field-effect  
20 transistors (GAAFETs), the conduction channels of which are formed by a stack of layers of nanoscale thickness each encircled by a gate metal, as described in patents US 10,249,739 B2 and US 11,018,222 B1. The gate of these semiconductor structures surrounds the channel, hence the  
25 expression "gate-all-around".

This principle has been applied to form complementary field-effect transistors (CFETs) having a three-dimensional structure formed using a pair of stacked superlattices: a first superlattice formed on a substrate is used to form an n-  
30 type transistor while a second superlattice formed on the first superlattice is used to form a p-type transistor, or vice versa. This three-dimensional structure is advantageous in terms of integration compared to conventional approaches used to implement CMOS technology, which typically employs p-  
35 type transistors and n-type transistors fabricated side-by-

side in the same plane. In particular, the CFET approach in principle makes it possible to halve the footprint of a pair of p- and n-type transistors, or to shorten the connections between the two transistors and therefore decrease the electrical resistance of the corresponding connections. This approach is for example described in documents US 2019/0319095 A1, US 2021/0104523 A1 and US 2023/0326925 A1.

Regardless of whether nanosheet transistors or CFETs are concerned, the fabrication processes in question involve fabrication of superlattices comprising stacks of two types of alternating materials: one is intended to form the channel regions of the transistors, the other to form sacrificial layers that will be removed and replaced by a gate-dielectric and gate-metal structure during the fabrication of the transistors.

Document US 2021/082901 A1 discloses a method for fabricating high-density logic and memory, that includes stacking superlattices.

Document US 2023/197721 A1 discloses a process for fabricating stacked transistors.

Document WO 20181/30781 A1 discloses a process for fabricating an image sensor.

Fabrication of CFETs requires two types of transistors, one n-type and one p-type, to be stacked on top of each other. Two approaches are possible.

The first approach is said to be "sequential", in the sense that the transistors of two types are formed sequentially, in separate steps. In this approach, a semiconductor structure made of silicon or another semiconductor, or indeed a superlattice intended to form second nanosheet transistors, is transferred to a semiconductor substrate already carrying, for example, first nanosheet transistors. Initially, the first transistors are formed on the substrate, then the semiconductor structure is

transferred thereto, second transistors then being formed in the semiconductor structure. The thermal budget for the process of transferring the semiconductor structure and for forming the second transistors is limited by the need to not  
5 degrade the first transistors. Furthermore, the alignment of the second transistors with the first transistors must be extremely exact and specific electrical contact structures must be provided between the two stages.

The second approach is said to be "monolithic", in the  
10 sense that the first and second transistors are formed on the same substrate, at least some of the fabrication steps being applied simultaneously to all the layers in which the first and second transistors are formed. Reference may be made to document US 2019/0319095 A1. One of the main advantages of  
15 this approach is the self-alignment of the second transistors with the first transistors, which allows a higher density of transistors on the substrate, and decreases parasitic capacitances and resistances between the first and second transistors.

The monolithic approach requires thicker superlattices as  
20 starting structure than the sequential approach, since these superlattices form the base structure of two simultaneously fabricated superposed transistors. The superlattices are generally fabricated by epitaxy. However, the number of layers  
25 that can be stacked to form these superlattices is limited by the critical epitaxy thickness, beyond which the quality of the layers deposited degrades as a result of elastic relaxation and/or plastic relaxation. The monolithic approach is getting close to the critical epitaxy thickness and could  
30 require it to be exceeded.

Furthermore, the monolithic approach is technologically more complex to implement than the sequential approach, in particular when it is desired to form a dielectric separation layer between the first transistors and second transistors.

Such a layer makes it easier to integrate interior spaces into the structure and to form metal layers for the sources and drains of the transistors. The vertical distance between the first transistors and second transistors may be decreased to the thickness of the dielectric layer, with positive effects on the decrease in the parasitic capacitances and resistances between the first and second transistors. However, obtaining such a dielectric layer requires a complex procedure and use of a sacrificial layer that is removed so as to leave room for the dielectric layer. This sacrificial layer associated with the dielectric separation layer must be compatible with a sacrificial layer intended to form a space for accommodating the gate dielectric and metal layers. Thus, both sacrificial layers employed must be able to be etched selectively with respect to each other and with respect to the semiconductor forming the conduction channel of the transistors. Silicon is for example used for the channel, and silicon alloyed with various percentages of germanium is for example used for the sacrificial layers. From a technical point of view, although such structures may be employed, obtaining them remains complex and tricky.

One approach consists in forming two superlattices independently of each other on two separate substrates, then in transferring one to the other using a layer-transfer technology such as the so-called "Smart-Cut" method. One possible implementation of this approach consists in (a) forming a weakening plane within one of the two substrates via ion implantation of light species through the superlattice formed on this substrate, (b) joining the two superlattices to each other via a direct-bonding process such as molecular bonding, and then (c) splitting the implanted substrate in the weakening layer. One drawback of this approach is that it generally requires at least one heat treatment to heal the transferred layers, which are damaged by the transfer process

and in particular by the ion-implantation step. This heat treatment has a negative effect on the superlattices because it causes germanium ions to diffuse into the silicon.

Thus, there is a need for a process for fabricating superlattices or for joining superlattices that allows the critical epitaxy thickness to be exceeded, while limiting the damage inflicted by the process to the layers forming the superlattices.

#### **SUMMARY OF THE INVENTION**

The objective of the applicant is to provide a process for fabricating a structure able to facilitate integration and production of nanosheet transistors, and more specifically of CFETs, i.e. of superposed p-type and n-type transistors. This fabrication process should preferably be particularly suitable for the monolithic approach to CFET fabrication.

In order to achieve this goal, one aspect of the invention is a process for fabricating a structure comprising a superlattice stack, the process comprising the steps of forming a first superlattice on a first substrate, by stacking a plurality of first channel layers in alternation with a plurality of first sacrificial layers; forming a seed layer of a second superlattice by adding material to a second substrate; forming a weakening plane in the second substrate by implanting ions of a light species into the second substrate; forming an assembly by joining the seed layer to the first superlattice via a dielectric separation layer that separates the first superlattice from the seed layer and keeps them fastened to each other; removing a first part of the second substrate by splitting the second substrate in the weakening plane, and removing this part of the second substrate, after the joining step; uncovering the seed layer after the step of splitting the second substrate in such a way that the uncovered seed layer forms an exterior side of the

assembly, the uncovering step including removing a second part (Don<sub>a</sub>) of the second substrate that remained joined to the seed layer after the step of removing the first part of the second substrate; and forming the second superlattice on and in  
5 direct contact with the exterior side of the uncovered seed layer, by stacking a plurality of second channel layers in alternation with a plurality of second sacrificial layers.

A first advantage of the process is that it provides a stack of superlattices that may be either identical or  
10 distinct in composition and/or orientation.

A second advantage of the process is the ability of the structures obtained to exceed the critical epitaxy thickness, which limits the number and thickness of layers able to be grown epitaxially on top of one another without the crystal  
15 structures of these layers losing their quality.

A third advantage of the process lies in the provision within the stack itself of a separation layer between two superlattices, this layer potentially having structural characteristics incompatible with conventional superlattice  
20 formation processes. Specifically, superlattices are conventionally formed by successively depositing layers by epitaxy. However, with the present process, the separation layer may be made of a dielectric such as a nitride or oxide that may be amorphous, incompatible with formation by epitaxy  
25 of semiconductor layers of good crystal quality on the surface of this amorphous layer: on the contrary, deposition by epitaxy requires a crystalline base layer. The present invention thus makes it possible to employ any type of dielectric, for example SiN, SiCN, or SiO<sub>2</sub>, which can be chosen  
30 depending on its inherent dielectric characteristics and its compatibility with the steps provided for fabricating transistors based on stacking superlattices.

A fourth advantage of the process is a comparative advantage over an approach involving transferring the second

superlattice from a substrate on which it is independently formed to the first lattice, via the Smart-Cut method. In such a situation, a heat treatment for healing the transferred layer may be necessary, but is irrelevant in the present process. Thus, the present process limits the potential negative impact of a heat treatment on the superlattices and/or a structure accompanying them.

A fifth advantage stems from the intended applications of the superlattice stack, namely formation of CFETs. The dielectric separation layer may be configured to perform a function providing electrical insulation between the stacked transistors, but also to serve as an etch-stop layer allowing differential treatment of the transistors or integration of structures such as on the back side of the carrier substrate.

Thus, the fabrication process according to the invention is suitable for producing structures able to serve as base for a monolithic process for producing an electronic circuit integrating CFETs.

According to additional non-limiting features of the process according to the invention, which may be implemented individually or in any technically feasible combination:

- the weakening plane of the second substrate is formed by implanting ions of a light species into the second substrate through the seed layer;

- the separation layer may be continuously formed in a plane parallel to a surface of the first substrate on which the first superlattice is formed;

- the first channel layers and second channel layers may each be formed from a semiconductor, and the first sacrificial layers and second sacrificial layers may each be formed from a material that is capable of having a faster etch rate than the first channel layers and second channel layers, respectively;

- the first channel layers and second channel layers may each be formed from silicon, and the first sacrificial layers

and second sacrificial layers may each be formed from a silicon-germanium alloy;

- the process may comprise steps of: forming a first cap layer covering the first superlattice before the fastening step; and, forming a second cap layer covering the seed layer before the fastening step; in which process the fastening step comprises placing the first cap layer in contact with the second cap layer, the first cap layer and second cap layer together forming the separation layer;

- the first cap layer and second cap layer may each comprise silicon and at least one of the first cap layer and second cap layer may be formed from an oxide;

- at least one of the first cap layer and second cap layer formed from an oxide may be formed via a step of forming a silicon layer followed by a step of oxidising this silicon layer;

- the process may further comprise a step of forming at least one etch-stop layer on the second substrate prior to forming the seed layer, the etch-stop layer being removed in the step of uncovering the seed layer;

- the at least one etch-stop layer may be formed from a layer of the same material as the second sacrificial layers and from a layer of the same material as the second channel layers, the layer of the same material as the second sacrificial layers and the layer of the same material as the second channel layers being removed in the step of uncovering the seed layer.

#### **BRIEF DESCRIPTION OF THE FIGURES**

Other features and advantages of the invention will become apparent from the following detailed description of the invention, this description being given with reference to the appended figures, in which:

[Fig. 1] Figure 1 illustrates a fabrication process according to the invention;

[Fig. 2] Figure 2 illustrates a sequence of the process of Figure 1;

5 [Fig. 3] Figure 3 illustrates variants of structures able to be obtained with the process of Figures 1 and 2;

[Fig. 4] Figure 4 illustrates variants of the separation layers of Figure 3; and

[Fig. 5] Figure 5 is a flowchart summarizing the fabrication  
10 process of Figures 1 and 2.

## **DETAILED DESCRIPTION OF THE INVENTION**

### **Embodiment**

15 One embodiment of the present invention will now be described by means of Figures 1 to 5 and of the associated description below.

Figure 3 illustrates in (A) a structure Strc formed from a carrier substrate Car, from a first superlattice Stck1, from a separation layer Sep, and from a second superlattice Stck2, stacked in this order. The first superlattice Stck1 comprises a plurality of first layers Ch1 stacked in alternation with a plurality of first layers Sac1, preferably so that each first layer Ch1 is interposed between and in direct contact with two  
20 of the first layers Sac1. The second superlattice Stck2 comprises a plurality of second layers Ch2 stacked in alternation with a plurality of second layers Sac2, preferably so that each second layer Ch2 is interposed between and in direct contact with two of the second layers Sac2.

30 The first layers Ch1 and second layers Ch2 are layers formed from at least one semiconductor intended to form transistor channel regions and may be designated the first channel layers Ch1 and second channel layers Ch2,

respectively. These channel layers may be formed from the same material, or from different materials.

The first layers Sac1 and second layers Sac2 are layers formed from at least one material capable of having faster  
 5 etch rates than the first layers Ch1 and second layers Ch2, and may be designated the first sacrificial layers Sac1 and second sacrificial layers Sac2, respectively. These sacrificial layers may be formed from the same material, or from different materials. In particular, the layers Sac1 may  
 10 have a  $\text{Si}_{1-x}\text{Ge}_x$  composition and the layers Sac2 may have a  $\text{Si}_{1-y}\text{Ge}_y$  composition where  $x$  and  $y$  represent the proportions of germanium in the layers Sac1 and Sac2, respectively, with  $x$  possibly being different from or equal to  $y$ . These layers Sac1 and Sac2 of SiGe alloy may be associated with silicon layers  
 15 Ch1 and Ch2 by virtue of the epitaxial growth compatibility of these two materials, which possess a fairly similar lattice parameter. The proportions  $x$  and  $y$  are preferably less than 40%, and for example between 15% and 35%.

The second layers Sac1 and Sac2 are intended to serve as  
 20 sacrificial layers in a procedure for forming nanosheet transistors, in which the layers Sac1 and Sac2 are removed by etching, possibly chemical etching, so as to obtain a structure with floating strips formed from the layers Ch1 and Ch2. These floating strips will subsequently be encircled by a  
 25 layer of gate dielectric and by a gate metal so as to form nanosheet transistors.

Figures 1, 2 and 5 illustrate a process 500 for fabricating the structure Strc, which process is advantageously based on separate fabrication of a first  
 30 superlattice Stck1 and of a seed layer Init of a second superlattice Stck2 on two respective substrates, then transfer of the seed layer from the second superlattice Stck2 to the first superlattice Stck1. The structure Strc is then completed by fabricating the second superlattice Stck2 by stacking

successive layers on the seed Init. Figure 5 is a flowchart schematically showing the steps of the fabrication process 500.

Figure 1 illustrates in (A) formation of the first superlattice Stck1 on a carrier substrate Car, in a step 510<sub>Car</sub>. In this example, the carrier substrate Car is a single-crystal silicon wafer.

On a surface S<sub>Car</sub> of the substrate Car, layers Ch1 of silicon Si that are from 5 to 15 nm thick, and preferably from 7 to 10 nm thick, are grown by epitaxy, in alternation with layers Sac1 of a first silicon-germanium alloy of formula Si<sub>1-x</sub>Ge<sub>x</sub> that are from 5 to 10 nm thick, and preferably from 6 to 9 nm thick, where x is the percentage of germanium in the alloy, the layers preferably starting and ending with a layer Sac1. On the last layer Sac1, in a step 520<sub>Car</sub>, a cap layer Cap1 is formed, here from silicon Si, which layer has the function of preventing oxidation of the last layer Sac1. The layer Cap1 may have a thickness smaller than those of the layers Sac1 and Ch1 forming the superlattice Stck1, this thickness preferably being between 1 and 2 nm. The advantage of limiting the thickness to these values is to avoid the need, subsequently, to form an additional silicon channel in a transistor formed using the obtained superlattice stack.

Figure 1 illustrates in (B) formation of the seed layer Init and associated layers on a donor substrate Don, in steps 510<sub>Don</sub> to 530<sub>Don</sub>. In this example, the donor substrate Don is a single-crystal silicon wafer.

The seed layer Init is deposited on a surface S<sub>Don</sub> of the substrate Don in a step 520<sub>Don</sub>, the seed layer here being a layer of the first silicon-germanium alloy of formula Si<sub>1-x</sub>Ge<sub>x</sub> that is from 5 to 10 nm thick, and preferably from 6 to 9 nm thick. On this layer Init, a cap layer Cap2, which is made of silicon, is formed in a step 530<sub>Don</sub>. The function of the layer Cap2 is to prevent oxidation of the layer Init, and it is

preferably configured to be subsequently oxidised to form the bonding interface. The thickness of the layer Cap2 depends on the targeted thickness of the future oxidised layer. In other words, when aiming for an oxide layer with a thickness between  
 5 10 and 35 nm, the layer Cap2 in this case must have a thickness between about 4 and 16 nm. This layer Cap2 is optional, its advantageousness depending on how easily the material from which the last layer of the second superlattice Stck2 is formed oxidises and on the advantageousness of  
 10 integrating it into a dielectric separation layer between the two superlattices.

Optionally, before the seed layer Init is formed, it is possible to form, on the donor substrate Don, a layer Stp of the first silicon-germanium alloy of formula  $\text{Si}_{1-x}\text{Ge}_x$  having a  
 15 thickness between 5 and 10 nm, then a protective silicon layer Cap2' having a thickness between 1 and 5 nm, in a step 510<sub>Don</sub>. These two layers are etch-stop layers and are intended to protect the integrity of the seed layer Init during the fabrication steps that come after the donor substrate has been  
 20 split as described below and illustrated in (B) and (C) of Figure 2.

Figure 1 illustrates in (C) oxidation of the layer Cap2 of silicon Si to form a cap layer Ox2 of silicon oxide  $\text{SiO}_2$  that is from 10 to 35 nm thick, in an oxidising step 540<sub>Don</sub>. The  
 25 layer Cap2 is preferably oxidised right through or almost right through its thickness, so as to prevent a silicon layer from remaining after etching of the sacrificial layers.

The oxidation temperature and time used are limited to avoid exceeding the permitted thermal budget, so as to avoid  
 30 or at least limit diffusion of germanium from one layer of the superlattices to another, and in particular contamination of the entire thickness of the channel layers with germanium.

Figure 1 also illustrates in (C) implantation of light species (such as hydrogen, helium, or a combination of such

species) into the donor substrate Don through the layer  $S_{Don}$ , the seed layer Init and, where appropriate, the cap layer Ox2, so as to form a weakening plane Imp in the donor substrate Don, in a step 550<sub>Don</sub>.

5        Following formation of the weakening plane Imp, the donor substrate Don is flipped and the oxide layer Ox2 is brought into close contact with the silicon layer Cap1 and is joined thereto, for example by molecular bonding or any other joining technique in which surfaces of elements to be joined are  
10 placed in direct contact, so as to obtain the structure illustrated in (A) of Figure 2, in a joining step 560. The obtained structure is referred to as the assembly Ass. The separation layer Sep is formed in this step by bonding the last layers formed on the carrier substrate Car and on the  
15 donor substrate Don, respectively, and corresponds to the assembly formed from the layers separating the first superlattice Stck1 and second superlattice Stck2, the layers Cap1 and Ox2 in the present embodiment, as illustrated in Figure 3. This separation layer Sep preferably completely  
20 covers the donor substrate Don. Furthermore, the separation layer Sep is continuously formed in a plane parallel to the surface  $S_{Car}$  of the carrier substrate Car bearing the first superlattice Stck1. Even if the separation layer does not rigorously cover the entirety of the carrier substrate Car, it  
25 is at least continuously formed on a region in which a set of semiconductor components such as transistors, possibly a set of CFETs, is intended to be formed.

At this stage of fabrication, the seed layer Init is sandwiched between the carrier substrate Car and the donor  
30 substrate Don. This seed layer Init must be uncovered in order to make it accessible. This uncovering operation 570 is carried out in two successive steps 570A and 570B. Step 570A here consists in removing most of the donor substrate while step 570B consists in uncovering the seed layer Init by

removing the remainder of the donor substrate. The uncovered seed layer Init forms an exterior side  $F_{\text{ext}}$  of the assembly Ass.

Figure 2 illustrates in (B) the donor substrate Don being  
 5 split in the weakening plane Imp, which is obtained by ion  
 implantation, so that part Don<sub>b</sub> is removed from the structure  
 illustrated in (A) while part Don<sub>a</sub> remains fastened thereto, in  
 the splitting and withdrawing step 570A. This split may be  
 obtained by heat treatment, optionally assisted by a split-  
 10 initiating mechanical force, using conventional layer-transfer  
 techniques that are well known in the field of  
 microelectronics.

Preferably, the carrier substrate Car and donor substrate  
 Don comprising the first superlattice Stck1 and the seed layer  
 15 Init, respectively, are substantially identical. This  
 advantageously makes it possible to easily produce them on a  
 large scale, thus facilitating their industrialisation.  
 Moreover, use of substantially identical carrier and donor  
 substrates advantageously makes it possible to obtain a joined  
 20 structure that is symmetrical and that has similar  
 coefficients of thermal expansion, which advantageously  
 prevents problems with mechanical deformation following the  
 bonding steps and future heat treatments.

Following assembly and splitting of the donor substrate, a  
 25 heat treatment may be applied so as to consolidate the joint  
 and heal the joined layers. The heat-treatment temperature and  
 time are limited to avoid exceeding the permitted thermal  
 budget, so as to avoid or at least limit diffusion of  
 germanium from one layer of the superlattices to another, and  
 30 in particular contamination of the entire thickness of the  
 channel layers with germanium. The heat treatment may  
 typically consist of an anneal of 2 h or less at a maximum  
 temperature of 750°C, and preferably of less than 700°C.

One alternative to the formation of a weakening plane and splitting of the donor substrate Don in this plane may consist in thinning the donor substrate Don after it has been joined, for example by etching, grinding and/or chemical-mechanical polishing (CMP). This thinning may be used to completely remove the second substrate Don if it is continued, for example, to the stop layer Stp.

Figure 2 illustrates in (C) the structure illustrated in (B) after it has been subjected to mechanical and/or chemical attacks to remove the part Don<sub>a</sub> of the donor substrate Don, the etch-stop layer Stp, and the protective layer Cap2' in step 570B. Thus, the seed layer Init is uncovered in this step, and accessible in the remainder of the fabrication process.

Next, the second superlattice Stck2 is formed. First, in a thin-film deposition tool, any native oxide is removed from the surface of the layer Init by virtue of the "in-situ" etching function available in many epitaxy tools, for example using HF gas. This operation makes it possible to clean the layer Init and guarantee the quality of its surface, in order to ensure the quality of the growth of the layers deposited on it. The second superlattice Stck2 is then formed directly on the seed layer Init, in an epitaxy step 580, and by epitaxial growth of layers Ch2 in alternation with layers Sac2. The operation of cleaning the layer Init prior to layer deposition is conventional and considered to form part of the step of forming the layers Ch2 and Sac2 by epitaxy. Alternatively, other known cleaning methods could be envisaged, such as complete oxidation of the layer Cap2' and its removal by HF directly in the tool. The main thing is to obtain a clean, non-oxidised surface before proceeding with the deposition of thin layers on this surface, whether the deposition sequence is started with a layer Sac2 or a layer Ch2.

The layers Ch2 are preferably made of silicon Si and have a thickness from 5 to 15 nm, and preferably a thickness from 7

to 10 nm, and the layers Sac2 are formed from the first silicon-germanium alloy of formula  $\text{Si}_{1-x}\text{Ge}_x$  and have a thickness from 5 to 10 nm, and preferably a thickness from 6 to 9 nm, preferably in such a way that each layer Ch2 is interposed  
 5 between and in direct contact with two of the first layers Sac2, the seed layer Init being considered to be one of the layers Sac2. Thus, it is possible either to grow a silicon layer Ch2 directly on the seed layer Init, which here is a layer of the first silicon-germanium alloy of formula  $\text{Si}_{1-x}\text{Ge}_x$ ,  
 10 or to start by forming a layer Sac2 of the first germanium alloy directly on the seed layer Init and then form a silicon layer Ch2 thereon, then to continue formation of the layers Ch2 and Sac2 in alternation.

The characteristics of the seed layer Init depend on this  
 15 step 580: this seed layer Init has a chemical nature and crystalline structure that are such as to allow the second superlattice Stck2 to be formed by successively growing layers by epitaxy. In the present case, since the second superlattice is formed from an alternation of layers Ch2 and Sac2, it is  
 20 appropriate to form a layer Init from one of these two types of layers. In the present case, it was chosen to form a layer Init from a silicon-germanium alloy of formula  $\text{Si}_{1-x}\text{Ge}_x$ . It is also possible to form the layer Init from another layer capable of forming a sacrificial layer with respect to the  
 25 layers Ch2, i.e. layers capable of having faster etch rates than the second layers Ch2. There are other alternatives, such as forming a layer Init made of silicon, or other materials favourable to formation by epitaxy of a layer of silicon (Si) or of an  $\text{Si}_{1-x}\text{Ge}_x$  alloy.

30 Forming the superlattice Stck2 after the transferring step advantageously makes it possible to avoid the need to subject it to a heat treatment intended to heal the effects of ion implantation on the layers of the superlattice. This type of healing heat treatment may prove to be indispensable for

semiconductor layers serving as an active layer in a transistor. Such a heat treatment may sometimes be carried out at a fairly high temperature, potentially causing diffusion of the germanium present in adjacent layers right through the channel layers.

The structure in (A) of Figure 3 shows the structure Strc formed from the carrier substrate Car, the first superlattice Stck1, the cap layer Cap1 formed from silicon, the silicon-oxide layer Ox2, and the seed layer Init, stacked in this order. The cap layer Cap1 and the silicon-oxide layer Ox2 form a dielectric separation layer Sep between the first superlattice Stck1 and second superlattice Stck2. The separation layer is considered to be a dielectric layer in that it is formed at least in part from a material that is considered to be dielectric, such as silicon nitride, silicon carbonitride, or silicon oxide. This structure is ready to be subjected to a monolithic process for forming CFETs.

The figures contain the indications "Si" or "SiGe" in the locations of certain layers, and in particular those forming the superlattices Stck1 and Stck2, in order to make them easier to read by indicating the compositions thereof for a given example. However, these indications should not be interpreted as limiting the nature of the layers thus annotated. Other materials, and in particular those mentioned in this description, may be used to form these layers.

Figure 3 illustrates in (A') and (A'') structures Strc' and Strc'', respectively, with possible variants Sep' and Sep'' of the separation layer Sep of the structure Strc. In (A), the separation layer Sep is formed by bonding the cap layer Ox2, which is formed from oxide, to the cap layer Cap1, these layers being the last layers formed on the donor substrate Don and on the carrier substrate Car, respectively.

A first variant illustrated in (A') consists in forming a silicon-oxide layer Ox1 as last layer formed on the carrier

substrate Car and in forming a silicon cap layer Cap2 as last layer formed on the donor substrate Don. Thus, the separation layer Sep' is formed by joining, by molecular bonding, the layer Ox1 to the layer Cap2.

5        A second variant illustrated in (A'') consists in forming two silicon-oxide layers as respective last layers formed on the substrates Car and Don. Thus, the separation layer Sep'' is formed by joining, by molecular bonding, these two silicon-oxide layers that, in the end, form a single silicon-oxide  
10    layer Ox.

      The separation layer Sep, which is also the layer linking the two superlattices to each other, need not necessarily be formed from crystalline silicon and/or amorphous silicon oxide obtained by oxidation of silicon. Thus, although Figure 1  
15    illustrates in (A) and (B) a process in which the oxide layer Ox2 is formed by oxidising a silicon layer, the oxide layer Ox2 could be formed by direct deposition of a silicon-oxide layer. This observation applies to the variants illustrated in (A') and (A'') of Figure 3 in respect of the layer Ox1 of (A')  
20    and to the oxide layers forming the layer Ox of (A'').

      The separation layer may also be composed of layers formed from amorphous silicon or other materials as long as they are compatible with the superlattice-treatment process envisaged below. Thus, generally, dielectrics, semiconductors or metals  
25    may be used to form the layers from which the separation layer is made, the main constraint being that these materials must take the form of layers of sufficiently high flatness and of sufficiently low roughness to be joined via a direct-bonding process such as molecular bonding. In the case where the  
30    superlattices are intended to form CFETs, dielectrics and/or semiconductors will preferably be used. For example, it is possible to employ one or a combination of the materials selected from silicon nitride (SiN), silicon carbonitride (SiCN), an oxide thereof (SiON, SiCNO<sub>x</sub>), or silicon oxide

(SiO<sub>2</sub>) deposited or formed via a low-temperature oxidation method. So-called "high-k" dielectrics such as HfO<sub>2</sub>, ZrO<sub>2</sub>, La<sub>2</sub>O<sub>3</sub>, Al<sub>2</sub>O<sub>3</sub>, TiO<sub>2</sub>, SrTiO<sub>3</sub>, their alloys or their alloys with silicon may also be employed. More generally, it is possible to employ any type of dielectric used in the semiconductor industry as dielectric layer, protective layer, hard mask or via coating (liner intended for TSVs, acronym of through-silicon vias).

Figure 4 illustrates such alternatives with, in (A), a separation layer Sep formed, in this order, from separation layers Sep<sub>a</sub>, Sep<sub>b</sub> and Sep<sub>c</sub>. The molecular bonding occurs in an interface plane Int located between the layers Sep<sub>c</sub> and Sep<sub>b</sub>, one of which is formed from silicon, amorphous silicon or silicon oxide, the other being formed from amorphous silicon or silicon oxide. The layer Sep<sub>a</sub> may be formed from silicon nitride, silicon carbonitride, silicon oxide or other dielectrics. The layers Sep<sub>a</sub> and Sep<sub>b</sub> may be formed on the donor substrate Don in place of the layer Ox<sub>2</sub>, and the layer Sep<sub>c</sub> may be formed on the carrier substrate Car in place of the layer Cap<sub>1</sub>. Alternatively, the layers Sep<sub>a</sub> and Sep<sub>b</sub> may be formed on the carrier substrate Car in place of the layer Cap<sub>1</sub>, and the layer Sep<sub>c</sub> may be formed on the donor substrate Don in place of the layer Ox<sub>2</sub>.

The configuration illustrated in (B) of Figure 4 differs from the configuration illustrated in (A) in that it further comprises a separation layer Sep<sub>d</sub> that is formed on the same side of the interface plane Int as the layer Sep<sub>c</sub>, and may be formed from silicon nitride, silicon carbonitride, silicon oxide or other dielectrics.

The separation layers of the variants illustrated in Figure 4 are multiple dielectric layers (MDLs) and may be used to improve the molecular bonding and adhesion strength in view of subsequent fabrication steps.

The fabrication process illustrated in Figures 1 and 2 allows a superposition of two superlattices to be obtained. In addition, the process may be repeated to stack an arbitrary number of superlattices. Thus, the critical epitaxy thickness  
5 may be exceeded: each of the superlattices considered individually may respect this thickness so as to be formed from high-quality layers, and stacking them allows an assembly of superlattices exceeding the critical thickness to be obtained while maintaining the quality of their constituent  
10 layers.

Forming the constituent layers of the superlattices by epitaxy requires the crystal structure to be reproduced from one layer to the next, and hence the Si layers and SiGe layers formed sequentially one after another by epitaxy have the same  
15 crystal structure. Usually it is not possible to grow a semiconductor layer having characteristics that are acceptable for forming transistors epitaxially on an amorphous layer such as a dielectric layer, and more particularly an oxide layer. Specifically, such a layer is unsuitable for epitaxy of a  
20 crystalline semiconductor layer of good quality. The separation layer obtained by the process according to the invention makes it possible to place a dielectric layer between two superlattices formed from semiconductor layers of sufficient quality to produce transistors for commercial  
25 applications.

Furthermore, the separation layer may be tailored (composition, thickness of the layer or layers forming it) to the intended use of the stacked superlattices. It is thus possible to achieve a desirable electrical insulation between  
30 the two superlattices Stck1 and Stck2 by modulating, for example, the thickness of the layer Cap2 which, once oxidised into the layer Ox2, forms a high-quality dielectric layer having a chosen thickness and covering the entirety of the structure, a whole wafer when the substrates are wafers.

The separation layer is continuously formed in a plane parallel to the upper surface of the substrate bearing it, covering substantially the entire surface of the substrate. Such a geometry contrasts with the situation found in CFET structures, in which the dielectric layer separating the n-type transistors and p-type transistors follows the reliefs formed by the structures resulting from formation of the transistors between the substrate and this dielectric layer, and may be discontinuous.

Thus, the separation layer according to the invention may be of high quality, of chosen thickness, further have a thickness of good uniformity, and be continuous over a segment of interest or over substantially the entire surface of a substrate, which makes it suitable for use as an etch-stop layer, during the process for fabricating the various transistors, or as an enabler of differential treatment of the transistors formed in the first superlattice and the transistors formed in the second superlattice. Moreover, if an SOI substrate is used as the substrate Car, it is also possible to produce a backside power delivery network (BSPDN) using the BOX as an etch-stop layer. A segment of interest may consist of a surface of a substrate expected to require the presence of the separation layer.

The carrier substrate Car and the donor substrate Don may comprise any semiconductor. Apart from silicon, the semiconductor may be germanium (GE), a silicon-germanium alloy (SiGe), silicon carbide (SiC), silicon-germanium carbide (SiGeC), III-V compound semiconductors or II-VI compound semiconductors, or SOI substrates (SOI standing for silicon-on-insulator), and more generally any type of semiconductor substrate comprising a layer of buried or surface dielectric. Such a dielectric layer may be used as an etch-stop layer when forming structures on the back side (same side as the carrier substrate Car) of the structure obtained by the process

illustrated in Figures 1 and 2, or, in the case where it is located on the surface, as insulation in order to prevent latch-up of an integrated circuit fabricated based on this structure.

5       The layers Ch1 and Ch2 may be formed, for example, from silicon or from a III-V compound semiconductor. The layers Sac1 and Sac2 may be formed, for example, from silicon-germanium alloys (generically designated SiGe). The layers Ch1 and Ch2 may have the same composition in both superlattices  
10 Stck1 and Stck2, and likewise, the layers Sac1 and Sac2 may have the same composition  $\text{Si}_{1-x}\text{Ge}_x$  in both superlattices Stck1 and Stck2. This last point makes it possible to remove the sacrificial layers Sac1 and Sac2 in the same step.

      Alternatively, the superlattices Stck1 and Stck2 may have  
15 different natures and/or orientations. The orientation of the second superlattice relative to the first superlattice is defined in the joining step. The layers Sac1 (and Ch1) on the one hand and the layers Sac2 (and Ch2) on the other hand may have different orientations, for example having  
20 crystallographic axes offset by  $45^\circ$ . It is also possible to consider using strained silicon, silicon-germanium alloys (SiGe) or germanium for the channel layers of either or both of the superlattices. When the two superlattices comprise silicon-germanium alloys, the proportions of germanium in the  
25 alloy may be the same or different in the two superlattices. Of course, the nature and characteristics of the sacrificial layers Sac1 and Sac2 must be tailored to those of the layers Ch1 and Ch2. Thus, it is necessary to tailor the nature and crystal structure of the seed layer Init to the  
30 characteristics of the layers Sac2 and Ch2 in order to guarantee adequate epitaxial growth of these layers.

      Likewise, the numbers of channel layers and sacrificial layers in the two superlattices may be the same, respectively, or may be different.

The above embodiment implemented, by way of example, associations between layers of silicon in alternation with layers of silicon-germanium alloys to form the first superlattice and second superlattice. However, the invention  
5 is not limited to this particular case, and could be applied for example (i) to superlattices made up of layers of germanium in alternation with layers of a silicon-germanium alloy, (ii) to superlattices made up of layers formed from a first silicon-germanium alloy having a germanium content for  
10 example lower than 20% in alternation with layers formed from a second silicon-germanium alloy having a high germanium content, for example higher than 75%, (iii) to superlattices having layers of different crystallographic orientations, or (iv) to superlattices comprising layers of III-V  
15 semiconductors.

The embodiment described above relates to an association of superlattices intended to form transistors, and more specifically nanosheet transistors or CFETs. However, the scope of the invention extends beyond this field and comprises  
20 combination of superlattices in general, not only in the field of semiconductors.

The invention is not limited to the embodiment described above, and variants may be employed without departing from the scope of the invention as defined by the claims.

## CLAIMS

1. Process (500) for fabricating a structure (Strc, Strc', Strc'') comprising a superlattice stack, comprising the steps of:

- forming (510<sub>Car</sub>) a first superlattice (Stck1) on a first substrate (Car), by stacking a plurality of first channel layers (Ch1) in alternation with a plurality of first sacrificial layers (Sac1);
- forming (520<sub>Don</sub>) a seed layer (Init) of a second superlattice (Stck2) by adding material to a second substrate (Don);
- forming (550<sub>Don</sub>) a weakening plane (Imp) in the second substrate (Don) by implanting ions of a light species into the second substrate (Don);
- forming an assembly (Ass) by joining (560) the seed layer (Init) to the first superlattice (Stck1) via a dielectric separation layer (Sep, Sep', Sep'') that separates the first superlattice (Stck1) from the seed layer (Init) and keeps them fastened to each other;
- removing (570A) a first part (Don<sub>b</sub>) of the second substrate (Don) by splitting the second substrate (Don) in the weakening plane (Imp), and removing this part (Don<sub>b</sub>) of the second substrate (Don), after the joining step (560);
- uncovering (570B) the seed layer (Init) after the step (570A) of splitting the second substrate (Don) in such a way that the uncovered seed layer forms an exterior side (F<sub>ext</sub>) of the assembly (Ass), the uncovering step including removing a second part (Don<sub>a</sub>) of the second substrate that remained joined to the seed layer (Init) after the step of removing the first part (Don<sub>b</sub>) of the second substrate (Don); and
- forming (580) the second superlattice (Stck2) on and in direct contact with the exterior side (F<sub>ext</sub>) of the uncovered seed layer (Init), by stacking a plurality of second channel layers

(Ch2) in alternation with a plurality of second sacrificial layers (Sac2).

2. Process according to Claim 1, wherein the weakening plane (Imp) of the second substrate (Don) is formed by implanting ions of a light species into the second substrate (Don) through the seed layer (Init).

3. Process according to Claim 1 or 2, wherein the separation layer (Sep, Sep', Sep'') is continuously formed in a plane parallel to a surface (S<sub>Car</sub>) of the first substrate (Car) on which the first superlattice (Stck1) is formed.

4. Process according to any of Claims 1 to 3, wherein:

- the first channel layers (Ch1) and second channel layers (Ch2) are each formed from a semiconductor material, and
- the first sacrificial layers (Sac1) and second sacrificial layers (Sac2) are each formed from a material that is capable of having a faster etch rate than the first channel layers (Ch1) and second channel layers (Ch2), respectively.

5. Process according to any of Claims 1 to 4 above, wherein:

- the first channel layers (Ch1) and second channel layers (Ch2) are each formed from silicon, and
- the first sacrificial layers (Sac1) and second sacrificial layers (Sac2) are each formed from a silicon-germanium alloy.

6. Process according to any of Claims 1 to 5, comprising the steps of:

- forming (520<sub>Car</sub>) a first cap layer (Cap1, Ox1) covering the first superlattice (Stck1) before the fastening step (560); and
- forming (530<sub>Don</sub>) a second cap layer (Cap2, Ox2) covering the seed layer (Init) before the fastening step (560);

wherein the fastening step (560) comprises placing the first cap layer (Cap1, Ox1) in contact with the second cap layer (Cap2, Ox2), the first cap layer (Cap1, Ox1) and second cap layer (Cap2, Ox2) together forming the separation layer (Sep, Sep', Sep'').

7. Process according to Claim 6, wherein the first cap layer (Ox2) and second cap layer (Cap2) each comprise silicon and at least one of the first cap layer (Ox1) and second cap layer (Ox2) is formed from an oxide.

8. Process according to Claim 7, wherein at least one of the first cap layer and second cap layer formed from an oxide is formed via a step of forming (530<sub>Don</sub>) a silicon layer (Cap2) followed by a step of oxidising (540<sub>Don</sub>) this silicon layer.

9. Process according to any of Claims 1 to 8, further comprising a step of forming (510<sub>Don</sub>) at least one etch-stop layer (Stp, Cap2') on the second substrate (Don) prior to forming the seed layer (Init), the etch-stop layer being removed in the step (570B) of uncovering the seed layer (Init).

10. Process according to Claim 9, wherein the at least one etch-stop layer is formed from a layer (Stp) of the same material as the second sacrificial layers (Sac2) and from a layer (Cap2') of the same material as the second channel layers (Ch2), the layer (Stp) of the same material as the second sacrificial layers (Sac2) and the layer (Cap2') of the same material as the second channel layers (Ch2) being removed in the step (570B) of uncovering the seed layer (Init).