Abstract

METHOD FOR FORMING A RAISED SOURCE AND DRAIN WITHOUT USING SELECTIVE EPITAIAL GROWTH

A method for forming a raised source and drain structure without using selective epitaxial silicon growth. A semiconductor substrate is provided having one or more gate areas covered by dielectric structures. Doped polysilicon structures are adjacent to the dielectric structures on each side and are co-planar with the dielectric structures from a CMP process. The first dielectric structures are removed to form gate openings and a liner oxide layer is formed on the bottom and sidewalls of the gate openings. Dielectric spacers are formed on the liner oxide layer over the sidewalls of the gate openings, and the liner oxide layer is removed from the bottom of the gate openings and from over the doped polysilicon structures. Source and drain regions are formed in the semiconductor substrate by diffusing impurity ions from the doped polysilicon layer. A gate oxide layer and a gate polysilicon layer are formed over the semiconductor structure and the gate polysilicon layer is planarized to form a gate electrode. In a key step, the dielectric spacers are removed to form spacer openings, and impurity ions are implanted through the spacer openings and annealed to form source and drain extensions. The dielectric spacers are reformed and a self-aligned silicide layer is formed on the doped polysilicon structure and the gate electrode. Alternatively, the self-aligned silicide layer can be formed prior to removing the dielectric spacers and implanting ions to form source and drain extensions.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)