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(54) Title: LATCH FOR BINARY BIT PAIR

	Input z_i		Output Z_i					
	x_i	y_i	Present $t=0$		Next $t=1$		Next $t=2$	
			X_i	Y_i	X_i	Y_i	X_i	Y_i
	(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)
1	0	0	0	0	0	0	0	0
2			0	1	0	1	0	1
3			1	0	1	0	1	0
4			1	1	0	0	0	0
5	0	1	0	0	0	1	0	1
6			0	1	0	1		
7			1	0	0	0		
8			1	1	0	0		
9	1	0	0	0	1	0	1	0
10			1	0	1	0		
11			0	1	0	0		
12			1	1	0	0		
13	1	1	0	0	0	0	0	0
14			0	1	0	0		
15			1	0	0	0		
16			1	1	0	0		

Figure 4a

(57) Abstract: A latch circuit for receiving a pair of bits, comprising: a first-latch input for one of the bit in the pair and a first-latch output, a second-latch input for the other one of the bit in the pair and a second-latch output (1) the first-latch input being one of two of a first-upstream gate, the first-latch output being the output of a first-downstream gate; the output of the first-upstream gate connected to one of two input of the first-downstream gate; the first-latch output connected to the other one of two of the first-upstream gate as a feedback; (2) the second-latch input being one of two of a second-upstream gate, the second-latch output being the output of a second-downstream gate; the output of the second-upstream gate connected to one of two input of the second-downstream gate; the second-latch output connected to the other one of two of the second-upstream gate as a feedback; (3) a midstream gate having two input each connected to one of the output of the first-upstream gate and the output of the second-upstream gate; the output of the midstream gate connected the other of the two input of the second-downstream gate and the other of the two input of the first-downstream gate.

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