CLAIMS

1. A method for improving lifetime and coherence time of a qubit in a quantum mechanical device, comprising:

providing a substrate having a frontside and a backside, the frontside having at least one qubit formed thereon, the at least one qubit comprising a first capacitor pad and a second capacitor pad having a gap reserved therebetween; and

removing an amount of substrate material from the backside of the substrate at least at an area below said gap to reduce radiofrequency electrical current loss due to at least one of silicon-air (SA) interface, metal-air (MA) interface or silicon-metal (SM) interface so as to enhance a lifetime (T1) and a coherence time (T2) in the at least one qubit.

2. The method according to claim 1, wherein reducing radiofrequency electrical current loss comprises reducing the radiofrequency electrical current loss by increasing radiofrequency overlap with lower loss geometric features in the quantum mechanical device and decreasing radiofrequency overlap with higher loss geometric features in the quantum mechanical device.

3. The method according to claim 1, wherein removing the amount of the substrate material from the backside of the substrate at least at the area below said gap comprises chemically etching the backside of the substrate selectively using a chemical etchant selected depending on the substrate material.

4. The method according to claim 3, wherein prior to chemically etching the backside of the substrate, forming an initial cavity in the backside of the substrate in a vicinity of the at least one qubit by mechanically removing material from the backside of the substrate and then chemically etching the backside of the substrate at the formed initial cavity with the chemical etchant.

5. The method according to claim 4, wherein forming the initial cavity in the backside of the substrate comprises defining faces of the initial cavity having one or more first crystal

planes and one or more second crystal planes so that the chemical etchant preferentially etches the substrate material from said one or more first crystal planes while substantially not etching substrate material from said one or more second crystal planes to form an etched final cavity in the vicinity of the at least one qubit.

6. The method according to claim 1, wherein removing the amount of substrate material from the backside of the substrate comprises removing the amount of substrate material in an area of the backside of the substrate to form a trench below the gap between the first capacitor pad and the second capacitor pad of the at least one qubit.

7. The method according to claim 6, wherein removing the amount of substrate material in the area of the backside of the substrate to form the trench below the gap between the first capacitor pad and the second capacitor pad of the at least one qubit comprises removing the amount of substrate material so that the trench is substantially centered around the gap between the first capacitor pad and the second capacitor pad of the at least one qubit.

8. The method according to claim 7, wherein removing the amount of substrate material so that the trench is substantially centered around the gap between the first capacitor pad and the second capacitor pad of the at least one qubit comprises forming the trench to reduce a participation rate of surface states with RF energy density for silicon-metal (SM) interface and increasing a participation rate of surface states with the RF energy density for silicon-air (SA) interface.

9. The method according to claim 6, wherein a surface state RF energy density overlap in silicon-metal (SM) interface is reduced and the surface state RF energy density overlap for silicon-air (SA) interface is increased with increasing depth of the trench.

10. The method according to claim 1, wherein removing the amount of substrate material from the backside of the substrate comprises forming a trench below the gap between the first capacitor pad and the second capacitor pad of the at least one qubit; and further comprising depositing a superconducting metal layer within the trench at the backside of the substrate.

11. The method according to claim 10, wherein forming the trench below the gap between the first capacitor pad and the second capacitor pad of the at least one qubit comprises forming the trench below and centered around one of the first capacitor pad and the second capacitor pad of the at least one qubit.

12. The method according to claim 10, wherein the radiofrequency electrical current loss due to metal-air (MA) interface is decreased based on a backside width of the trench.

13. The method according to claim 1, wherein removing the amount of the substrate material from the backside of the substrate comprises applying an etch mask film to the backside of the substrate and etching a selected area at the backside of the substrate opposite the at least one qubit.

14. The method according to claim 13, further comprising: subsequent to applying the etch mask film to the backside of the substrate and prior to etching the selected area at the backside of the substrate, forming one or more openings in the etch mask film at the selected area.

15. The method according to claim 13, wherein etching the selected area at the backside of the substrate opposite the at least one qubit comprises chemically etching a desired thickness of the substrate to form a trench at the selected area.

16. The method according to claim 15, further comprising depositing a superconducting metal layer within the trench.

17. The method according to claim 1, wherein removing the amount of the substrate material from the backside of the substrate at the area opposite the at least one qubit comprises applying a mask film to the backside of the substrate and depositing a metal superconductor layer on masked areas of the backside of the substrate.

18. A quantum mechanical device, comprising:

a substrate having a frontside and a backside; and

a plurality of qubits formed on the frontside of the substrate, the plurality of qubits comprising a first capacitor pad and a second capacitor pad having a gap reserved therebetween,

wherein the substrate comprises at least one trench formed on the backside of the substrate opposite at least one qubit of the plurality of qubits, at least at an area below said gap, and

wherein at least one of a size, a shape, or a position of the at least one trench are selected to reduce radiofrequency electrical current loss due to at least one of silicon-air (SA) interface, metal-air (MA) interface or silicon-metal (SM) interface, or any combination thereof, so as to enhance a lifetime (T1) and a coherence time (T2) in the at least one qubit.

19. The quantum mechanical device according to claim 18, wherein the substrate is selected from the group consisting of silicon, and sapphire.

20. The quantum mechanical device according to claim 19, wherein the first capacitor pad and the second capacitor pad are made from a superconducting material.

21. The quantum mechanical device according to claim 20, wherein the superconducting material is selected from the group consisting of aluminum (Al) and niobium (Nb).

22. The quantum mechanical device according to claim 18, wherein the at least one trench is provided below the gap between the first capacitor pad and the second capacitor pad.

23. The quantum mechanical device according to claim 22, wherein the at least one trench is substantially centered around the gap so as to reduce surface state energy density for silicon-metal (SM) interface and to increase surface state energy density for silicon-air (SA) interface.

24. The quantum mechanical device according to claim 18, further comprising a superconducting metal layer provided within the at least one trench so as to reduce the radiofrequency electrical current loss due to metal-air (MA) interface.

25. The quantum mechanical device according to claim 24, wherein the at least one trench is formed below and centered around the first capacitor pad or the second capacitor pad.