

Figure 1A

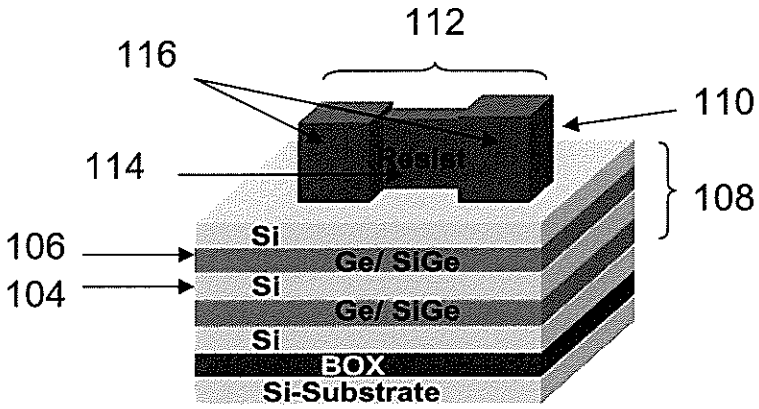


Figure 1B

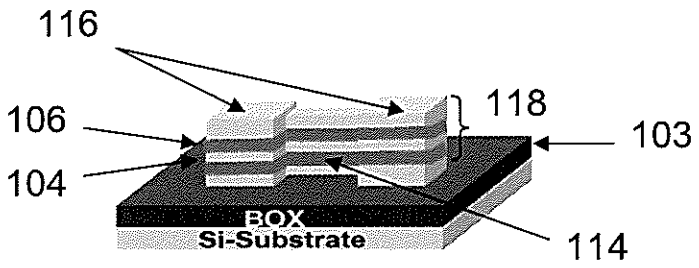


Figure 1C

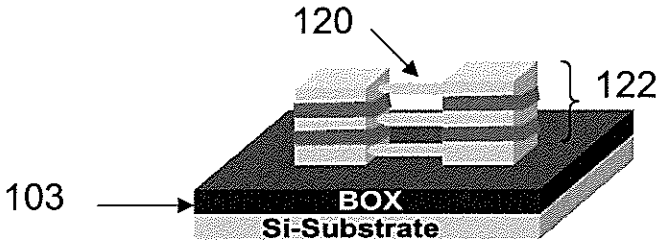


Figure 1D

200

Figure 2

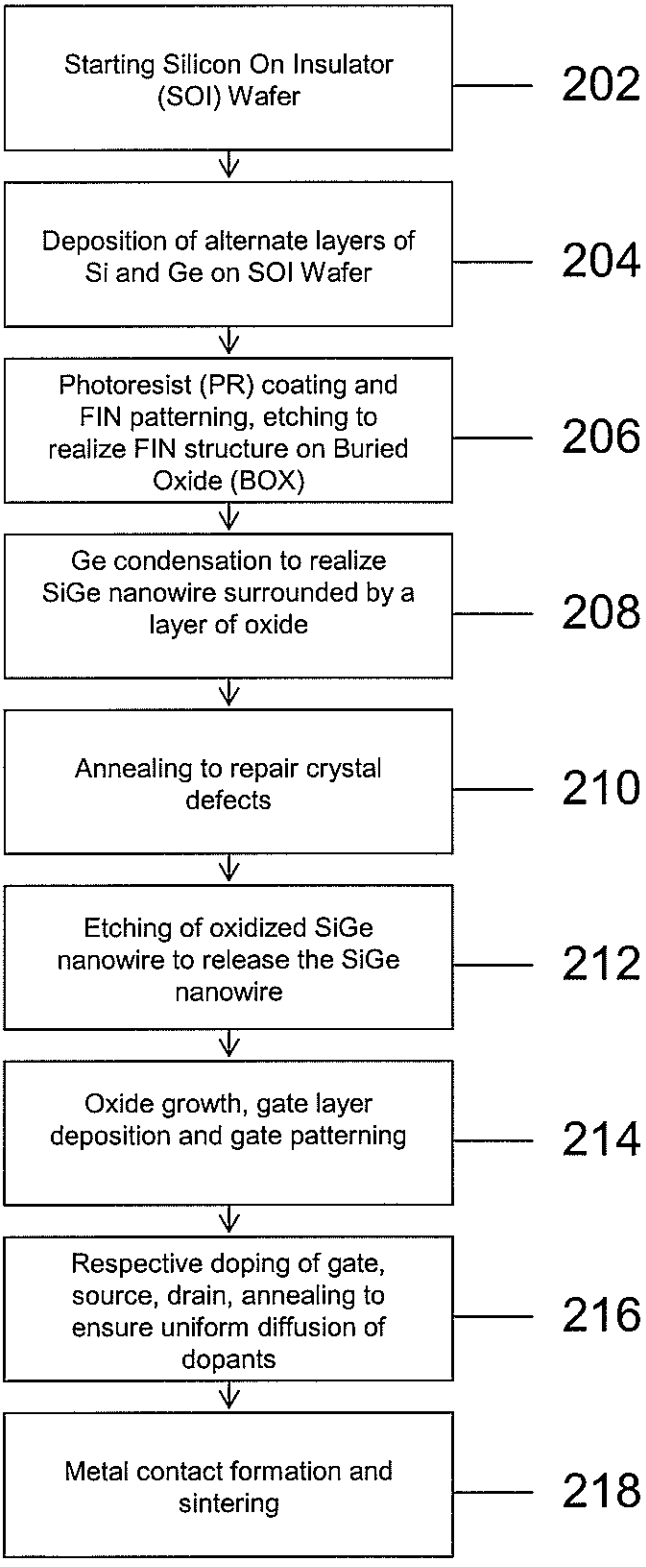

Starting Silicon On Insulator (SOI) Wafer
202
Deposition of alternate layers of Si and Ge on SOI Wafer
204
Photoresist (PR) coating and FIN patterning, etching to realize FIN structure on Buried Oxide (BOX)
206
Ge condensation to realize SiGe nanowire surrounded by a layer of oxide
208
Annealing to repair crystal defects
210
Etching of oxidized SiGe nanowire to release the SiGe nanowire
212
Oxide growth, gate layer deposition and gate patterning
214
Respective doping of gate, source, drain, annealing to ensure uniform diffusion of dopants
216
Metal contact formation and sintering
218

Figure 3

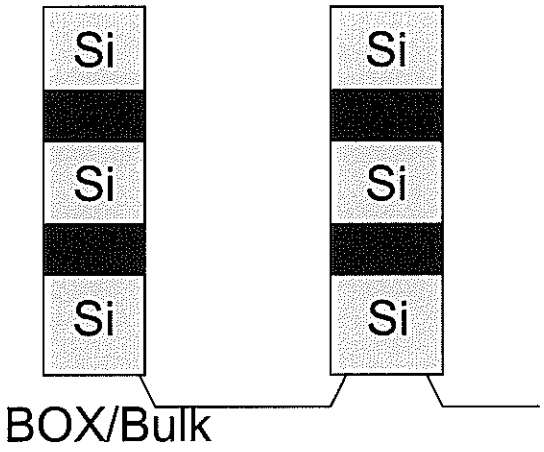


Figure 4

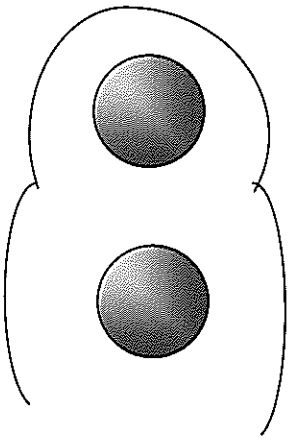


Figure 5

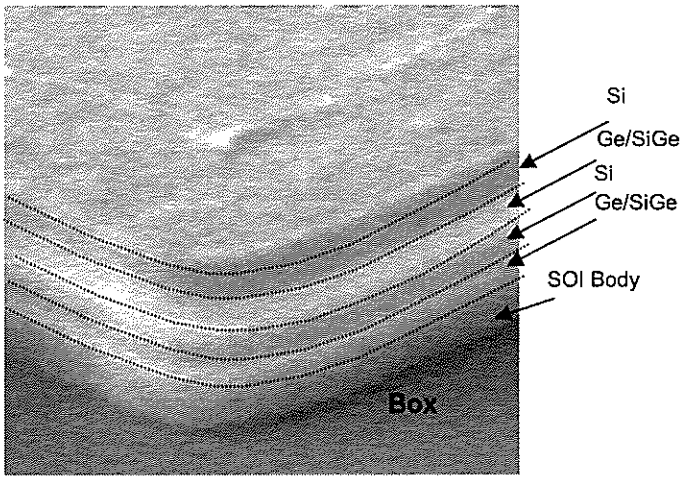


Figure 6A

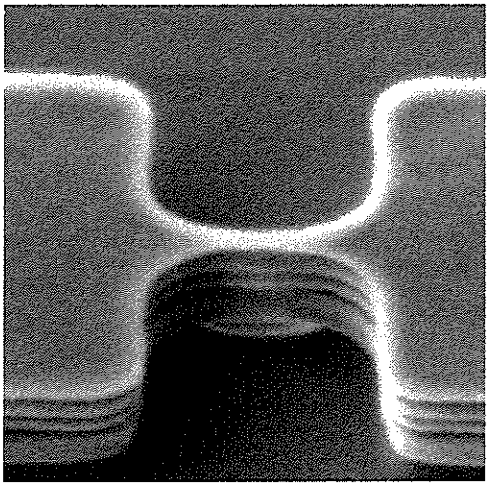


Figure 6B

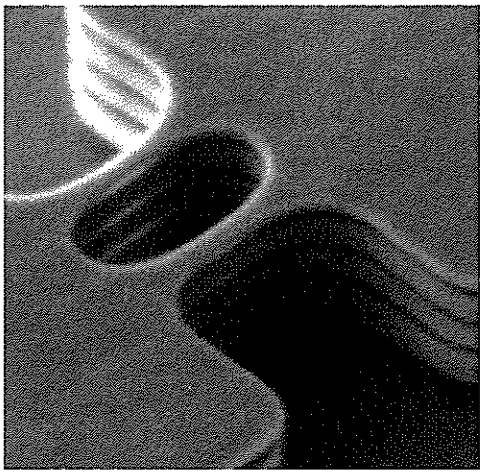


Figure 7A

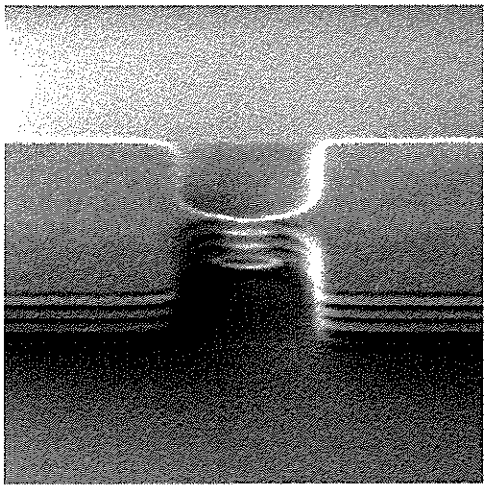
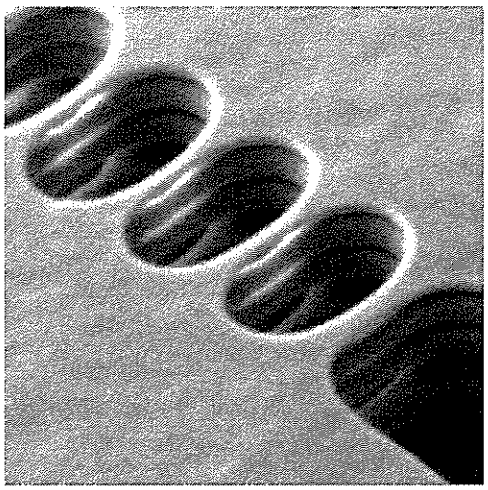


Figure 7B



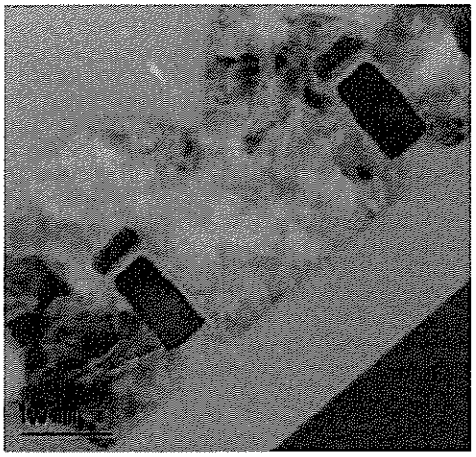


Figure 8A



Figure 8B

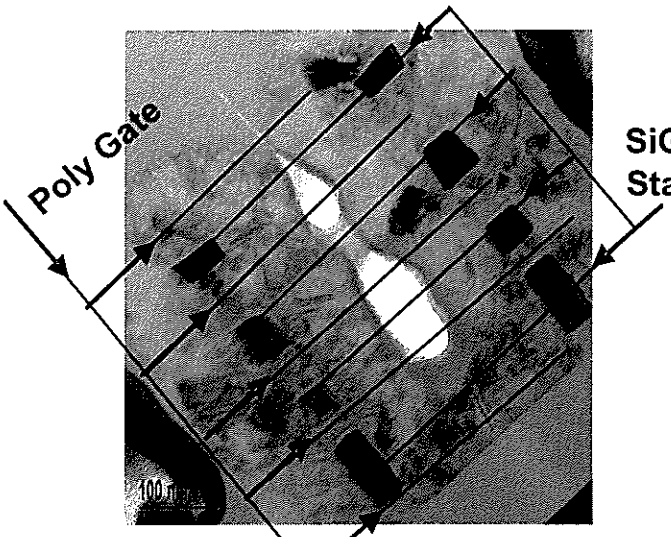


Figure 8C

Figure 9

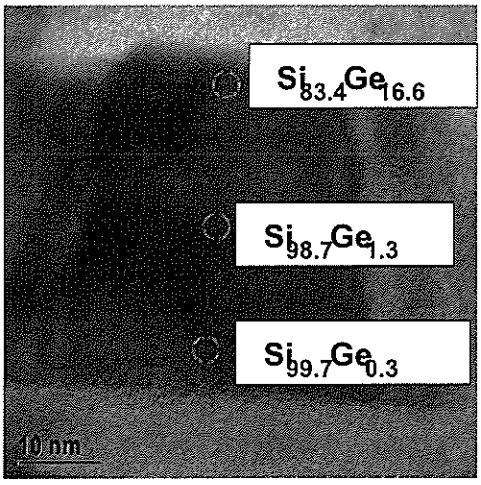


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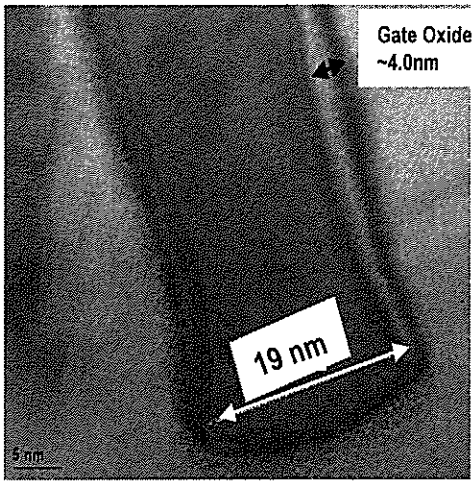


Figure 11

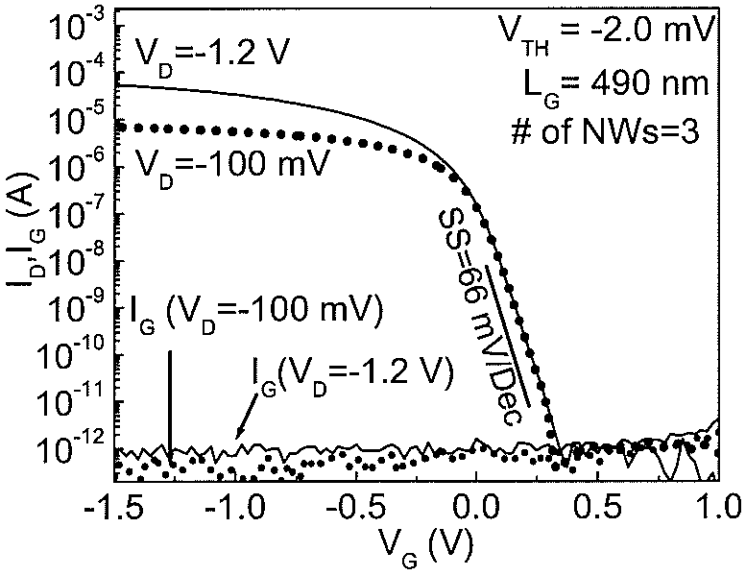


Figure 12

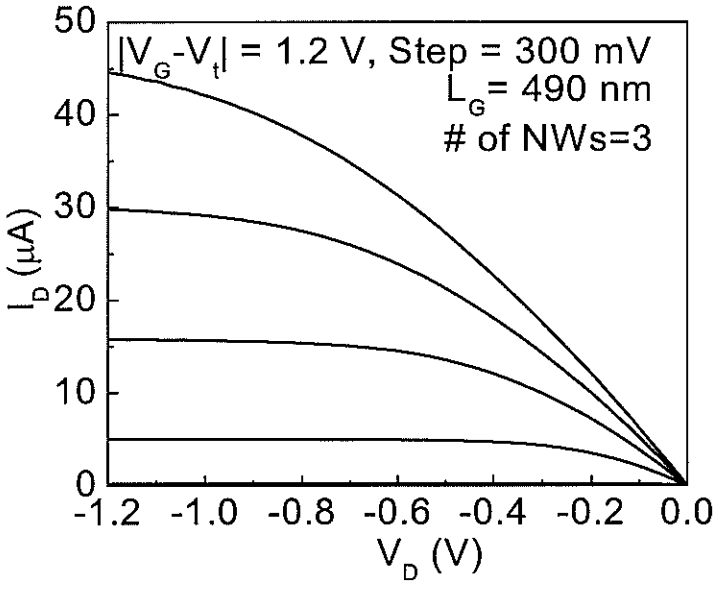


Figure 13

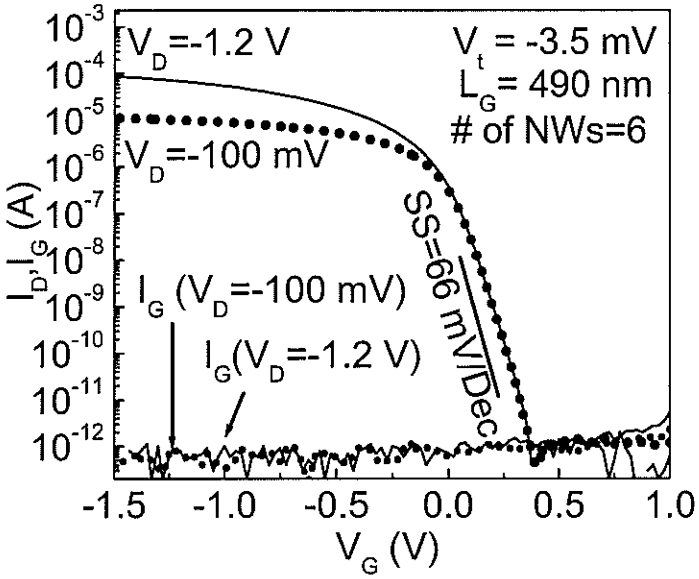


Figure 14

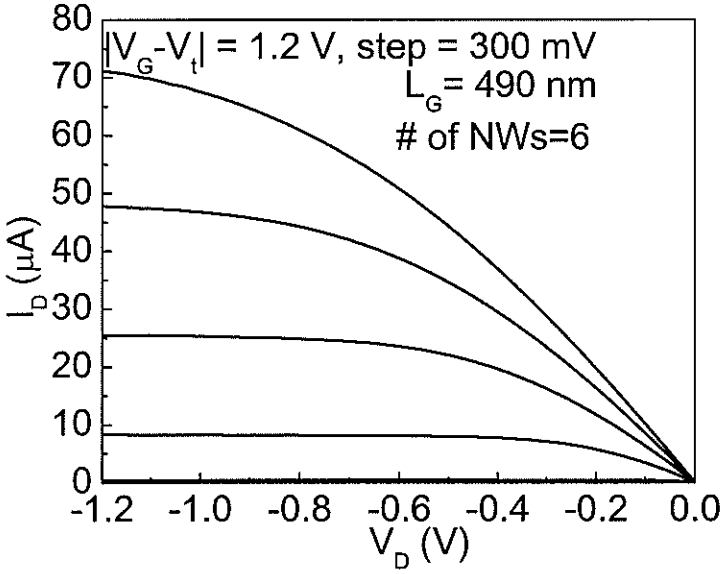


Figure 15

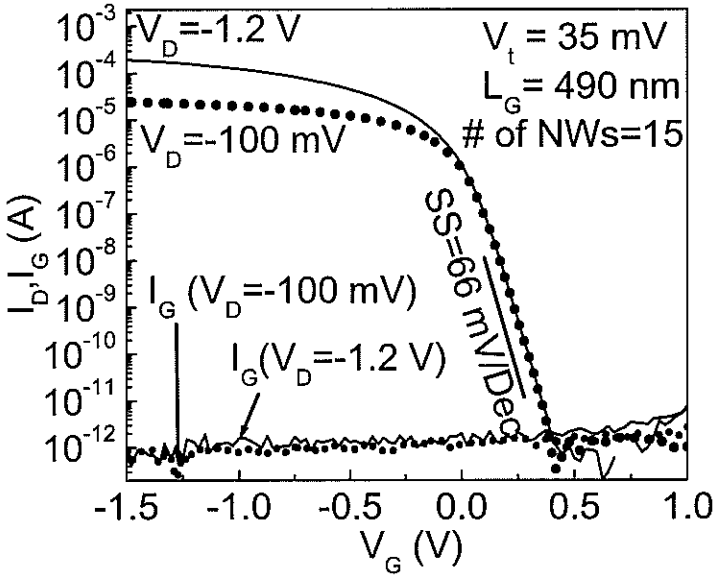


Figure 16

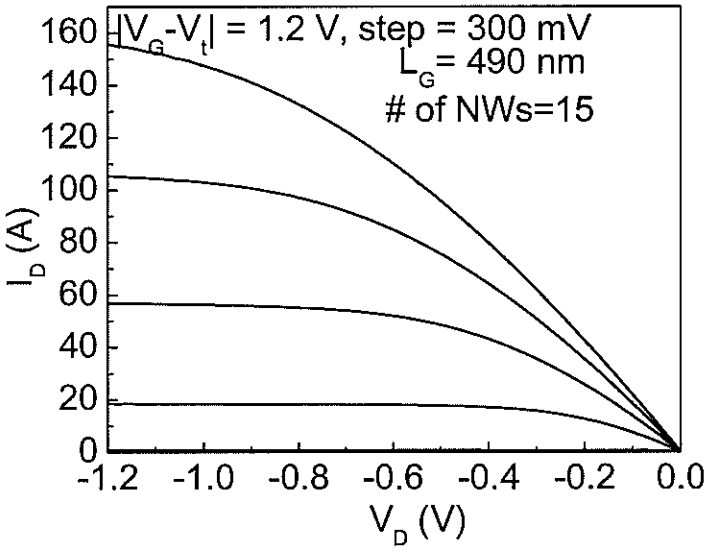


Figure 17

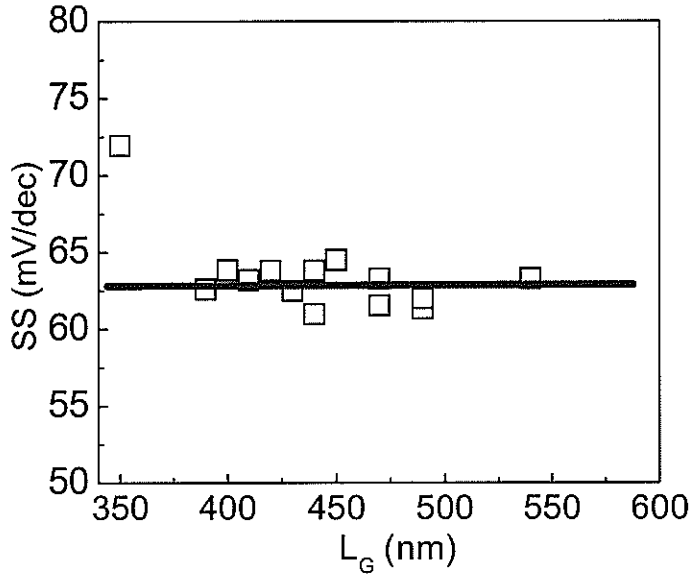


Figure 18

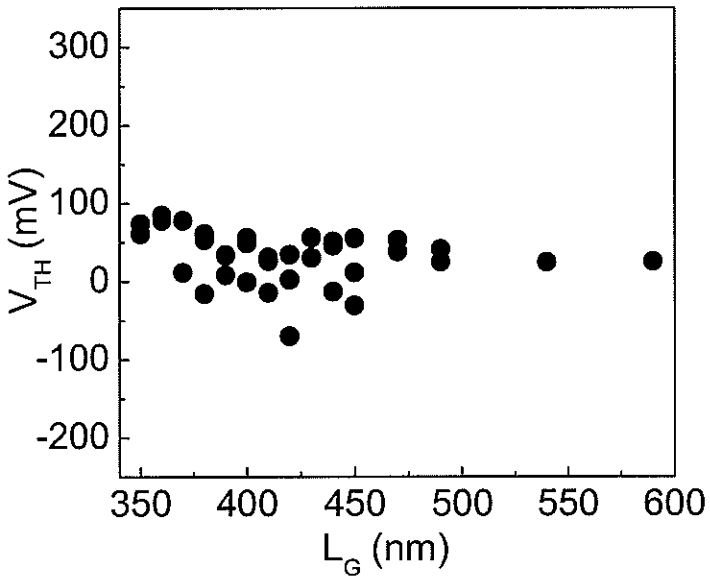


Figure 19

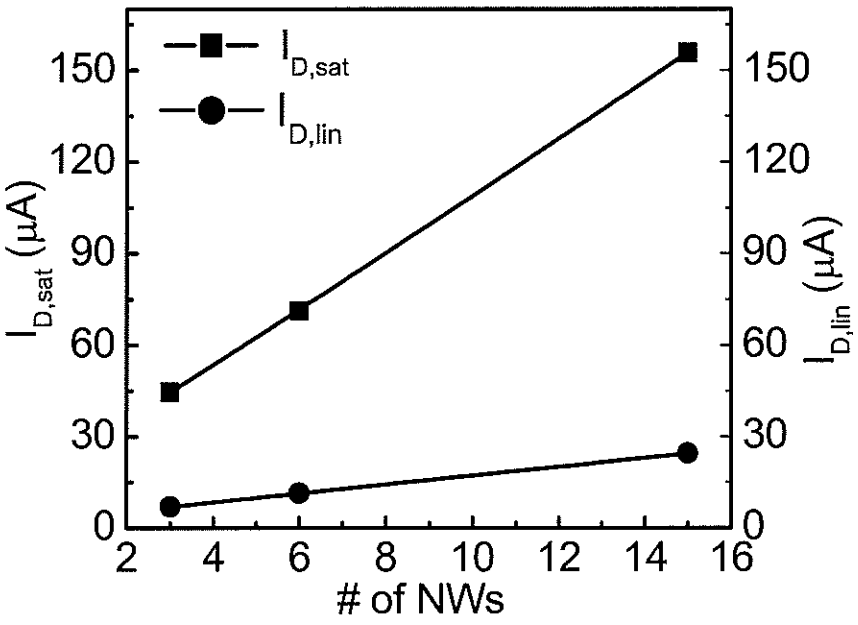


Figure 20

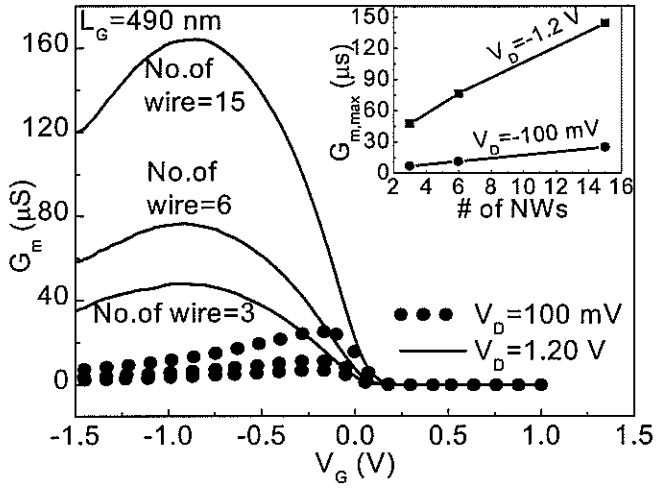
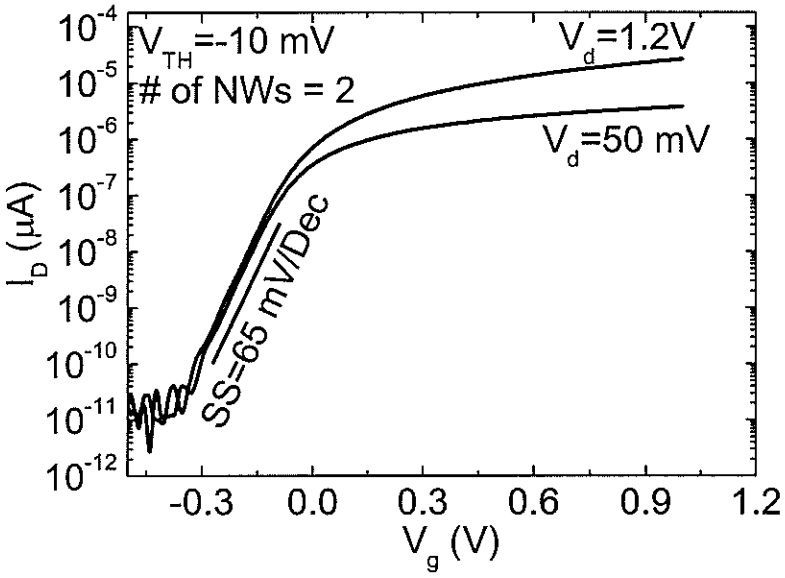


Figure 21


10^{-4}
10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
10^{-12}
I_D (μA)
V_{TH}=-10 mV
# of NWs = 2
V_d=1.2V
V_d=50 mV
SS=65 mV/Dec
-0.3
0.0
0.3
0.6
0.9
1.2
V_g (V)