IMPROVED METHOD FOR PLANARIZED INTERCONNECT VIAS USING ELECTROLESS PLATING AND CMP

ABSTRACT

An improved and new method for fabricating conducting vias between successive layers of conductive interconnection patterns in a semiconductor integrated circuit has been developed. The method utilizes a first CMP step to form a barrier lined contact hole, deposition of copper by electroless plating into the barrier lined contact hole, and a second CMP step to remove overgrowth of copper, thus producing coplanarity between the copper surface and the surrounding insulator surface.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)