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SPECIFICATION

TITLE OF THE INVENTION

A semiconductor device and a process for producing the same

FIELD OF THE INVENTION

The present invention relates to a semiconductor producing technique and, more particularly, a technique effective at improving the reliability of a fan-in and fan-out CSP (Chip Size Package or Chip Scale Package).

BACKGROUND OF THE INVENTION

The techniques described hereinbelow were examined by the inventor through his study to accomplish the present invention. The outline of the techniques is as follows.

As an example of a semiconductor device to be made thinner and smaller, a CSP as a semiconductor device equivalent or slightly larger than the chip size is known. The CSP is often mounted on a printed wiring board to be assembled in a portable electronic device or the like.

A general structure of a CSP will be described. A CSP comprises: a tape substrate on which bump electrodes as external terminals are mounted and is provided with leads which are electrically connected to connection terminals (electrode pads) of a semiconductor chip; an elastomer (elastic material) which

is disposed between the semiconductor chip and the tape substrate and reduces a stress which occurs at the time of mounting bumps; and a sealing portion for sealing the connection terminals of the semiconductor chip and the leads of the tape substrate electrically connected to the connection terminals by using a sealing resin.

Recently, in order to deal with increase in the number of pins and chip shrinkage (reduction in size of a semiconductor chip) performed to reduce the cost, a CPS having a structure such that bump electrodes as external terminals are disposed on the outside of a semiconductor chip has been proposed. The CSP of such a structure is called a fan-in and fan-out CSP.

Various fan-in and fan-out CSPs are disclosed in, for example, publications of Japanese Unexamined Patent Application (JP-A) Nos. 9-223759, 10-79402, 10-340968, 6-504408 (U.S.P 5,148,265 and 5,148,266), 9-260535 (U.S.Serial No. 08/822,933), and 11-87414(U.S.Serial No. 09/113,500).

First, a CSP disclosed in JP-A-9-223759 has a structure such that a polyimide film is formed on a semiconductor chip and a supporting frame on the outside of the chip, and a plurality of solder bumps are formed on the polyimide film.

A CSP disclosed in JP-A-10-79402 has a structure such that an outline ring made of copper is provided around a chip, the outline ring and the chip are connected to each other via a lead pattern, and a plurality of external connection terminals are

formed on the lead pattern and the chip.

Further, a CSP disclosed in JP-A-10-340968 has a structure such that a buffer layer having a three-dimensional mesh structure is provided on a chip and a chip supporting substrate which extends around the chip, and a plurality of solder bumps are formed on the buffer layer.

A CSP disclosed in JP-A-6-504408 has a structure using an elastomer layer.

A CSP disclosed in JP-A-9-260535 has a structure such that a plurality of solder bumps are formed via an elastomer over a semiconductor chip and a support ring around the chip.

A CSP disclosed in JP-A-11-87414 has a structure such that a tape substrate which extends on and around a semiconductor chip is provided, the semiconductor chip is attached to the tape substrate via a porous elastomer, and bumps as external terminals are provided over the tape substrate.

SUMMARY OF THE INVENTION

In each of the CSPs in the above-described techniques, that is, fan-in and fan-out CSPs, the support for bumps (external terminals) disposed on the outside of a semiconductor chip is weak structurally, so that insufficient support for bumps is an issue. In each of the fan-in and fan-out CSPs disclosed in the six publications, the support for the bumps disposed on the outside of the semiconductor chip is not sufficiently described or its

fabricating method is complicated.

Further, also in the case of using a porous elastomer to improve the reflowing resistance, since the strength of the porous elastomer is low, there is a problem such that it is difficult to assemble the CSP having the structure in which bumps are disposed on the outside of the chip.

An object of the invention is to provide a fan-in and fan-out semiconductor device which has high reflowing resistance and in which bump electrodes disposed on the outside of the chip are supported with reliability and a method of fabricating the device.

Another object of the invention is to provide a fan-in and fan-out semiconductor device which can be easily produced and a method of fabricating the device.

The above and other objects and novel features will become apparent from the following description of the specification and attached drawings.

In the invention disclosed in the application, the outline of representative techniques will be described briefly.

A semiconductor device of the invention comprises: a plurality of bump electrodes as external terminals disposed over a principal surface of a semiconductor chip and on the outside of the principal surface of the chip; a porous elastic member which is disposed on the principal surface of the semiconductor chip and in which an opening from which a connection terminal of the semiconductor chip is exposed is formed; a tape substrate which

is provided with a lead extending from the principal surface of the semiconductor chip to the outside of the chip, whose one end is electrically connected to the connection terminal and whose other end is electrically connected to the bump electrode, and in which an opening for exposing the connection terminal is formed; a reinforcing member for reinforcing support for the bump electrodes disposed on the outside of the semiconductor chip; and a sealing portion for sealing the connection terminal of the semiconductor chip and the lead of the tape substrate.

By providing the reinforcing member disposed on the outside of the semiconductor chip, the support for the bump electrodes on the outside of the chip is reinforced by the reinforcing member. Consequently, the plurality of bump electrodes on the outside of the chip can be supported with reliability. Further, since the porous elastic member is disposed on the principal surface of the semiconductor chip, no void is formed in the elastic member in reflowing for mounting a semiconductor device. Thus, a semiconductor device having excellent reflowing resistance can be realized.

As a result, the reliability of the semiconductor device can be improved.

According to the invention, there is provided another semiconductor device comprising: an elastic member having an elastic member body disposed on the principal surface of a semiconductor chip and an elastic member reinforcing part which

extends on the outside of the principal surface of the semiconductor chip, and having an opening from which a connection terminal formed on the principal surface of the semiconductor chip is exposed; a tape substrate which is provided with a lead extending from the principal surface of the semiconductor chip to the outside of the chip, whose one end is electrically connected to the connection terminal and whose other terminal is electrically connected to a bump electrode as an external terminal, which includes a tape base material, and has an opening from which the connection terminal is exposed; a sealing portion for sealing the connection terminal of the semiconductor chip and the lead connected to the connection terminal; and bump electrodes as the external terminals disposed over the principal surface of the semiconductor chip and on the outside of the semiconductor chip, wherein the bump electrode disposed on the outside of the semiconductor chip is supported and reinforced by the tape substrate and the elastic member reinforcing part of the elastic member.

Further, according to the invention, there is provided a semiconductor device comprising: a plurality of bump electrodes disposed over a principal surface of a semiconductor chip and on the outside of the principal surface of the chip; an elastic member which has an elastic member body part disposed on the principal surface of the semiconductor chip and an elastic member reinforcing part extending on the outside of the principal surface

of the semiconductor chip, and in which an opening for exposing a connection terminal of the semiconductor chip is formed; a tape substrate which is provided with a lead extending from the principal surface of the semiconductor chip to the outside of the chip, whose one end is electrically connected to the connection terminal and whose other end is electrically connected to the bump electrode, and in which an opening for exposing the connection terminal is formed; and a sealing portion for sealing the connection terminal of the semiconductor chip and the lead of the tape substrate, wherein the elastic member is formed in thickness equal to or thicker than that of the tape substrate, and support by the tape substrate for the bump electrodes disposed on the outside of the semiconductor chip is reinforced by the thick elastic member reinforcing part.

Further, according to the invention, there is provided a semiconductor device comprising: a porous elastic member which extends on the outside of a principal surface of a semiconductor chip, and has an opening from which a connection terminal formed on the principal surface of the semiconductor chip is exposed; a tape substrate which is provided with a lead extending from the principal surface of the semiconductor chip to the outside of the chip, whose one end is electrically connected to the connection terminal and whose other end is electrically connected to a bump electrode as an external terminal, and which has an opening for exposing the connection terminal; a sealing portion for sealing

the connection terminal of the semiconductor chip and the lead of the tape substrate; and a plurality of bump electrodes as external terminals disposed over the principal surface of the semiconductor chip and on the outside of the semiconductor chip, wherein the tape base material in the tape substrate is formed thicker than the core layer of the porous elastic member, and the support by the tape substrate for the bump electrodes disposed on the outside of the semiconductor chip is reinforced by the thick tape base material.

According to the invention, there is provided a method of fabricating a semiconductor device in which bump electrodes as external terminals are disposed on a principal surface of a semiconductor chip and on the outside of the chip, comprising the steps of: preparing a tape substrate which is provided with a lead on one of its faces and in which an opening where a part of the lead is disposed is formed; preparing an elastic member which is formed in thickness equal to or thicker than the tape substrate and has both an elastic member body part in which an opening of substantially the same shape as that of the opening in the tape substrate is formed and an elastic member reinforcing part formed on the outside of the elastic member body part; adhering the tape substrate and the elastic member to each other while aligning the opening in the tape substrate and the opening in the elastic member: exposing the connection terminals of the semiconductor chip from the two openings, disposing the elastic member body part

on the principal surface of the semiconductor chip, allowing the elastic member reinforcing part to extend on the outside of the principal surface of the semiconductor chip, and adhering the principal surface of the semiconductor chip and the elastic member to each other; connecting the connection terminal of the semiconductor chip and the corresponding lead disposed in the opening in the tape substrate to each other; sealing the connection terminal of the semiconductor chip and the lead connected to the connection terminal with a resin, thereby forming a sealed portion; forming the bump electrode to be connected to the lead on one of the sides of the tape substrate; and dicing the tape substrate into pieces, wherein the support by the tape substrate for the bump electrodes disposed on the outside of the semiconductor chip can be reinforced by the thick elastic member reinforcing part.

Further, according to the invention, there is provided a method of fabricating a semiconductor device in which bump electrodes as external terminals are disposed on a principal surface of a semiconductor chip and on the outside of the chip, comprising the steps of preparing a tape substrate which is provided with a lead on one of its faces and has an opening in which a part of the lead is disposed; preparing a porous elastic member in which an opening of substantially the same shape as that of the opening in the tape substrate is formed; preparing a reinforcing member for reinforcing support by the tape substrate

for the bump electrodes disposed on the outside of the semiconductor chip; adhering the tape substrate and the elastic member to each other while aligning the opening in the tape substrate and the opening in the elastic member; adhering the tape substrate and the reinforcing member to each other; exposing the connection terminals of the semiconductor chip from the two openings, disposing the reinforcing member around the semiconductor chip, and adhering the principal surface of the semiconductor chip and the elastic member to each other; connecting the connection terminal of the semiconductor chip and the corresponding lead disposed in the opening in the tape substrate to each other; forming a sealing portion by sealing the connection terminal of the semiconductor chip and the lead connected to the connection terminal with a resin; forming the bump electrode to be connected to the lead on one side of the tape substrate; and dicing the tape substrate into pieces, wherein the support by the tape substrate for the bump electrodes disposed on the outside of the semiconductor chip can be reinforced by the reinforcing member.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a plan view showing an example of the structure of a semiconductor device (fan-in and fan-out CSP) according to a first embodiment of the invention, in which a sealing portion is not illustrated.

Fig. 2 is a cross section taken along line A-A of the semiconductor device shown in Fig. 1.

Fig. 3 is a process flow chart showing an example of a procedure of producing the semiconductor device shown in Fig. 1.

Figs. 4A to 4D are diagrams each showing the structure in each of steps in the process for producing the semiconductor device illustrated in Fig. 1; Fig. 4A is a perspective view showing a tape substrate, Fig. 4B is a perspective view showing a state in which an elastic member is attached, Fig. 4C is a perspective view showing a state in which a reinforcing member is attached, and Fig. 4D is a perspective view showing a state where a chip is bonded.

Figs. 5A to 5C are diagrams each showing the structure in each of steps in the process for producing the semiconductor device illustrated in Fig. 1; Fig. 5A is a perspective view showing a state where leads are bonded, Fig. 5B is a perspective view showing a sealed state, and Fig. 5C is a perspective view showing a bump electrodes mounting state.

Fig. 6 is a plan view showing an example of a mounting state of the semiconductor device illustrated in Fig. 1 on a card board (mounting board).

Fig. 7 is a cross section showing the mounting state of the semiconductor device on the card board (mounting board) shown in Fig. 6.

Fig. 8 is a plan view showing the structure of a modification

of the semiconductor device (fan-in and fan-out CSP) illustrated in Fig. 1, in which the sealing portion is not illustrated.

Fig. 9 is a cross section taken along line B-B of the semiconductor device shown in Fig. 8.

Fig. 10 is a plan view showing an example of the structure of a semiconductor device (fan-in and fan-out CSP) according to a second embodiment of the invention, in which a sealing portion is not illustrated.

Fig. 11 is a cross section taken along line C-C of the semiconductor device shown in Fig. 10.

Fig. 12 is a process flow chart showing an example of a procedure of producing the semiconductor device illustrated in Fig. 10.

Figs. 13A to 13C are diagrams each showing the structure in each of steps in the process for producing the semiconductor device illustrated in Fig. 10; Fig. 13A is a perspective view showing a tape substrate, Fig. 13B is a perspective view showing a state in which an elastic member is attached, and Fig. 13C is a perspective view showing a state where a chip is bonded.

Figs. 14A to 14C are diagrams each showing the structure in each of steps in the process for producing the semiconductor device illustrated in Fig. 10; Fig. 14A is a perspective view showing a state where leads are bonded, Fig. 14B is a perspective view showing a sealing state, and Fig. 14C is a perspective view showing a bump electrodes mounting state.

Fig. 15 is a plan view showing the structure of a modification of the semiconductor device (fan-in and fan-out CSP) illustrated in Fig. 10, in which the sealing portion is not shown.

Fig. 16 is a cross section taken along line D-D of the semiconductor device shown in Fig. 15.

Fig. 17 is a plan view showing an example of the structure of a semiconductor device (fan-in and fan-out CSP) according to a third embodiment of the invention, in which a sealing portion is not illustrated.

Fig. 18 is a cross section taken along line E-E of the semiconductor device shown in Fig. 17.

Fig. 19 is a plan view showing a structure of a modification of the semiconductor device (fan-in and fan-out CSP) illustrated in Fig. 17, in which the sealing portion is not shown.

Fig. 20 is a cross section take along line F-F of the semiconductor device shown in Fig. 19.

Fig. 21 is a plan view showing an example of the structure of a semiconductor device (fan-in and fan-out CSP) according to a fourth embodiment of the invention, in which the sealing portion is not illustrated.

Fig. 22 is a cross section taken along line G-G of the semiconductor device shown in Fig. 21.

Fig. 23 is a plan view showing the structure of a modification of the semiconductor device (fan-in and fan-out CSP) illustrated in Fig. 21, in which the sealing portion is not shown.

Fig. 24 is a cross section taken along line H-H of the semiconductor device shown in Fig. 23.

Fig. 25 is a plan view showing an example of the structure of a semiconductor device (fan-in and fan-out CSP) according to a fifth embodiment of the invention, in which a sealing portion is not illustrated.

Fig. 26 is a cross section taken along line I-I of the semiconductor device shown in Fig. 25.

Fig. 27 is a plan view showing the structure of a modification of the semiconductor device (fan-in and fan-out CSP) illustrated in Fig. 25, in which the sealing portion is not shown.

Fig. 28 is a cross section taken along line J-J of the semiconductor device shown in Fig. 27.

Fig. 29 is a plan view showing an example of the structure of a semiconductor device (fan-in and fan-out CSP) according to a sixth embodiment of the invention, in which the sealing portion is not illustrated.

Fig. 30 is a cross section taken along line K-K of the semiconductor device shown in Fig. 29.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiments of the invention will be described in detail hereinbelow with reference to the drawings. In all of the drawings, members having the same function are designated by the same reference numeral and the repetitive description will be

omitted.

First Embodiment

Fig. 1 is a plan view showing an example of the structure of a semiconductor device (fan-in and fan-out CSP) according to a first embodiment of the invention, in which a sealing portion is not illustrated. Fig. 2 is a cross section taken along line A-A of the semiconductor device shown in Fig. 1. Fig. 3 is a process flow chart showing an example of a procedure of producing the semiconductor device shown in Fig. 1. Figs. 4A to 4D are diagrams each showing the structure in each of steps in the process for producing the semiconductor device illustrated in Fig. 1; Fig. 4A is a perspective view showing a tape substrate, Fig. 4B is a perspective view showing a state in which an elastic member is attached, Fig. 4C is a perspective view showing a state in which a reinforcing member is attached, and Fig. 4D is a perspective view showing a state where a chip is bonded. Figs. 5A to 5C are diagrams each showing the structure in each of steps in the process for producing the semiconductor device illustrated in Fig. 1; Fig. 5A is a perspective view showing a state where leads are bonded, Fig. 5B is a perspective view showing a sealing state, and Fig. 5C is a perspective view showing a bump electrodes mounting state. Fig. 6 is a plan view showing an example of a mounting state of the semiconductor device illustrated in Fig. 1 on a card board (mounting board). Fig. 7 is a cross section showing the mounting

state of the semiconductor device on the card board (mounting board) shown in Fig. 6. Fig. 8 is a plan view showing the structure of a modification of the semiconductor device illustrated in Fig. 1, in which the sealing portion is not shown. Fig. 9 is a cross section taken along line B-B of the semiconductor device shown in Fig. 8.

A semiconductor device (CSP 11) shown in Figs. 1 and 2 is of a small size such that its package size is slightly larger than the chip size. The CSP 11 is of a fan-in and fan-out type in which a plurality of bump electrodes 2 as external terminals are disposed over the principal surface 1a of a semiconductor chip 1 and on the outside of the semiconductor chip 1.

Examples to which such a CSP 11 is applied are, although not limited, a rambus DRAM (Dynamic Random Access Memory), a direct rambus DRAM, and the like.

The structure of the CSP 11 will be described. The CSP 11 comprises: a porous elastomer 3 (elastic member) which is disposed on the principal surface 1a of the semiconductor chip 1 and in which an opening 3c for exposing electrode pads 1b (connection terminals) of the semiconductor chip 1 is formed; leads 4c which extend from the principal surface 1a of the semiconductor chip 1 to the outside of the chip and each of which has one end electrically connected to the electrode pad 1b and the other end electrically connected to the bump electrode 2; a tape substrate 4 in which an opening 4e for exposing the electrode pads 1b is

formed; a reinforcing member 6 for reinforcing the support for the bump electrodes 2 disposed on the outside of the semiconductor chip 1; and a sealing portion 5 for sealing the electrode pads 1b of the semiconductor chip 1 and the leads 4c of the tape substrate 4. The support by the tape substrate 4 for the bump electrodes 2 disposed on the outside of the semiconductor chip 1 is reinforced by the reinforcing member 6.

Specifically, in the fan-in and fan-out CSP 11, the support for the bump electrodes 2 mounted in the fan-out area (area outside of the chip) by the tape substrate 4 is reinforced by the reinforcing member 6, thereby improving the flatness of the tape substrate 4. As a result, the reliability in mounting of the CSP 11 is improved.

In the plan view of the CSP 11 of Fig. 1, in order to show the electrode pads 1b on the semiconductor chip 1 and the leads 4c on the tape substrate 4, the sealing portion 5 shown in Fig. 2 is not illustrated.

Although the sealing portion 5 is omitted in the plan view of the CSP 11 of Fig. 1, the sealing portion 5 as shown in Fig. 2 is formed in practice in the opening 4e of the tape substrate 4 of the CSP 11 shown in Fig. 1 (ditto for the second to fifth embodiments).

In the CSP 11 of the first embodiment, the electrode pads 1b on the semiconductor chip 1 are arranged almost in parallel to a pair of facing sides in the principal surface 1a of the

semiconductor chip 1, in the center portion between the pair of sides.

That is, the semiconductor chip 1 assembled in the CSP 11 has a center pad alignment.

Further, a plurality of bump electrodes 2 as external terminals of the CSP 11 are provided on both sides of the sealing portion 5 (12 pieces on each side, total 24 pieces) in a lattice array. Since the CSP 11 is of a fan-in and fan-out type, the bump electrodes 2 arranged over the principal surface 1a of the semiconductor chip 1 and the bump electrodes 2 disposed on the outside of the principal surface 1a of the semiconductor chip 1 are provided.

As shown in Fig. 2, the reinforcing member 6 in the CSP 11 of the first embodiment is fixed to the tape substrate 4 via an adhesive layer 8 in the area outside of the semiconductor chip 1. As shown in Fig. 1, the reinforcing member 6 is a continuous reinforcing frame. On the inside of the frame, therefore, as shown in Fig. 2, the semiconductor chip 1 and the elastomer 3 are arranged.

The reinforcing member 6 does not always have to be a continuous member. It is also possible to use two or more divided members and almost uniformly disperse and attach them to the tape substrate 4 on the outside of the chip, thereby reinforcing the support by the tape substrate 4 for the bump electrodes 2 disposed in the area outside of the chip.

The reinforcing member 6 is made of, for example, a polyimide resin and is thickly formed for reinforcement. When a tape base material 4g in the tape substrate 4 is made of a polyimide resin, it is preferable to set the total thickness of the reinforcing member 6 as a reinforcing frame made of a polyimide resin and the polyimide resin of the tape base material 4g in the tape substrate 4 to about 100 to 175 μm. By the arrangement, the support by the tape substrate 4 for the bump electrodes 2 disposed on the outside of the chip can be reinforced.

The reinforcing member 6 may be also made of a metal material such as aluminium or copper. In this case, the reinforcing member 6 can be formed relatively thinly.

In the tape substrate 4 of the CSP 11 of the first embodiment, the rectangular opening 4e which is elongated almost in parallel with a pair of facing sides of the outer shape is formed in an intermediate part between the sides. Consequently, when the principal surface 1a of the semiconductor chip 1 is attached to the elastomer 3, the plurality of electrode pads 1b arranged in a line in the center pad alignment are exposed from the opening 4e as shown in Fig. 1.

The tape substrate 4 in the CSP 11 of the first embodiment has a substrate body 4a in the area corresponding to the principal surface 1a of the semiconductor chip 1 and a substrate protruded part 4b corresponding to the area extended from the principal surface 1a of the semiconductor chip 1 to the outside. When the

semiconductor chip 1 is adhered to the elastomer 3, the substrate body 4a, the elastomer 3, and the semiconductor chip 1 are stacked and the substrate protruded part 4b of the tape substrate 4 is protruded around the semiconductor chip 1. The frame-shaped reinforcing member 6 is attached via the adhesive layer 8 to a face of the substrate projecting part 4b, which is opposite to the face on which the bump electrodes are mounted.

The elastomer 3 is formed small enough to be within the frame of the reinforcing member 6. The elastomer 3 is an insulating elastic member for supporting the semiconductor chip 1, disposed between the tape substrate 4 and the semiconductor chip 1, and is in contact with the principal surface 1a of the semiconductor chip 1.

The structure and material of each of the members will now be described in detail.

First, in the tape substrate 4, a plurality of bump lands 4f which are electrically connected to the leads 4c and on which the bump electrodes 2 are mounted are provided on the bump electrode mounding side of the tape base material 4g as the base material of the tape substrate 4.

Further, the tape substrate 4 has the tape base material 4g made of a polyimide resin. As shown in Fig. 2, on the surface side of the tape base material 4g, the leads 4c (including the bump lands 4f) made of metal foil such as copper foil are formed. The leads 4c are covered with either a thin Au plating layer, Au/Ni

plating layer or Pd plating layer. The surface side of the tape base material 4g including the plating layer is covered with an insulating film such as a solder resist 4h. The plating layer covering the leads 4c is, for example, a double-sided Au plating layer having a thickness of 1.5 μm or the plating layer whose thickness on the semiconductor chip side and thickness on the bump electrode side are different from each other (as an example, Au/Ni = 3.0/0.5 μm (semiconductor chip side) and 0.3/0.5 μm (bump electrode side)).

The wiring structure of the tape substrate 4 on which the leads 4c are formed on the surface of such a tape base material 4g will be called a surface wiring structure. In the CSP 11 shown in Fig. 2, the tape substrate 4 has the surface wiring structure. The tape substrate 4 in the CSP 11 of the first embodiment may also have a rear face wiring structure such that the leads 4c are formed on the rear face side of the tape base material 4g.

In such a manner, the openings 4d for bumps are formed in positions corresponding to the bump lands 4f, in the solder resist 4h. By disposing the bump electrodes 2 in the openings 4d for bumps, the bump electrodes 2 and the leads 4c are electrically connected to each other via the bump lands 4f.

The elastomer 3 is a porous member and has a three-layer structure of a core layer 3d (also called a base layer or the like) and adhesive layers 3e formed on the surface and back of the core layer 3d (refer to Fig. 11). In this case, the core layer 3d is

made of a porous fluorine plastic or the like and the adhesive layer 3e is made of an epoxy-impregnated porous fluorine plastic or the like.

By making the core layer 3d of the elastomer 3 of a porous fluorine plastic, the air permeability and water repellency can be improved.

The elastomer 3 made of a porous fluorine plastic is constructed by a three-dimensional mesh structure which is a nonwoven fabric formed by tangling a fiber compound in a three-dimensional manner.

The sealed part 5 is formed by sealing the electrode pads 1b on the semiconductor chip 1 and the leads 4c connected to the electrode pads 1b with the sealing resin 9 (refer to Fig. 5).

Although the sealing resin 9 as a sealing material of the sealed part 5 has a relatively high viscosity, by making travel time of a potting nozzle 10 (refer to Fig. 5) at the time of application longer to make application time longer, heating the sealing resin 9, or the like, the sealing resin 9 having a high viscosity can be used.

It is preferable to use a resin containing silica as the sealing resin 9 in order to suppress a residual stress caused by shrinkage when the sealing resin is cured.

Examples of the material of the bump electrode 2 are eutectic solder of Sn/Pb, other solders such as Sn/Ag, Sn/Ag/Cu, Sn/Ag/Bi/Cu, Sn/Ag/Bi and Sn/Bi/Cu, Au plated Ni, and the like.

The diameter of the material is about 0.3 to 0.6 mm.

The embodiment of the CSP 11 of the first embodiment will now be described with reference to Figs. 6 and 7.

Figs. 6 and 7 show an example of mounting the CSP 11 on a card product such as a memory card. A plurality of CSPs 11 are mounted together with a surface mounting type package such as a QFP (Quad Flat Package) 21 onto the same mounting board 22 by reflowing. The mounting board 22 is, for example, a card board. A plurality of external contact leads 22a to be electrically connected to external devices are provided on one of the ends of the mounting board 22.

Referring to Figs. 1 to 5, a process for producing the fan-in and fan-out CSP 11 (semiconductor device) according to the first embodiment will now be described in accordance with the process flow chart of Fig. 3.

First, the tape substrate 4 (also called a flexible wiring board) having a surface wiring structure shown in Fig. 4A in which the leads 4c are provided on one of the faces (surface in the first embodiment since the surface wiring structure is employed) and the opening 4e where a part of each of the leads 4c is disposed is prepared.

The plurality of leads 4c provided on the tape substrate 4 are formed in the width direction of the rectangular opening 4e so as to extend on the inside and outside of the opening 4e.

Further, on the tape substrate 4, the leads 4c made of metal

foil such as copper foil are formed on the surface of the tape base material 4g as the base material of the tape substrate 4. The leads 4c are covered with a thin Au plating layer, Au/Ni plating layer or Pd plating layer. The surface side of the tape base material 4g including the plating layer is covered with an insulating film such as the solder resist 4h.

The tape base material 4g of the tape substrate 4 used for the CSP 11 is made of, for example, a polyimide resin.

On the other hand, the porous elastomer 3 in which the opening 3c having almost the same shape as the opening 4e in the tape substrate 4 is prepared.

Further, the frame-shaped reinforcing member 6 for reinforcing the support by the tape substrate 4 for the bump electrodes 2 disposed on the outside of the semiconductor chip 1 is prepared.

Although the reinforcing member 6 used for the CSP 11 of the embodiment is made of, for example, a polyimide resin, a member made of a metal material other than a polyimide resin such as aluminium (Al) or copper (Cu), or a member obtained by performing a corrosion proofing plating process on the metal member by using Ni, Sn or the like may be also used.

Further, when the reinforcing member 6 is made of a polyimide resin, the tape substrate 4 and the reinforcing member 6 formed so that the total thickness of the polyimide resin of the reinforcing member 6 and that of the tape base material 4g is 100

μm or thicker, preferably, 100 to 175 μm may be also used.

After that, the opening 4e in the tape substrate 4 and the opening 3c in the elastomer 3 are aligned and the tape substrate 4 and the elastomer 3 are adhered to each other.

At this stage, "bonding of elastomer" in step S1 in Fig. 3 is performed.

Specifically, the opening 4e in the tape substrate 4 and the opening 3c in the elastomer 3 are aligned, and the elastomer 3 is bonded to the tape substrate 4 via the adhesive layer 8, thereby obtaining a state as shown in Fig. 4B.

Subsequently, the frame-shaped reinforcing member 6 is disposed around the elastomer 3, and the tape substrate 4 and the reinforcing member 6 are bonded via the adhesive layer 8.

That is, by performing "bonding of reinforcing member" in step S2, the frame-shaped reinforcing member 6 is bonded to the protruded part 4b of the tape substrate 4.

Consequently, as shown in Fig. 4C, a state in which the elastomer 3 is disposed in the frame of the reinforcing member 6 is obtained.

The bonding of the reinforcing member 6 to the tape substrate 4 may be performed either simultaneously with or before the bonding of the elastomer 3.

That is, the order of steps S1 and S2 shown in Fig. 3 may be changed as follows. Before bonding the elastomer 3, first, the tape substrate 4 and the reinforcing member 6 are bonded via

the adhesive layer 8. After that, the elastomer 3 is disposed on the inside of the frame-shaped reinforcing member 6, and the tape substrate 4 and the elastomer 3 are adhered to each other while aligning the openings 4e and 3e.

After that, "bonding of chip" in step S3 is performed.

Specifically, in a state where the semiconductor chip 1 is disposed in the frame-shaped reinforcing member 6 and the plurality of electrode pads 1b on the principal surface 1a of the semiconductor chip 1 are exposed through the two openings 3c and 4e, the principal surface 1a of the semiconductor chip 1 and the elastomer 3 are adhered to each other via the adhesive layer 3e (refer to Fig. 11).

Consequently, as shown in Fig. 4D, a state in which the frame-shaped reinforcing member 6 is disposed around the semiconductor chip 1 and the semiconductor chip 1 is adhered to the elastomer 3 is obtained.

After that, "bonding of lead" shown in step S4 is performed.

To be specific, the electrode pads 1b on the semiconductor chip 1 and the leads 4c disposed in the corresponding openings 4e in the tape substrate 4 are connected to each other.

As shown in Fig. 5A, it is arranged so that the opening 4e in the tape substrate 4 faces upward. The leads 4c are connected to the electrode pads 1b by single-point inner lead bonding using a bonding tool 7.

In this case, first, the bonding tool 7 is positioned over

a predetermined lead 4c in the opening 4e and lowered to press and apply a load to the lead 4c. The lead 4c is pressed and cut by the load.

Further, by the continuous operation of the bonding tool 7, the cut lead 4c is pressed against the electrode pad 1b on the semiconductor chip 1. The lead 4c and the electrode pad 1b are connected to each other by thermo-compression bonding (with ultrasonic wave) or the like.

The operation of the bonding tool 7 is repeatedly performed on the leads 4c, thereby connecting the electrode pads 1b and the corresponding leads 4c one by one.

Then, "sealing" in step S5 is made.

Specifically, the electrode pads 1b on the semiconductor chip 1 and the leads 4c connected to the electrode pads 1b are sealed with a resin to thereby form the sealed portion 5 shown in Fig. 2.

As shown in Fig. 5B, a sealing resin 9 as a sealing material is dropped from a potting nozzle 10 to the opening 4e in the tape substrate 4 by a potting method, thereby sealing the electrode pads 1b on the semiconductor chip 1 and the leads 4c on the tape substrate 4 connected to the electrode pads 1b with the resin.

After elapse of predetermined time, the sealing resin 9 is cured, thereby forming the sealed portion 5. After that, "formation of bumps" in step S6 is carried out.

Specifically, the bump electrodes 2 as external terminals

are formed on the bump lands 4f to be connected to the leads 4c on one of the faces (surface) of the tape substrate 4.

First, solder balls 23 are supplied to the openings 4d for bumps in the solder resist 4h of the tape substrate 4 as shown in Fig. 5C. After that, by performing reflowing, as shown in Fig. 2, the bump electrodes 2 are formed on the bump lands 4f.

Subsequently, marking in step S7 is performed.

For example, a mark such as a model number of the product is printed on the reinforcing member 6 and the like.

After that, "dicing into packages" in step S8 is performed.

To be specific, the tape substrate 4 is diced in predetermined positions by using a cutter or the like into packages, thereby obtaining the CSPs 11 each in a desired size.

Then, a "test" in step S9 is carried out, thereby completing the CSP 11.

In such a manner, the fan-in and fan-out CSP 11 in which the support by the tape substrate 4 for the bump electrodes 2 disposed on the outside of the semiconductor chip 1 is reinforced by the reinforcing member 6 can be obtained.

According to the fan-in and fan-out CSP 11 of the first embodiment and the method of fabricating the CSP 11, the following actions and effects can be obtained.

That is, by providing the reinforcing member 6 disposed on the outside of the semiconductor chip 1, the support for the bump electrodes 2 on the outside of the chip by the tape substrate is

reinforced by the reinforcing member 6. Thus, the plurality of bump electrodes 2 on the outside of the chip can be supported with reliability.

Further, by disposing the porous elastomer 3 on the principal surface 1a of the semiconductor chip 1, no void is formed in the elastomer 3 in the reflowing for forming the bump electrodes or in the reflowing for mounting the CSP 11. Since steam generated in the sealed part 5 can be efficiently discharged to the outside, a reflow crack, that is, occurrence of an inconvenience in the CSP mounting can be prevented.

Thus, the fan-in and fan-out CSP 11 having excellent reflow resistance can be obtained.

Further, by the water repellency of fluorine in the porous fluorine plastic of the elastomer 3, intrusion of moisture into the CSP 11 can be prevented. Thus, deterioration in electric characteristics of the fan-in and fan-out CSP 11 can be reduced.

As a result, the fan-in and fan-out CSP 11 having excellent reflow resistance and high reliability, in which the plurality of bump electrodes 2 on the outside of the chip can be supported with reliability can be realized.

In the fan-in and fan-out CSP 11 in the first embodiment, by setting the total of the thickness of the reinforcing member 6 made of a polyimide resin and the thickness of the polyimide resin of the tape base material 4g in the tape substrate 4 to 100 to 175 μm, the tape substrate 4 can be reinforced by the reinforcing

member 6 and the rigidity of the tape substrate 4 itself can be also enhanced.

As a result, the bump electrodes 2 on the outside of the chip can be supported with higher reliability by the tape substrate 4.

In the fan-in and fan-out CSP 11 of the first embodiment, the tape substrate 4 of the surface wiring structure is used. Consequently, the openings 4d for bumps can be formed in the solder resist 4h without forming the openings 4d for bumps in the tape base material 4g.

Since the tape base material 4g can be therefore formed thickly, the strength in the portion protruded to the outside of the semiconductor chip 1 in the tape substrate 4, that is, the substrate protruded part 4b can be enhanced.

Thus, the support for the bump electrodes 2 disposed on the outside of the chip can be reinforced together with the reinforcing member 6. As a result, the reliability of the fan-in and fan-out CSP 11 can be increased.

Since the support for the bump electrodes 2 disposed on the outside of the chip in the fan-in and fan-out CSP 11 can be reinforced, the smaller and thinner CSP 11 can be mounted in a portable small thin electronic device such as a portable telephone.

The structure of a CSP 12 (refer to Figs. 8 and 9) as a modification of the CSP 11 of the first embodiment will now be

described.

The CSP 11 has the center pad alignment in which the electrode pads 1b on the semiconductor chip 1 are arranged in the center portion. In contrast, the CSP 12 shown in Figs. 8 and 9 has a peripheral pad alignment in which the electrode pads 1b are arranged in the peripheries of the semiconductor chip 1.

In the CSP 12 as the modification of the first embodiment, as shown in Fig. 8, the electrode pads 1b on the semiconductor chip 1 are arranged almost in parallel with a pair of facing sides in the principal surface 1a of the semiconductor chip 1 so as to face each other in the peripheries of the principal surface 1a.

Fig. 9 is a cross section taken along line B-B of the CSP 12 of Fig. 8.

The CSP 12 as the modification shown in Figs. 8 and 9 is obtained by replacing the center pad alignment of the electrode pads 1b on the semiconductor chip 1 in the CSP 11 shown in Figs. 1 and 2 by the peripheral pad alignment.

In the CSP 12, the electrode pads 1b are aligned in the peripheries of the principal surface 1a along the pair of facing sides of the principal surface 1a of the semiconductor chip 1. Consequently, two elongated openings 4e from which the electrode pads 1b in the lines are exposed are formed in the tape substrate 4. The area between the two openings 4e corresponds to the substrate body 4a and the areas on the outside of the openings 4e are the substrate protruded parts 4b.

As shown in Fig. 9, since the porous elastomer 3 is disposed between the facing electrode pad groups 1b, the electrode pad groups 1b can be disposed on both sides of the elastomer 3. In the elastomer 3 in the CSP 12, the opening 3c as in the CSP 11 is not formed.

Since the structure other than the alignment of the electrode pads 1b in the CSP 12 is similar to that of the CSP 11, the repetitive description is omitted here.

Since the method of fabricating the CSP 12 and actions and effects obtained by the CSP 12 and its fabricating method are also similar to those of the CSP 11, the repetitive description is omitted here.

Second Embodiment

Fig. 10 is a plan view showing an example of the structure of a semiconductor device (fan-in and fan-out CSP) according to a second embodiment of the invention, in which a sealing portion is not illustrated. Fig. 11 is a cross section taken along line C-C of the semiconductor device shown in Fig. 10. Fig. 12 is a process flow chart showing an example of a procedure of producing the semiconductor device illustrated in Fig. 10. Figs. 13A to 13C are diagrams each showing the structure in each of steps in the process for producing the semiconductor device illustrated in Fig. 10; Fig. 13A is a perspective view showing a tape substrate, Fig. 13B is a perspective view showing a state in which an elastic

member is adhered, and Fig. 13C is a perspective view showing a state where a chip is bonded. Figs. 14A to 14C are diagrams each showing the structure in each of steps in the process for producing the semiconductor device illustrated in Fig. 10; Fig. 14A is a perspective view showing a state where leads are bonded, Fig. 14B is a perspective view showing a sealing state, and Fig. 14C is a perspective view showing a bump electrodes mounting state. Fig. 15 is a plan view showing the structure of a modification of the semiconductor device (fan-in and fan-out CSP) illustrated in Fig. 10, in which the sealing portion is not shown. Fig. 16 is a cross section taken along line D-D of the semiconductor device shown in Fig. 15.

A CSP 13 (semiconductor device) of the second embodiment is of a fan-in and fan-out type with the center pad alignment similar to the CSP 11 of the first embodiment shown in Fig. 1. The points of the CSP 13 of the second embodiment which are different from the CSP 11 of the first embodiment are as follows. The reinforcing member 6 is not provided but the core layer 3d of the elastomer 3 is formed by using a polyimide resin. In association with the change, the total thickness of the polyimide resin of the core layer 3d and the polyimide resin of the tape base material 4g of the tape substrate 4 is specified, thereby reinforcing the support for the bump electrodes 2 disposed on the outside of the chip by the tape substrate 4.

The elastomer 3 therefore comprises an elastomer body (body

of elastic member) 3a disposed on the principal surface 1a of the semiconductor chip 1 and an elastomer reinforcing part 3b extending on the outside of the principal surface 1a of the semiconductor chip 1.

The elastomer body 3a corresponds to the substrate body 4a of the tape substrate 4, which is disposed on the principal surface 1a of the semiconductor chip 1. Further, the elastomer reinforcing part 3b is disposed in correspondence with the substrate protruded part 4b extended from the principal surface 1a of the semiconductor chip 1. As a result, the support for the bump electrodes 2 disposed on the outside of the semiconductor chip 1 is reinforced by the tape material base 4g in the tape substrate 4 and the elastomer reinforcing part 3b in the elastomer 3.

In the CSP 13, both the core layer 3d of the elastomer 3 and the tape base material 4g of the tape substrate 4 are made of a polyimide resin. For example, the core layer 3d of the elastomer 3 is deposited in thickness of 50 to 125 μm (such as 50 μm, 75 μm or 125 μm). On the other hand, the tape base material 4g of the tape substrate 4 is formed in thickness of about 50 μm. The total thickness of the polyimide resin of the core layer 3d of the elastomer 3 and that of the tape base material 4g of the tape substrate 4 is therefore set to 100 to 175 μm.

By the total thickness of both of the polyimide resin layers, the strength of the support by the tape substrate 4 for the bump

electrodes 2 disposed on the outside of the semiconductor chip 1 can be enhanced.

Since the polyimide resin of the tape base material 4g has to be formed thickly, the wiring structure of the tape substrate 4 in the CSP 13 is a surface wiring structure.

Specifically, by employing the surface wiring structure such that the leads 4c made of copper foil are formed on the surface of the tape base material 4g (face opposite to the face bonded to the elastomer 3), the openings 4d for bumps can be formed in the solder resist 4h. Consequently, the tape base material 4g can be formed thickly.

The CSP 13 therefore uses the tape substrate 4 of the surface wiring structure.

Since the other structure in the CSP 13 of the second embodiment is similar to that of the CSP 11 described in the first embodiment, its repetitive description is omitted here.

Referring to Figs. 10 to 14, a process for producing the fan-in and fan-out CSP 13 (semiconductor device) according to the second embodiment will be described in accordance with the process flow chart of Fig. 12.

First, in a manner similar to the first embodiment, the tape substrate 4 (also called a flexible wiring board) of the surface wiring structure shown in Fig. 13A in which the leads 4c are provided on one of the faces (surface) and the opening 4e in which a part of each of the leads 4c is disposed is formed is prepared.

The plurality of leads 4c formed on the tape substrate 4 are formed in the width direction of the rectangular opening 4e so as to extend on the inside and outside of the opening 4e.

In the tape substrate 4 used for the CSP 13, the tape base material 4g is made of, for example, a polyimide resin. Further, since the polyimide resin of the tape base material 4g has to be formed thickly, the surface wiring structure is employed.

On the other hand, the elastomer 3 is prepared in which the opening 3c having almost the same shape as that of the opening 4e in the tape substrate 4 is formed. The elastomer 3 comprises the elastomer body 3a and the elastomer reinforcing part 3b and the core layer 3d is made of a polyimide resin.

For example, the tape substrate 4 and the elastomer 3 are used such that the core layer 3d of the elastomer 3 is formed in thickness of 50 to 125 μm and the tape base material 4g of the tape substrate 4 is formed in thickness of about 50 μm, so that the total thickness of the polyimide resin of the core layer 3d of the elastomer 3 and that of the polyimide resin of the tape base material 4g of the tape substrate 4 becomes 100 to 175 μm.

After that, the opening 4e in the tape substrate 4 and the opening 3c in the elastomer 3 are aligned and the tape substrate 4 and the elastomer 3 are adhered to each other.

At this stage, "bonding of the elastomer" in step S1 in Fig. 12 is performed.

Specifically, the opening 4e in the tape substrate 4 and

the opening 3c in the elastomer 3 are aligned, and the elastomer 3 is adhered to the tape substrate 4 via the adhesive layer 8, thereby obtaining a state as shown in Fig. 13B.

After that, "bonding of chip" in step S2 is performed.

Specifically, in a state where the plurality of electrode pads 1b on the principal surface 1a of the semiconductor chip 1 are exposed through the two openings 3c and 4e, the principal surface 1a of the semiconductor chip 1 and the elastomer 3 are adhered via the adhesive layer 3e.

Consequently, as shown in Figs. 11 and 13C, the semiconductor chip 1 is bonded to the elastomer 3 in a state where the substrate protruded part 4b and the elastomer reinforcing part 3b are extended around the semiconductor chip 1.

After that, "bonding of lead" shown in step S3 is performed.

To be specific, the electrode pads 1b on the semiconductor chip 1 and the corresponding leads 4c disposed in the opening 4e in the tape substrate 4 are connected to each other.

As shown in Fig. 14A, it is arranged so that the opening 4e in the tape substrate 4 faces upward. The leads 4c are connected to the electrode pads 1b by single-point inner lead bonding using the bonding tool 7.

In this case, in a manner similar to the first embodiment, the bonding tool 7 is positioned over a predetermined lead 4c in the opening 4e and lowered to press and apply a load to the lead 4c. The lead 4c is pressed and cut by the load.

Further, by the continuous operation of the bonding tool 7, the cut lead 4c is pressed against the electrode pad 1b on the semiconductor chip 1. The lead 4c and the electrode pad 1b are connected to each other by thermo-compression bonding (with ultrasonic wave) or the like.

The operation of the bonding tool 7 is repeatedly performed on the leads 4c, thereby connecting the electrode pads 1b and the corresponding leads 4c one by one.

Then, "sealing" in step S4 is made.

Specifically, the electrode pads 1b on the semiconductor chip 1 and the leads 4c connected to the electrode pads 1b are sealed with a resin to thereby form the sealed portion 5 shown in Fig. 11.

As shown in Fig. 14B, the sealing resin 9 as a sealing material is dropped from the potting nozzle 10 to the opening 4e in the tape substrate 4 by a potting method, thereby sealing the electrode pads 1b on the semiconductor chip 1 and the leads 4c on the tape substrate 4 connected to the electrode pads 1b with the resin.

After elapse of predetermined time, the sealing resin 9 is cured, thereby forming the sealed portion 5. Then, "formation of bumps" in step S5 is carried out.

Specifically, the bump electrodes 2 as external terminals are formed on the bump lands 4f to be connected to the leads 4c on one of the faces (surface) of the tape substrate 4.

First, the solder balls 23 are supplied to the opening 4d for bumps in the solder resist 4h of the tape substrate 4 as shown in Fig. 14C. After that, by performing reflowing, as shown in Fig. 11, the bump electrodes 2 are formed on the bump lands 4f.

Subsequently, marking in step S6 is performed.

For example, a mark such as a model number of the product is on the elastomer 3 and the like.

After that, "dicing into packages" in step S7 is performed.

To be specific, the tape substrate 4 is diced in predetermined positions by using a cutter or the like into packages, thereby obtaining the CSPs 13 each in a desired size.

Then, a "test" in step S8 is carried out, thereby completing the CSP 13.

In such a manner, the fan-in and fan-out CSP 13 in which the support by the tape substrate 4 for the bump electrodes 2 disposed on the outside of the semiconductor chip 1 is reinforced by the tape base material 4g of the tape substrate 4 and the core layer 3d of the elastomer 3 can be obtained.

According to the fan-in and fan-out CSP 13 of the second embodiment and the method of fabricating the CSP 13, the following actions and effects can be obtained.

That is, by providing the tape substrate 4 and the elastomer 3 extending from the semiconductor chip 1 to the outside and by setting the total thickness of the polyimide resin of the tape base material 4g in the tape substrate 4 and the polyimide resin

of the core layer 3d in the elastomer 3 to 100 to 175 μm, the bump electrodes 2 disposed on the outside of the chip can be supported with reliability without providing the reinforcing member 6 used for the CSP 11 shown in Fig. 1.

Since the tape substrate 4 of the surface wiring structure is used in the CSP 13, the tape base material 4g made of a polyimide resin in the tape substrate 4 can be formed thickly. As a result, the support by the tape substrate 4 for the bump electrodes 2 disposed on the outside of the chip can be reinforced.

Since the CSP 13 can be assembled without using the reinforcing member 6, the production (assembly) of the fan-in and fan-out CSP 13 can be facilitated.

Consequently, the fan-in and fan-out CSP 13 which is produced easily and in which the plurality of bump electrodes 2 on the outside of the chip are supported with reliability can be realized.

Since the CSP 13 does not use the reinforcing member 6, the cost is lower as compared with the CSP 11 shown in Fig. 1.

Further, since the core layer 3d in the elastomer 3 is made of a polyimide resin, the cost can be made lower as compared with the porous elastomer 3. The cost of the CSP 13 can be accordingly reduced.

The structure of a CSP 14 (refer to Figs. 15 and 16) as a modification of the CSP 13 of the second embodiment will now be described.

The CSP 13 has the center pad alignment in which the electrode pads 1b on the semiconductor chip 1 are aligned in the center portion. In contrast, the CSP 14 shown in Figs. 15 and 16 has a peripheral pad alignment in which the electrode pads 1b on the semiconductor chip 1 are aligned in the peripheries.

In the CSP 14 as the modification of the second embodiment, as shown in Fig. 15, the electrode pads 1b on the semiconductor chip 1 are arranged almost in parallel with a pair of facing sides in the principal surface 1a of the semiconductor chip 1 in the peripheries of the principal surface 1a so as to face each other.

Fig. 16 is a cross section taken along line D-D of the CSP 14 of Fig. 15.

The CSP 14 as the modification shown in Figs. 15 and 16 is obtained by replacing the center pad alignment of the electrode pads 1b on the semiconductor chip 1 in the CSP 13 shown in Figs. 10 and 11 by the peripheral pad alignment.

In the CSP 14, the electrode pads 1b are aligned in the peripheries of the principal surface 1a along the pair of facing sides in the principal surface 1a of the semiconductor chip 1. Consequently, two elongated openings 4e from which the electrode pads 1b in the lines are exposed are formed in the tape substrate 4. The area between the two openings 4e corresponds to the substrate body 4a and the areas on the outside of the openings 4e are the substrate protruded parts 4b.

As shown in Fig. 16, in correspondence with the tape

substrate 4, the elastomer 3 comprises: the elastomer body part 3a (area between the two openings 3c) disposed on the principal surface 1a of the semiconductor chip 1; and the elastomer reinforcing parts 3b (areas on the outside of the openings 3c) extending on the outside of the principal surface 1a of the semiconductor chip 1.

That is, the elastomer body part 3a corresponds to the substrate body part 4a in the tape substrate 4, which is disposed on the principal surface 1a of the semiconductor chip 1 and, further, the elastomer reinforcing part 3b is disposed on the substrate protruded part 4b which extends from the principal surface 1a of the semiconductor chip 1. Consequently, the support by the tape substrate 4 for the bump electrodes 2 disposed on the outside of the semiconductor chip 1 is reinforced by the tape base material 4g in the tape substrate 4 and the elastomer reinforcing part 3b in the elastomer 3.

Since the structure other than the alignment of the electrode pads 1b in the CSP 14 is similar to that of the CSP 13, the repetitive description is omitted here.

Since the method of fabricating the CSP 14 and actions and effects obtained by the CSP 14 and its fabricating method are also similar to those of the CSP 13, the repetitive description is omitted here.

Third Embodiment

Fig. 17 is a plan view showing an example of the structure of a semiconductor device (fan-in and fan-out CSP) according to a third embodiment of the invention, in which a sealing portion is not illustrated. Fig. 18 is a cross section taken along line E-E of the semiconductor device shown in Fig. 17. Fig. 19 is a plan view showing the structure of a modification of the semiconductor device (fan-in and fan-out CSP) illustrated in Fig. 17, in which the sealing portion is omitted. Fig. 20 is a cross section take along line F-F of the semiconductor device shown in Fig. 19.

A CSP 15 (semiconductor device) of the third embodiment is of a fan-in and fan-out type with the center pad alignment similar to the CSP 13 of the second embodiment shown in Fig. 11. The different point of the CSP 15 of the third embodiment from the CSP 13 of the second embodiment is that the support for the bump electrodes 2 disposed on the outside of the chip by the tape substrate 4 is reinforced by using the elastomer 3 which is formed thickly.

Similar to the CSP 13, the elastomer 3 comprises the elastomer body (body of elastic member) 3a disposed on the principal surface 1a of the semiconductor chip 1 and the elastomer reinforcing part 3b (elastic member reinforcing part) extending on the outside of the principal surface 1a of the semiconductor chip 1.

The elastomer body 3a corresponds to the substrate body 4a

in the tape substrate 4, which is disposed on the principal surface 1a of the semiconductor chip 1. Further, the elastomer reinforcing part 3b is disposed on the substrate protruded part 4b extended from the principal surface 1a of the semiconductor chip 1. As a result, the support for the bump electrodes 2 disposed on the outside of the semiconductor chip 1 is reinforced by the elastomer reinforcing part 3b formed thickly.

The elastomer 3 in the CSP 15 has a three-layer structure of the core layer 3d and the adhesive layers 3e formed on both faces of the core layer 3d. Examples of the thickness of each of the layers are as follows. The core layer 3d is 50 μm thick, the adhesive layer 3e on the chip side is 50 μm thick, and the adhesive layer 3e on the tape side is 75 μm thick (total 175 μm). In another example, the core layer 3d is 75 μm thick, the adhesive layer 3e on the chip side is 50 μm thick, and the adhesive layer 3e on the tape side is 75 μm thick (total 200 μm). In further another example, the core layer 3d is 125 μm thick, the adhesive layer 3e on the chip side is 50 μm thick, and the adhesive layer 3e on the tape side is 75 μm thick (total 250 μm).

In the CSP 15, the core layer 3d in the elastomer 3 is made of a polyimide resin. The tape base material 4g in the tape substrate 4 is also made of a polyimide resin. For example, the core layer 3d in the elastomer 3 is formed in thickness of 50 to 125 μm as described above. On the other hand, the tape base material 4g in the tape substrate 4 is formed relatively thin in

thickness of about 50 μm.

In the CSP 15 of the third embodiment, with respect to the relation of the thickness of the elastomer 3 and that of the tape substrate 4, it is sufficient that the thickness of the elastomer 3 is equal to or thicker than the tape substrate 4.

Consequently, by the elastomer reinforcing part 3b in the elastomer 3 formed thickly, the strength of the support by the tape substrate 4 for the bump electrodes 2 disposed on the outside of the semiconductor chip 1 can be enhanced.

The tape substrate 4 in the CSP 15 has the rear face wiring structure.

That is, the leads 4c made of copper foil are formed on the rear face of the tape base material 4g (face bonded to the elastomer 3) in the tape substrate 4.

Since the other structure in the CSP 15 of the third embodiment is similar to that of the CSP 13 described in the second embodiment, its repetitive description is omitted here.

The method of fabricating the CSP 15 in the third embodiment is substantially the same as that of the CSP 13 in the second embodiment. The different point is as follows. Since the tape substrate 4 of the rear face wiring structure is used, when the bump electrodes 2 as external terminals are formed on the tape substrate 4, the bump electrodes 2 are electrically connected to the leads 4c via the openings 4d for bumps provided in the mounting positions of the bumps in the tape base material 4g.

When the tape substrate 4 and the semiconductor chip 1 are adhered via the elastomer 3 which is formed thickly, the substrate protruded part 4b in the tape substrate 4 and the elastomer reinforcing part 3b in the elastomer 3 extend from the whole periphery of the semiconductor chip 1 to the outside.

Since the method of fabricating the CSP 15 of the third embodiment except for the above is similar to that of the CSP 13 of the second embodiment, its repetitive description is omitted here.

According to the fan-in and fan-out CSP 15 of the third embodiment and the method of fabricating the CSP 15, the following actions and effects can be obtained.

That is, by providing the tape substrate 4 and the elastomer 3 extending from the semiconductor chip 1 to the outside and by using the tape substrate 4 of the back face wiring structure, the elastomer 3 can be formed thickly. As a result, even when the tape substrate 4 is formed thinly, the bump electrodes 2 disposed on the outside of the chip can be supported with reliability without providing the reinforcing member 6 used for the CSP 11 shown in Fig. 1.

By using the tape substrate 4 of the back face wiring structure, the elastomer 3 can be formed thickly and the openings 4d for bumps are formed directly in the tape base material 4g without needing the solder resist 4h as in the surface wiring structure. Thus, the process for producing the tape substrate

4 in the process for producing the CSP 15 can be simplified.

As a result, the cost of producing the CSP 15 can be reduced.

Further, since the solder resist 4h is unnecessary for the tape substrate 4, the cost of the tape substrate 4 itself can be reduced and, accordingly, the cost of the CSP 15 can be reduced.

The tape base material 4g in the tape substrate 4 can be made thickly. In this case, since the elastomer 3 is also formed thickly, the rigidity of the substrate protruded part 4b in the tape substrate 4 and the elastomer reinforcing part 3b can be enhanced. As a result, the bump electrodes 2 disposed on the outside of the chip can be supported with reliability.

Since the core layer 3d in the elastomer 3 is made of a polyimide resin, the cost can be made lower as compared with the porous elastomer 3. The cost of the CSP 15 can be accordingly reduced.

The structure of a CSP 16 (refer to Figs. 19 and 20) as a modification of the CSP 15 of the third embodiment will now be described.

The CSP 15 has the center pad alignment in which the electrode pads 1b on the semiconductor chip 1 are aligned in the center portion. In contrast, the CSP 16 shown in Figs. 19 and 20 has a peripheral pad alignment in which the electrode pads 1b on the semiconductor chip 1 are aligned in the peripheries.

In the CSP 16 as the modification of the third embodiment, as shown in Fig. 19, the electrode pads 1b on the semiconductor

chip 1 are arranged almost in parallel with a pair of facing sides in the principal surface 1a of the semiconductor chip 1 in the peripheries of the principal surface 1a so as to face each other.

Fig. 20 is a cross section taken along line F-F of the CSP 16 of Fig. 19.

The CSP 16 as the modification shown in Figs. 19 and 20 is obtained by replacing the center pad alignment of the electrode pads 1b on the semiconductor chip 1 in the CSP 15 shown in Figs. 17 and 18 by the peripheral pad alignment.

In the CSP 16, the electrode pads 1b are aligned in the peripheries of the principal surface 1a along the pair of facing sides of the principal surface 1a of the semiconductor chip 1. Consequently, two elongated openings 4e from which the electrode pads 1b in the lines are exposed are formed in the tape substrate 4. The area between the two openings 4e corresponds to the substrate body 4a and the areas on the outside of the openings 4e are the substrate protruded parts 4b.

As shown in Fig. 20, in correspondence with the tape substrate 4, the elastomer 3 comprises: the elastomer body part 3a (area between the two openings 3c) disposed on the principal surface 1a of the semiconductor chip 1; and the elastomer reinforcing parts 3b (areas on the outside of the openings 3c) extending on the outside of the principal surface 1a of the semiconductor chip 1.

That is, the elastomer body part 3a corresponds to the

substrate body part 4a in the tape substrate 4, which is disposed over the principal surface 1a of the semiconductor chip 1 and, further, the elastomer reinforcing part 3b corresponds to the substrate protruded part 4b which extends from the principal surface 1a of the semiconductor chip 1. Consequently, the support by the tape substrate 4 for the bump electrodes 2 disposed on the outside of the semiconductor chip 1 is reinforced by the tape base material 4g in the tape substrate 4 and the elastomer reinforcing part 3b in the elastomer 3 which is formed thickly.

Since the structure other than the alignment of the electrode pads 1b in the CSP 16 is similar to that of the CSP 15, the repetitive description is omitted here.

Since the method of fabricating the CSP 16 and actions and effects obtained by the CSP 16 and its fabricating method are also similar to those of the CSP 15, the repetitive description is omitted here.

Fourth Embodiment

Fig. 21 is a plan view showing an example of the structure of a semiconductor device (fan-in and fan-out CSP) according to a fourth embodiment of the invention, in which the sealing portion is omitted. Fig. 22 is a cross section taken along line G-G of the semiconductor device shown in Fig. 21. Fig. 23 is a plan view showing the structure of a modification of the semiconductor device illustrated in Fig. 21, in which the sealing portion is

omitted. Fig. 24 is a cross section taken along line H-H of the semiconductor decide shown in Fig. 23.

A CSP 17 (semiconductor device) of the fourth embodiment is of a fan-in and fan-out type with the center pad alignment similar to the CSP 13 of the second embodiment shown in Fig. 10. The point of the CSP 13 of the second embodiment which is different from the CSP 17 of the fourth embodiment is that a porous elastomer 3 is used. Consequently, the support for the bump electrodes 2 disposed on the outside of the chip is reinforced by forming the tape substrate 4 thickly.

The elastomer 3 has a three-layer structure of the core layer 3d and the adhesive layers 3e formed on both faces of the core layer 3d. The core layer 3d is made of a porous fluorine plastic and the adhesive layers 3e are made of an epoxy-impregnated porous fluorine plastic.

The elastomer 3 in the CSP 17 has substantially the same size as the tape substrate 4. The elastomer 3 is disposed on the principal surface 1a of the semiconductor chip 1 and is also disposed on the substrate protruded part 4b in the tape substrate 4.

In the reflowing for forming the bump electrodes or in the reflowing for mounting the CSP 17, no void is therefore formed in the elastomer 3.

Further, by the water repellency of fluorine in the porous fluorine plastic of the elastomer 3, intrusion of moisture into

the CSP 17 can be prevented.

Since the polyimide resin of the tape base material 4g has to be formed thickly, the tape substrate 4 in the CSP 17 has the surface wiring structure.

Specifically, by using the surface wiring structure such that the leads 4c made of copper foil are formed on the surface (face opposite to the side to which the elastomer 3 is bonded) of the tape base material 4g, the openings 4d for bumps can be formed in the solder resist 4h. Thus, the tape base material 4g can be formed thickly.

In this case, the thickness of the tape base material 4g made of a polyimide resin in the tape substrate 4 used for the CSP 17 is, for example, 100 μm or thicker.

In such a manner, the tape base material 4g can be formed thickly and the support for the bump electrodes 2 disposed on the outside of the chip can be reinforced.

Since the other structure of the CSP 17 of the fourth embodiment is similar to that of the CSP 13 described in the second embodiment, its repetitive description is omitted here.

Since the method of fabricating the CSP 17 of the fourth embodiment is similar to that of the CSP 13 of the second embodiment, its repetitive description is omitted here.

According to the fan-in and fan-out CSP 17 of the fourth embodiment and the method of fabricating the CSP 17, the following actions and effects can be obtained.

That is, by providing the tape substrate 4 and the elastomer 3 extending from the semiconductor chip 1 to the outside and by using the tape substrate 4 of the surface wiring structure, the tape base material 4g made of the polyimide resin in the tape substrate 4 can be formed thickly. By using the tape substrate 4 in which the tape base material 4g is formed in thickness of 100 μm or thicker, the rigidity of the tape substrate 4 can be enhanced.

As a result, the support for the bump electrodes 2 disposed on the outside of the chip can be reinforced.

The core layer 3d in the elastomer 3 is made of a porous fluorine plastic and the adhesive layer 3e is made of an epoxy-impregnated porous fluorine plastic, so that the porous elastomer 3 is disposed on the principal surface 1a of the semiconductor chip 1. Therefore, no void is formed in the elastomer 3 in the reflowing for forming the bump electrodes or in the reflowing for mounting the CSP 17. Since steam generated in the sealed part 5 can be efficiently discharged to the outside, a reflow crack, that is, occurrence of an inconvenience in the CSP mounting can be prevented.

Thus, the fan-in and fan-out CSP 17 having excellent reflow resistance can be obtained.

Further, by the water repellency of fluorine in the porous fluorine plastic of the elastomer 3, intrusion of moisture into the CSP 17 can be prevented. Accordingly, deterioration in

electric characteristics of the fan-in and fan-out CSP 17 can be reduced.

As a result, the fan-in and fan-out CSP 17 having excellent reflow resistance and high reliability, in which the plurality of bump electrodes 2 on the outside of the chip can be supported with reliability can be realized.

Since the CSP 17 can be produced without using the reinforcing member 6 as in the CSP 11 shown in Fig. 1, the production (assembly) of the fan-in and fan-out CSP 17 can be facilitated.

The fan-in and fan-out CSP 17 which is produced easily and in which the plurality of bump electrodes 2 on the outside of the chip are supported with reliability can be realized.

Since the reinforcing member 6 is not used in the CSP 17, the cost is lower as compared with that of the CSP 11.

The structure of a CSP 18 (refer to Figs. 23 and 24) as a modification of the CSP 17 of the fourth embodiment will now be described.

The CSP 17 has the center pad alignment in which the electrode pads 1b on the semiconductor chip 1 are aligned in the center portion. In contrast, the CSP 18 shown in Figs. 23 and 24 has a peripheral pad alignment in which the electrode pads 1b on the semiconductor chip 1 are aligned in the peripheries.

In the CSP 18 as the modification of the fourth embodiment, as shown in Fig. 23, the electrode pads 1b on the semiconductor

chip 1 are arranged almost in parallel with a pair of facing sides in the principal surface 1a of the semiconductor chip 1 so as to face each other in the peripheries of the principal surface 1a.

Fig. 24 is a cross section taken along line H-H of the CSP 18 of Fig. 23.

The CSP 18 as the modification shown in Figs. 23 and 24 is obtained by replacing the center pad alignment of the electrode pads 1b on the semiconductor chip 1 in the CSP 17 shown in Figs. 21 and 22 by the peripheral pad alignment.

In the CSP 18, the electrode pads 1b are aligned in the peripheries of the principal surface 1a along the pair of facing sides of the principal surface 1a of the semiconductor chip 1. Consequently, two elongated openings 4e from which the electrode pads 1b in the lines are exposed are formed in the tape substrate 4. The area between the two openings 4e corresponds to the substrate body 4a and the areas on the outside of the openings 4e are the substrate protruded parts 4b.

The elastomer 3 has almost the same size as that of the tape substrate 4. The two openings 3c corresponding to the two openings 4e are formed in the elastomer 3. The elastomer 3 comprises the parts corresponding to the substrate body part 4a and the substrate protruded part 4b, that is, the part (elastomer body part 3a) disposed on the principal surface 1a of the semiconductor chip 1 and the part (elastomer reinforcing part 3b) extending from the principal surface 1a to the outside of the chip.

Consequently, the support by the tape substrate 4 for the bump electrodes 2 disposed on the outside of the semiconductor chip 1 is reinforced by the tape base material 4g which is formed in thickness of 100 μm or thicker.

Since the structure other than the alignment of the electrode pads 1b in the CSP 18 is similar to that of the CSP 17, the repetitive description is omitted here.

Since the method of fabricating the CSP 18 and actions and effects obtained by the CSP 18 and its fabricating method are also similar to those of the CSP 17, the repetitive description is omitted here.

Fifth Embodiment

Fig. 25 is a plan view showing an example of the structure of a semiconductor device (fan-in and fan-out CSP) according to a fifth embodiment of the invention, in which the sealed part is not illustrated. Fig. 26 is a cross section taken along line I-I of the semiconductor device shown in Fig. 25. Fig. 27 is a plan view showing the structure of a modification of the semiconductor device (fan-in and fan-out CSP) illustrated in Fig. 25, in which the sealing portion is omitted. Fig. 28 is a cross section taken along line J-J of the semiconductor device shown in Fig. 27.

A CSP 19 (semiconductor device) of the fifth embodiment is of a fan-in and fan-out type with the center pad alignment in a manner similar to the CSP 17 of the second embodiment shown in

Fig. 21. The different point of the CSP 19 of the fifth embodiment from the CSP 17 of the fourth embodiment is that, not the porous elastomer 3 but an elastomer 3f without a core layer (elastic body without a core layer) is used.

Consequently, the support for the bump electrodes 2 disposed on the outside of the chip is reinforced by forming the tape substrate 4 thickly in a manner similar to the CSP 17 of the fourth embodiment.

The elastomer 3f without a core layer in the CSP 19 is, for example, a member which is made of an acrylic/epoxy resin and has an adhering function. Since the elastomer 3f does not have the core layer 3d as in the CSP 17, it is cheap and can be formed thinly.

In a manner similar to the CSP 17, the elastomer 3f without a core layer has almost the same size as the tape substrate 4 and is disposed on the principal surface 1a of the semiconductor chip 1 and also on the substrate protruded part 4b of the tape substrate 4 on the outside.

Since the polyimide resin of the tape base material 4g has to be formed thickly, the tape substrate 4 in the CSP 19 has the surface wiring structure.

By using the surface wiring structure in which the leads 4c made of copper foil are formed on the surface of the tape base material 4g, the openings 4d for bumps can be formed in the solder resist 4h in a manner similar to the CSP 17. Thus, the tape base material 4g can be formed thickly.

In this case, the thickness of the tape base material 4g made of a polyimide resin in the tape substrate 4 used for the CSP 19 is, for example, 100 μm or thicker.

In such a manner, the tape base material 4g can be formed thickly and the support for the bump electrodes 2 disposed on the outside of the chip can be reinforced.

Since the other structure of the CSP 19 of the fourth embodiment is similar to that of the CSP 17 described in the fourth embodiment, its repetitive description is omitted here.

Since the method of fabricating the CSP 19 of the fifth embodiment is similar to that of the CSP 13 of the second embodiment, its repetitive description is omitted here.

According to the fan-in and fan-out CSP 19 of the fifth embodiment and the method of fabricating the CSP 19, the following actions and effects can be obtained.

That is, by providing the tape substrate 4 and the elastomer 3 without a core layer extending from the semiconductor chip 1 to the outside and by using the tape substrate 4 of the surface wiring structure, the tape base material 4g made of the polyimide resin in the tape substrate 4 can be formed thickly. By using the tape substrate 4 in which the tape base material 4g is formed in thickness of 100 μm or thicker, the rigidity of the tape substrate 4 can be enhanced.

As a result, the support for the bump electrodes 2 disposed on the outside of the chip can be reinforced.

By using the elastomer 3f without a core layer, the elastomer 3f can be formed thinly and the cost can be reduced.

Consequently, the CSP 19 can be made smaller and thinner and the cost can be reduced.

Since the CSP 19 can be produced without using the reinforcing member 6 as in the CSP 11 shown in Fig. 1, the production (assembly) of the fan-in and fan-out CSP 19 can be facilitated.

The fan-in and fan-out CSP 19 which is produced easily and in which the plurality of bump electrodes 2 on the outside of the chip are supported with reliability can be realized.

Since the reinforcing member 6 is not used in the CSP 19, the cost is lower as compared the CSP 11.

The structure of a CSP 20 (refer to Figs. 27 and 28) as a modification of the CSP 19 of the fifth embodiment will now be described.

The CSP 19 has the center pad alignment in which the electrode pads 1b on the semiconductor chip 1 are aligned in the center portion. In contrast, the CSP 20 shown in Figs. 27 and 28 has a peripheral pad alignment in which the electrode pads 1b on the semiconductor chip 1 are aligned in the peripheries.

In the CSP 20 as the modification of the fifth embodiment, as shown in Fig. 27, the electrode pads 1b on the semiconductor chip 1 are aligned almost in parallel with a pair of facing sides in the principal surface 1a of the semiconductor chip 1 so as to

face each other in the peripheries of the principal surface 1a.

Fig. 28 is a cross section taken along line J-J of the CSP 20 of Fig. 27.

The CSP 20 as the modification shown in Figs. 27 and 28 is obtained by replacing the center pad alignment of the electrode pads 1b on the semiconductor chip 1 in the CSP 19 shown in Figs. 25 and 26 by the peripheral pad alignment.

In the CSP 20, the electrode pads 1b are aligned in the peripheries of the principal surface 1a along the pair of facing sides of the principal surface 1a of the semiconductor chip 1. Consequently, two elongated openings 4e from which the electrode pads 1b in the lines are exposed are formed in the tape substrate 4. The area between the two openings 4e corresponds to the substrate body part 4a and the areas on the outside of the openings 4e are the substrate protruded parts 4b.

The elastomer 3f without a core layer has almost the same size as the tape substrate 4. The two openings 3c corresponding to the two openings 4e are formed in the elastomer 3f. The elastomer 3f comprises the parts corresponding to the substrate body part 4a and the substrate protruded part 4b, that is, the part disposed on the principal surface 1a of the semiconductor chip 1 and the part extending from the principal surface 1a to the outside of the chip.

The support by the tape substrate 4 for the bump electrodes 2 disposed on the outside of the semiconductor chip 1 is reinforced

by the tape base material 4g which is formed thickly in thickness of 100 μm or thicker.

Since the structure other than the alignment of the electrode pads 1b in the CSP 20 is similar to that of the CSP 19, the repetitive description is omitted here.

Since the method of fabricating the CSP 20 and actions and effects obtained by the CSP 20 and its fabricating method are also similar to those of the CSP 19, the repetitive description is omitted here.

Sixth Embodiment

Fig. 29 is a plan view showing an example of the structure of a semiconductor device (fan-in and fan-out CSP) according to a sixth embodiment of the invention, in which the sealing portion is not illustrated. Fig. 30 is a cross section taken along line K-K of the semiconductor device shown in Fig. 29.

A CSP 30 (semiconductor device) of the sixth embodiment is of a fan-in and fan-out type with the center pad alignment similar to the CSP 11 of the first embodiment shown in Fig. 1. The different point of the CSP 30 of the sixth embodiment from the CSP 11 of the first embodiment is that the electrode pad 1b on the semiconductor chip 1 is connected to the corresponding lead 4c on the tape substrate 4 by wire bonding using a wire 24 for bonding.

Specifically, as shown in Fig. 30, an opening 4i for bonding

from which an end (a part) of each of the leads 4c is exposed is formed in the solder resist 4h of the tape substrate 4. The end of each of the leads 4c exposed from the opening 4i for bonding is connected to each of the electrode pads 1b on the semiconductor chip 1 via the wire 24.

Although each of the leads 4c on the tape substrate 4 extends toward the opening 4e from which the electrode pads 1b on the semiconductor chip 1 are exposed, the lead 4c is not disposed in the opening 4e but is terminated in a state where it is covered with the solder resist 4h.

Since the end (end opposite to the side connected to the bump electrode 2) of each of the leads 4c on the tape substrate 4 is subjected to the wire bonding, not only the opening 4e in the tape substrate 4 but also the joint between the lead 4c and the wire 24 is also covered with the sealing portion 5.

That is, the opening 4e in the tape substrate 4 and the joints between the leads 4c and the wires 24 are covered with the sealing portion 5 in the CSP 30. The sealing portion 5 is therefore formed in a wider range than the sealing portion 5 in the CSP 11.

The end opposite to the end to which the wire 24 is bonded in each of the leads 4c is electrically connected to the bump electrode 2 in a manner similar to the CSP 11.

As shown in Fig. 30, the tape substrate 4 used for the CSP 30 of the sixth embodiment has the surface wiring structure in which the leads 4c are formed on the surface of the tape base

material 4g.

The wire 24 used for the wire bonding is, for example, a metal wire. A copper wire or the like may be also used.

Since the other structure in the CSP 30 of the sixth embodiment is similar to that of the CSP 11 described in the first embodiment, its repetitive description is omitted here.

A process for producing the CSP 30 of the sixth embodiment will now be described.

The process for producing the CSP 30 is similar to that of the CSP 11 but is different with respect to the following point. In "bonding of lead" in step S4 in Fig. 3, the wire bonding is performed, thereby connecting the electrode pad 1b on the semiconductor chip 1 and the lead 4c on the tape substrate 4 via the wire 24 for bonding such as a metal wire.

After completion of "bonding of chip" in step S3, the wire bonding is performed by using a wire bonding apparatus in step S4. By the wire bonding, the electrode pad 1b on the semiconductor chip 1 exposed from the opening 4e in the tape substrate 4 and the corresponding end (a part) exposed from the opening 4i for bonding, of the lead 4c on the tape substrate 4 are connected via the wire 24 for bonding.

After that, "sealing" in step S5 is carried out.

Specifically, a sealing material is dropped to the opening 4e in the tape substrate 4 to seal the electrode pad 1b on the semiconductor chip 1 and the wire 24 for bonding connected to the

electrode pad 1b with the resin. The sealing material is also dropped to the joint between the lead 4c and the wire 24 around the opening 4e, thereby forming the sealing portion 5.

Then, steps S6 to S9 are carried out in a manner similar to the fabrication of the CSP 11 of the first embodiment, thereby completing the CSP 30.

According to the fan-in and fan-out CSP 30 of the sixth embodiment and the method of fabricating the CSP 30, the following actions and effects are obtained.

In the CSP 30, since the electrode pads 1b on the semiconductor chip 1 and the corresponding leads 4c on the tape substrate 4 are bonded by the wire bonding using the wires 24, an assembling apparatus such as an existing wire bonder can be used in the producing process. As a result, the manufacturing cost of the CSP 30 can be suppressed.

Since the other actions and effects are similar to those of the CSP 11 of the first embodiment, its repetitive description is omitted here.

Although the CSP 30 of the sixth embodiment shown in Figs. 29 and 30 is of the center pad alignment, the structure of connecting the electrode pads 1b on the semiconductor chip 1 and the corresponding leads 4c on the tape substrate 4 by wire bonding and the method of fabricating the structure can be also applied to a CSP of the peripheral pad alignment in a manner similar to the first to fifth embodiments. The actions and effects obtained

by the peripheral pad alignment are similar to those of the CSP 30 of the center pad alignment.

Although the invention achieved by the inventor has been specifically described on the basis of the first to six embodiments of the invention, the invention is not limited to the foregoing first to six embodiments of the invention but, obviously, can be variously modified without departing from the gist.

For example, although the case where the semiconductor chip 1 has a rectangular shape has been described in the first to six embodiments, the semiconductor chip 1 may have a square shape.

Further, in the case of the peripheral pad alignment, the mounting positions of the electrode pads 1b provided for the semiconductor chip 1 are not limited to the both ends but can be provided in anywhere as long as it is in the peripheral area in the principal surface 1a of the semiconductor chip 1. For example, the electrode pads 1b can be provided in the whole peripheral area in the principal surface 1a.

The number of the electrodes pads 1b and the number of the bump electrodes 2 are not limited to those in the first to sixth embodiments but any number can be used.

Each of the shape of the opening 4e in the tape substrate 4 and that of the opening 3c in the elastomer 3 is not limited to a rectangle. As long as the electrode pads 1b on the semiconductor chip 1 can be exposed, other shapes may be used.

Although the case where the tape substrate 4 in the CSP 30

is of the surface wiring structure has been described in the sixth embodiment, the tape substrate 4 used for the CSP 30 may be of the rear face wiring structure. In the tape substrate 4 of the rear face wiring structure, the opening 4i for bonding is formed in the tape base material 4g.

Further, the CSP structure obtained by the wire bonding described in the sixth embodiment can be applied to the CSPs 11, 12, 13, 14, 15, 16, 17, 18, 19 and 20 in the first to fifth embodiments. As the structure in this case, the leads 4c connected to the electrode pads 1b on the semiconductor chip 1 are replaced by the wires 24.

The plating layer with which the leads 4c on the tape substrate 4 used for the CSP 11 described in the first embodiment and the CSP 12 as the modification of the CSP 11 is also applied to each of the CSPs in the second to sixth embodiments.

The fan-in and fan-out semiconductor device (CSP) described in each of the first to sixth embodiments can be used for, for example, DRAM (Dynamic Random Access Memory), synchronous DRAM, static RAM, rambus DRAM, direct rambus DRAM, synchronous DRAM of a DDR (Double Data Rate) system, flash memory, ASIC (Application Specific IC), CPU (Central Processing Unit), gate array and the like. Products to which each of the above devices are applied are electronic devices such as module and card or portable small and thin electronic devices.

The CSP can be obviously applied to products other than the

module, card and portable small and thin electronic device.

The effects obtained by representative devices of the invention disclosed in the specification will be briefly described as follows.

(1) In the fan-in and fan-out semiconductor device (CSP), by providing the reinforcing member disposed on the outside of the semiconductor chip, the plurality of bump electrodes on the outside of the chip can be supported with reliability.

(2) By disposing the porous elastic member on the principal surface of the semiconductor chip, voids are not formed in the elastic member by the reflowing performed at the time of mounting the semiconductor device, so that the semiconductor device having excellent reflow resistance can be obtained. As a result, the reliability of the semiconductor device can be improved.

(3) By providing the tape substrate and the elastic member extending from the semiconductor chip to the outside and setting the total thickness of the polyimide resin of the tape base material in the tape substrate and the polyimide resin of the core layer in the elastic member to 100 to 175 μm, the bump electrodes on the outside of the chip can be supported with reliability without providing the reinforcing member. As a result, the production of the fan-in and fan-out semiconductor device (CSP) is facilitated and the plurality of bump electrodes on the outside of the chip can be supported with reliability.

What is claimed is:



1. A semiconductor device comprising:

a plurality of bump electrodes disposed over a principal surface of a semiconductor chip and on the outside of the principal surface of the chip;

a porous elastic member which is disposed on the principal surface of the semiconductor chip and in which an opening from which a connection terminal of the semiconductor chip is exposed is formed;

a tape substrate which is provided with a lead extending from the principal surface of the semiconductor chip to the outside of the chip, whose one end is electrically connected to the connection terminal and whose other end is electrically connected to the bump electrode, and in which an opening for exposing the connection terminal is formed;

a reinforcing member for reinforcing support for the bump electrodes disposed on the outside of the semiconductor chip; and

a sealing portion for sealing the connection terminal of the semiconductor chip and the lead of the tape substrate.

2. A semiconductor device according to claim 1, wherein the reinforcing member is made of a polyimide resin and is formed thickly.

3. A semiconductor device according to claim 1, wherein the

reinforcing member is made of a metal material.

4. A semiconductor device according to claim 1, wherein the reinforcing member is formed in a frame shape, and the semiconductor chip and the elastic member are disposed on the inside of the frame.

5. A semiconductor device according to claim 1, wherein the connection terminals of the semiconductor chip are disposed along a pair of facing sides in the principal surface of the semiconductor chip, in an intermediate area between the sides.

6. A semiconductor device according to claim 1, wherein the connection terminals of the semiconductor chip are disposed in the peripheries of the principal surface of the semiconductor chip along any of the sides of the principal surface.

7. A semiconductor device according to claim 1, wherein the porous elastic member has a three-layer structure of a core layer and adhesive layers formed on both sides of the core layer, the core layer is made of a porous fluorine plastic, and the adhesive layers are made of an epoxy-impregnated fluorine plastic.

8. A semiconductor device according to claim 1, wherein the tape base material in the tape substrate is made of a polyimide



resin and the lead made of copper foil is formed on the tape substrate.

9. A semiconductor device according to claim 1, wherein the total thickness of the reinforcing member made of a polyimide resin and the tape base material made of the polyimide resin in the tape substrate lies in a range from 100 to 175 μm.

10. A semiconductor device comprising:

an elastic member having an elastic member body disposed on the principal surface of a semiconductor chip and an elastic member reinforcing part which extends on the outside of the principal surface of the semiconductor chip, and having an opening from which a connection terminal formed on the principal surface of the semiconductor chip is exposed;

a tape substrate which is provided with a lead extending from the principal surface of the semiconductor chip to the outside of the chip, whose one end is electrically connected to the connection terminal and whose other terminal is electrically connected to a bump electrode as an external terminal and a tape base material, and which has an opening for exposing the connection terminal;

a sealing portion for sealing the connection terminal of the semiconductor chip and the lead connected to the connection terminal; and



bump electrodes as the external terminals disposed over the principal surface of the semiconductor chip and on the outside of the semiconductor chip,

wherein the bump electrode disposed on the outside of the semiconductor chip is supported and reinforced by the tape substrate and the elastic member reinforcing part of the elastic member.

11. A semiconductor device according to claim 10, wherein the elastic member has a core layer made of a polyimide resin.

12. A semiconductor device according to claim 10, wherein the elastic member has a core layer made of a polyimide resin, the tape base material in the tape substrate is made of a polyimide resin, and the total thickness of the core layer made of the polyimide resin and the tape base material lies in a range from 100 to 175 μm.

13. A semiconductor device according to claim 12, wherein thickness of the polyimide resin of the tape base material is 50 μm and the thickness of the polyimide resin of the core layer in the elastic member is in a range from 50 to 125 μm.

14. A semiconductor device according to claim 10, wherein the connection terminals of the semiconductor chip are disposed along



a pair of facing sides in the principal surface of the semiconductor chip, in an intermediate area between the sides.

15. A semiconductor device according to claim 10, wherein the connection terminals of the semiconductor chip are disposed in the peripheries of the principal surface of the semiconductor chip along any of the sides of the principal surface.

16. A semiconductor device according to claim 10, wherein the tape base material in the tape substrate is made of a polyimide resin and the lead made of copper foil is formed on one of the faces of the tape base material.

17. A semiconductor device according to claim 16, wherein the lead made of copper foil is formed on the surface opposite to the side connected to the elastic member, of the tape base material in the tape substrate.



18. A semiconductor device comprising:

a plurality of bump electrodes disposed over a principal surface of a semiconductor chip and on the outside of the principal surface of the chip;

an elastic member which has an elastic member body part disposed on the principal surface of the semiconductor chip and an elastic member reinforcing part extending on the outside of

the principal surface of the semiconductor chip, and in which an opening for exposing a connection terminal of the semiconductor chip is formed;

a tape substrate which is provided with a lead extending from the principal surface of the semiconductor chip to the outside of the chip, whose one end is electrically connected to the connection terminal and whose other end is electrically connected to the bump electrode, and in which an opening for exposing the connection terminal is formed; and

a sealing portion for sealing the connection terminal of the semiconductor chip and the lead of the tape substrate,

wherein the elastic member is formed in thickness equal to or thicker than that of the tape substrate, and support by the tape substrate for the bump electrodes disposed on the outside of the semiconductor chip is reinforced by the thick elastic member reinforcing part.

19. A semiconductor device according to claim 18, wherein the connection terminals of the semiconductor chip are disposed in an intermediate area between a pair of facing sides in the principal surface of the semiconductor chip so as to be almost in parallel with the sides.

20. A semiconductor device according to claim 18, wherein the connection terminals of the semiconductor chip are disposed in



the peripheries of the principal surface of the semiconductor chip so as to be almost in parallel with any of the sides of the principal surface.

21. A semiconductor device according to claim 18, wherein the tape base material in the tape substrate is made of a polyimide resin and the lead made of copper foil is formed on one of the faces of the tape base material.

22. A semiconductor device according to claim 21, wherein the lead made of copper foil is formed on the surface to which the elastic member is adhered, of the tape base material in the tape substrate.

23. A semiconductor device according to claim 18, wherein the thickness of the polyimide resin of the tape base material is 50 μm and the thickness of the polyimide resin of the elastic member is in a range from 50 to 125 μm.



24. A semiconductor device comprising:

a porous elastic member which extends on the outside of a principal surface of a semiconductor chip, and has an opening from which a connection terminal formed on the principal surface of the semiconductor chip is exposed;

a tape substrate which is provided with a lead extending

from the principal surface of the semiconductor chip to the outside of the chip, whose one end is electrically connected to the connection terminal and whose other end is electrically connected to a bump electrode as an external terminal, and which has an opening from which the connection terminal is exposed;

a sealing portion for sealing the connection terminal of the semiconductor chip and the lead of the tape substrate; and

a plurality of bump electrodes as external terminals disposed over the principal surface of the semiconductor chip and on the outside of the semiconductor chip,

wherein the tape base material in the tape substrate is formed thicker than the core layer of the porous elastic member, and the support by the tape substrate for the bump electrodes disposed on the outside of the semiconductor chip is reinforced by the thick tape base material.



25. A semiconductor device according to claim 24, wherein the tape base material in the tape substrate is made of a polyimide resin, and the lead made of copper foil is formed on one of the faces of the tape base material.

26. A semiconductor device according to claim 25, wherein the lead made of copper foil is formed on the face opposite to the side to which the elastic member is adhered, of the tape base material.

27. A semiconductor device according to claim 24, wherein the connection terminals of the semiconductor chip are disposed almost in parallel with a pair of facing sides in the principal surface of the semiconductor chip, in an intermediate area between the sides.

28. A semiconductor device according to claim 24, wherein the connection terminals of the semiconductor chip are disposed in the peripheries of the principal surface of the semiconductor chip almost in parallel with any of the sides of the principal surface.

29. A semiconductor device according to claim 24, wherein the porous elastic member has a three-layer structure of the core layer and adhesive layers formed on both sides of the core layer, the core layer is made of a porous fluorine plastic and the adhesive layers are made of an epoxy-impregnated fluorine plastic.

30. A semiconductor device according to claim 24, wherein the thickness of the tape base material in the tape substrate is 100 μm or thicker.



31. A semiconductor device comprising:

a plurality of bump electrodes disposed over a principal surface of a semiconductor chip and on the outside of the principal

surface of the chip;

an elastic member without a core layer, which extends on the outside of the principal surface of the semiconductor chip and in which an opening for exposing a connection terminal of the semiconductor chip is formed;

a tape substrate which is provided with a lead extending from the principal surface of the semiconductor chip to the outside of the chip, whose one end is electrically connected to the connection terminal and whose other terminal is electrically connected to the bump electrode, and in which an opening for exposing the connection terminal is formed; and

a sealing portion for sealing the connection terminal of the semiconductor chip and the lead of the tape substrate,

wherein the tape base material in the tape substrate is formed in thickness of 100 μm or thicker, and support by the tape substrate for the bump electrodes disposed on the outside of the semiconductor chip is reinforced by the tape base material having the thickness of 100 μm or thicker.

32. A semiconductor device according to claim 31, wherein the connection terminals of the semiconductor chip are disposed almost in parallel with a pair of facing sides in the principal surface of the semiconductor chip, in an intermediate area between the sides.

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33. A semiconductor device according to claim 31, wherein the connection terminals of the semiconductor chip are disposed in the peripheries of the principal surface of the semiconductor chip in almost parallel to any of the sides of the principal surface.

34. A semiconductor device comprising:

a plurality of bump electrodes disposed over a principal surface of a semiconductor chip and on the outside of the principal surface of the chip;

a porous elastic member which is disposed on the principal surface of the semiconductor chip and in which an opening from which a connection terminal of the semiconductor chip is exposed is formed;

a tape substrate which is provided with a lead extending from the principal surface of the semiconductor chip to the outside of the chip, whose part is exposed and whose one end is electrically connected to the bump electrode, and in which an opening for exposing the connection terminal is formed;

a bonding wire for bonding the connection terminal of the semiconductor chip to the exposed part of the lead of the tape substrate;

a reinforcing member for reinforcing support for the bump electrodes disposed on the outside of the semiconductor chip; and

a sealing portion for sealing the connection terminal of the semiconductor chip and the wire.

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35. A semiconductor device according to claim 34, wherein the tape base material in the tape substrate is made of a polyimide resin and the lead made of copper foil is formed on one of the surface and rear face of the tape base material.



36. A method of fabricating a semiconductor device, comprising the steps of:

preparing a semiconductor chip having a plurality of connection terminals on its principal surface;

preparing a tape substrate which is provided with a lead on one of its faces and in which an opening where a part of the lead is disposed is formed;

preparing an elastic member which is formed in thickness equal to or thicker than the tape substrate and has both an elastic member body part in which an opening of substantially the same shape as that of the opening in the tape substrate is formed and an elastic member reinforcing part formed on the outside of the elastic member body part;

adhering the tape substrate and the elastic member to each other while aligning the opening in the tape substrate and the opening in the elastic member:

exposing the connection terminals of the semiconductor chip from the two openings, disposing the elastic member body part on the principal surface of the semiconductor chip, allowing the

elastic member reinforcing part to extend on the outside of the principal surface of the semiconductor chip, and adhering the principal surface of the semiconductor chip and the elastic member to each other;

connecting the connection terminal of the semiconductor chip and the corresponding lead disposed in the opening in the tape substrate to each other;

sealing the connection terminal of the semiconductor chip and the lead connected to the connection terminal with a resin, thereby forming a sealed portion;

forming the bump electrode to be connected to the lead on one of the sides of the tape substrate; and

dicing the tape substrate into pieces,

wherein the support by the tape substrate for the bump electrodes disposed on the outside of the semiconductor chip can be reinforced by the thick elastic member reinforcing part.

37. A method of fabricating a semiconductor device according to claim 36, wherein as the tape substrate, a tape substrate such that the tape base material is made of a polyimide resin and the lead made of copper foil is formed on one of the faces of the tape base material is used.



38. A method of fabricating a semiconductor device according to claim 36, wherein as the tape substrate, a tape substrate in

which the tape base material is made of a polyimide resin and the lead made of copper film is formed on a face to which the elastic member is connected, of the tape base material is used and, in the case of forming the bump electrodes over the tape substrate, the bump electrodes are electrically connected to the leads through the openings for bumps provided in bump mounting positions in the tape base material.

39. A method of fabricating a semiconductor device according to claim 36, wherein when the tape substrate and the semiconductor chip are adhered to each other via the elastic member, the tape substrate extends from the whole periphery of the semiconductor chip to the outside.

40. A method of fabricating a semiconductor device, comprising the steps of:

preparing a semiconductor chip having a plurality of connection terminals on its principal surface;

preparing a tape substrate which has a lead on one of its faces and in which an opening where a part of the lead is disposed is formed;

preparing a porous elastic member in which an opening of substantially the same shape as that of the opening in the tape substrate is formed;

adhering the tape substrate and the elastic member to each

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other while aligning the opening in the tape substrate and the opening in the elastic member:

exposing the connection terminals of the semiconductor chip from the two openings, allowing the tape substrate and the elastic member to extend from the principal surface of the semiconductor chip to the outside, and adhering the principal surface of the semiconductor chip and the elastic member to each other;

connecting the connection terminal of the semiconductor chip and the corresponding lead disposed in the opening in the tape substrate to each other;

forming a sealed portion by sealing the connection terminal of the semiconductor chip and the lead connected to the connection terminal with a resin;

forming the bump electrode to be connected to the lead on one of the faces of the tape substrate; and

dicing the tape substrate into pieces,

wherein the support by the tape substrate for the bump electrodes disposed on the outside of the semiconductor chip can be reinforced by the tape base material in the tape substrate formed thicker than the core layer in the elastic member.

41. A method of fabricating a semiconductor device according to claim 40, wherein as the porous elastic member, an elastic member of which core layer is made of a porous fluorine plastic is used.

42. A method of fabricating a semiconductor device according to claim 40, wherein as the tape substrate, a tape substrate of which tape base material is made of a polyimide resin and in which the lead made of metal foil is formed on one of the faces of the tape base material is used.

43. A method of fabricating a semiconductor device according to claim 42, wherein the lead of the tape substrate is a lead made of copper foil.



44. A method of fabricating a semiconductor device according to claim 42, wherein as the tape substrate, a tape substrate in which the tape base material is made of a polyimide resin and is 100 μm thick or thicker is used.

45. A method of fabricating a semiconductor device according to claim 42, wherein as the tape substrate, a tape substrate in which the lead is formed on the face opposite to the side to which the elastic member is adhered, of the tape base material is used.

46. A method of fabricating a semiconductor device, comprising the steps of:

preparing a semiconductor chip having a plurality of connection terminals on its principal surface;

preparing a tape substrate which has a lead on one of its faces and has an opening in which a part of the lead is disposed;

preparing a porous elastic member in which an opening of substantially the same shape as that of the opening in the tape substrate is formed;

preparing a reinforcing member for reinforcing support by the tape substrate for the bump electrodes disposed on the outside of the semiconductor chip;

adhering the tape substrate and the elastic member to each other while aligning the opening in the tape substrate and the opening in the elastic member;

adhering the tape substrate and the reinforcing member to each other;

exposing the connection terminals of the semiconductor chip from the two openings, disposing the reinforcing member around the semiconductor chip, and adhering the principal surface of the semiconductor chip and the elastic member to each other;

connecting the connection terminal of the semiconductor chip and the corresponding lead disposed in the opening in the tape substrate to each other;

forming a sealing portion by sealing the connection terminal of the semiconductor chip and the lead connected to the connection terminal with a resin;

forming the bump electrode to be connected to the lead on one side of the tape substrate; and



dicing the tape substrate into pieces,

wherein the support by the tape substrate for the bump electrodes disposed on the outside of the semiconductor chip can be reinforced by the reinforcing member.

47. A method of fabricating a semiconductor device according to claim 46, wherein after adhering the tape substrate and the elastic member to each other, the reinforcing member is disposed around the elastic member and the tape substrate and the reinforcing member are adhered to each other.

48. A method of fabricating a semiconductor device according to claim 46, wherein after adhering the tape substrate and the reinforcing member to each other, the elastic member is disposed on the inside of the reinforcing member and the tape substrate and the elastic member are adhered to each other.

49. A method of fabricating a semiconductor device according to claim 46, wherein the reinforcing member is formed in a frame shape and the semiconductor chip is disposed on the inside of the frame of the reinforcing member.

50. A method of fabricating a semiconductor device according to claim 46, wherein as the reinforcing member, a reinforcing member made of a metal material is used.



51. A method of fabricating a semiconductor device according to claim 46, wherein as the reinforcing member, a reinforcing member made of a polyimide resin is used.

52. A method of fabricating a semiconductor device according to claim 51, wherein a tape substrate of which tape base material is made of a polyimide resin is used and the total thickness of the reinforcing member and the polyimide resin in the tape base material is 100 μm or thicker.

53. A method of fabricating a semiconductor device, comprising the steps of:

preparing a semiconductor chip having a plurality of connection terminals on its principal surface;

preparing a tape substrate which has a lead on one of its faces and has an opening for exposing the connection terminal of the semiconductor chip and in which a part of the lead is exposed;

preparing a porous elastic member in which an opening of substantially the same shape as that of the opening in the tape substrate is formed;

preparing a reinforcing member for reinforcing support by the tape substrate for the bump electrodes disposed on the outside of the semiconductor chip;

adhering the tape substrate and the elastic member to each

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other while aligning the opening in the tape substrate and the opening in the elastic member;

adhering the tape substrate and the reinforcing member to each other;

exposing the connection terminals of the semiconductor chip from the two openings, disposing the reinforcing member around the semiconductor chip, and adhering the principal surface of the semiconductor chip and the elastic member to each other;

bonding the connection terminal of the semiconductor chip and the exposed part of the corresponding lead of the tape substrate to each other by wire bonding;

forming a sealing portion by sealing the connection terminal of the semiconductor chip and a bonding wire bonded to the connection terminal with a resin;

forming the bump electrode to be connected to the lead on one side of the tape substrate; and

dicing the tape substrate into pieces,

wherein the support by the tape substrate for the bump electrodes disposed on the outside of the semiconductor chip can be reinforced by the reinforcing member.

