CLAIMS

1. Method for fabricating a semiconductor structure comprising a semiconductor layer (5) and a metallic layer (7), the method comprising the steps of:

   a) providing a semiconductor layer (5) comprising defects and/or dislocations (11a, 11b, 11c), wherein the semiconductor layer (5) is chosen from any one of GaN, Silicon, strained Silicon, Germanium, SiGe or a III-V material, III/N material, binary or ternary or quaternary alloy,

   b) removing material at one or more locations of the defects and/or dislocations (11a, 11b, 11c) such that parts of the defects and/or dislocations (11a, 11b, 11c) are removed thereby forming pits (13a, 13b, 13c) in the semiconductor layer (5) on top of the defects and/or dislocations (11a, 11b, 11c) in the semiconductor layer (5),

   c) passivating the pits (13a, 13b, 13c), wherein passivating the pits includes a step of at least partially filing the pits with a dielectric material (15), and

   d) providing the metallic layer (7) directly over the semiconductor layer (5) and directly over the passivated pits (13a, 13b, 13c), thereby forming a semiconductor-metallic junction, wherein the metallic layer is chosen from any one of Al, Au, Pt, chromium, palladium, tungsten, molybdenum or silicides from the same, polycrystalline or amorphous material and alloys or combinations thereof.

2. The method according to claim 1, wherein the material removal step b) comprises a step of etching the surface of the semiconductor layer (5) preferentially at one or more locations of the defects and/or dislocations (11a, 11b, 11c).

3. The method according to claims 1 or 2, wherein the dielectric material (15) is chosen from any one of silicon oxide, silicon nitride and mixtures thereof.

4. The method according to any one of claims 1 to 3, wherein the dielectric material (15) completely fills the pits (13a, 13b, 13c) formed in step b).

5. The method according to any one of claims 1 to 4, further comprising a step e) of polishing the surface of the semiconductor layer (5) after step c) and before step d).

6. The method according to any one of claims 1 to 5, wherein the metallic layer is provided by any one of physical vapor deposition (PVD), sputtering and chemical vapor deposition.

7. A semiconductor structure comprising a semiconductor layer (5) and a metallic layer (7) provided over the semiconductor layer (5),

wherein pits (13a, 13b, 13c) at least partially filed with a dielectric material (15) are arranged in the semiconductor layer (5) on top of dislocations and/or defects in the semiconductor layer,

wherein the metallic layer (7) is provided directly over the semiconductor layer (5) and directly over the pits at least partially filled with a dielectric material (15), thereby forming a semiconductor-metallic junction, and

wherein the semiconductor layer (5) is chosen from any one of GaN, Silicon, strained Silicon, Germanium, SiGe or a III-V material, III/N material, binary or ternary or quaternary alloy, and the metallic layer is chosen from any one of Al, Au, Pt, chromium, palladium, tungsten, molybdenum or silicides from the same, polycrystalline or amorphous material and alloys or combinations thereof.

8. The semiconductor structure according to claim 7, wherein the metallic layer (7) is provided on the semiconductor layer (5) and the pits extend up to the interface with the metallic layer (7).

9. The semiconductor structure according to claim 7 or 8, wherein the dielectric material (15) is chosen from any one of silicon oxide, silicon nitride and mixtures thereof.

10. The semiconductor structure according to any one of claims 7 to 9, wherein the pits are completely filed with the dielectric material (15).

11. A device using the semiconductor structure of any one of claims 7 to 10, in particular a Schottky diode.